Department of Electrical & Electronic Engineering

Information for Second Year Tutors

2011/2012, Autumn Term

Contents

Purpose of tutorials

Your tutor is your first contact point. He/she is there to follow your progress, advise you in learning approaches, have a listening ear when you have academic or non-academic problems, collect information from you to allow us to build a picture of you that will help us in writing reference letters for you in the future… In a tutorial session we encourage active contributions and discussions over a wide range of technical or non-technical subjects.

The tutorial booklet contains specific questions on the courses that are running during this term. We expect you to solve these questions or at least think about how they can be solved before you go to a tutorial. In the tutorial session the team can discuss the solutions and the course in general. These questions are aimed at making you revise lectures and think about their contents. We strongly encourage you to investigate the connections between the different courses not only those of year 2 but also investigate relationships with those of year 1. You will be surprised how different ideas and techniques can be exchanged between different courses.

For instance:

- Transients in Signals and systems and Devices (option course)
- Feedback networks in Analogue electronics and Control
- And many more – discover them

In this booklet you will find, apart from the tutorial questions, some information about the organization of the 2nd year course and the progression criteria. Please have a look at them.

I have changed the time table in order to try to reduce the total number of scheduled contact hours for Analogue, Digital, Power and Computer architecture in order to reduce your work load. I have also introduced an "Assimilation period" in week 6-7. Here you will have less lectures and more classes. This period is intended for you to **revise** the lectures, **solve** the problem sheets and **find help** in classes and office hours. Use this time effectively!!!

Although these changes have been introduced to improve your learning experience, this is only the first step. We need your feedback and help in order to further improve the timetable, within given restrictions, to make it work. Therefore I would really appreciate comments, critique and help with the timetable and course contents. So do not hesitate to talk to me or send me an e-mail on k.fobelets@imperial.ac.uk. An excellent contact point is your year representative who will be able to voice your comments at the staff –student meetings.

DO NOT SKIP TUTORIAL SESSIONS!

Inform your tutor when you are unable to come before the tutorial and contact him/her later on to ensure you are well and keeping up with the courses. Catch up in another tutorial session if possible.

Assessment Timetables

EE2 Electrical Engineering Lab

All timetabled lab assessments will be during scheduled lab sessions, in weeks 6 and 11 of Term.

Week	Work	Assessment	Cumulative Marks/90
Autumn			
6	2-5	Logbook interviewX2	10
6	2-5	Blackboard Test	20
11	7-10	Logbook interviewX2	30
11	7-10	Staff Interview	40

EE2 Group project and Technical communications

Week	Time	Assessment
Autumn		
2	5pm	Outline proposal
10	5 pm	Tech Com e-mail

EE2 Introduction to computer architecture

Week	Time	Assessment
Autumn		
6	In lab	Blackboard test
9	In lab	Blackboard test
11	Jan	Re-sit test are e-mailed

EE2 Humanities and Language tests

Note that these times might change.
Always check the course webpage for the most up-to-date information and read your e-mails!

Course time table - autumn term 2011

In an attempt to reduce the load on the 2nd year students I have changed the time table for the autumn term such that:

i) a *maximum* of 16 lecture contact hours are scheduled,
ii) an *assimilation period* is introduced (weeks 6-7)
iii) office hours are reduced from 8 to 3.

The EE2 courses consist of:
15 lecture hours (L)
8 class hours (C)
3 office hours (OH)

The time table for the autumn term courses (excl. maths, labs, humanities) is:
The tables below give the number of hrs/week of each L, C, OH and the last column gives total hours scheduled.

Digital electronics

week	1	2	3	4	5	6	7	8	9	10	11	TOT
L	0	2	1	2	2	1	0	2	2	2	2	16
C	0	0	0*	1	1	0	2	0	1	1	1	7
OH	0	0	0	0	0	1	1	0	0	0	1	3

Analogue electronics

week	1	2	3	4	5	6	7	8	9	10	11	TOT
L	0	2	1	2	2	1	0	2	2	2	2	16
C	0	0	1	1	1	0	2[†]	0	1	1	1	8
OH	0	0	0	0	0	1	1	0	0	0	1	3

Power

week	1	2	3	4	5	6	7	8	9	10	11	TOT
L	0	2	2	2	2	1	0	2	2	2	1	16
C	0	0	1	1	1	0	2	0	1	1	1	7
OH	0	0	0	0	0	1	1	0	0	0	1	3

Introduction to Computer architecture

week	1	2	3	4	5	6	7	8	9	10	11	TOT
L	0	2	2	2	2	1	0	2	2	2	0	15
C	0	0	0	0	0	0	2	0	0	0	0	2
OH	0	0	0	0	0	0	0	0	0	0	0	0

During the assimilation weeks 6-7, the lectures are reduced to limit the supply of new material and the classes are increased to enhance revision and problem solving. The students are strongly encouraged to use these weeks to revise lectures and solve problem sheets. Time tabled office hours are available in that period in order to encourage students to find help from course lecturers. These office hours can be regarded as technical tutoring time.

Any feedback on this system is gladly received. E-mail k.fobelets@imperial.ac.uk or talk to your year rep.

Digital Electronics II *Prof.* P. Cheung: p.cheung@imperial.ac.uk
Course web page: http://www.ee.ic.ac.uk/hp/staff/dmb/courses/dig2/dig2.htm

Week-by-week course content (year 2010-2011)
Note that this course has a new course lecturer. As a consequence some changes might be implemented during the running of the course.

			Introduction
Week 1		L1	Notation, Cause and Effect, Flipflops, Counters
			Interfacing Digital Systems
Week 2		L2	Synchronous bit-serial interfacing
Week 3	Prob 1		→ Problem Class: P1.1, P1.3, P1.5
		L3	Asynchronous bit-serial interfacing
Week 4			→ Problem Class: P1.8
		L4	Microprocessor-to-memory interface
Week 5	Prob 2		→ Problem Class: P2.2, P2.3, P2.4
		L5	Microprocessor-to-memory timing constraints
Week 6			→ Problem Class: P2.7, P2.8, P2.12
			Synchronous State Machines
		L6	Shift register control and sequencing
		L7	Data decoding with a counter
Week 7	Prob 3		→ Problem Class: P3.3, P3.5, P3.7
		L8	Synchronous state machine analysis
		L9	Synchronous state machine design
Week 8	Prob 4		→ Problem Class: P4.2, P4.5, P4.8
			Digital ↔ Analog Conversion
		L10	Digital-to-analog conversion
		L11	Analog-to-digital conversion: Flash and dither
Week 9	Prob 5		→ Problem Class: P5.5, P5.6, P5.8
		L12	Analog-to-digital conversion: Successive approximation
			Addition Circuits
		L13	Adders and propagation delays
Week 10	Prob 6		→ Problem Class: P6.2, P6.8, P6.9
		L14	Fast adders: bit inversion & carry lookahead
		L15	Fast adders: carry skip and carry save

EE2-3 ***Electrical Power Engineering*** *Prof.* T C Green: t.green@imperial.ac.uk
Course information on blackboard: **http://learn.imperial.ac.uk**

Lecture Plan

Week 2: Description of a typical generation, transmission and distribution system including the commercial separation of the tasks. Reasons for adoption of a sinusoidal voltage source system at 50/60 Hz and a variety of voltage magnitudes.
Review of calculation of real, reactive and apparent power and power factor.

Week 3: Comparison of efficiency of linear and switch-mode circuits for voltage conversion. Description of operating principles of step-down switch-mode power supplies. Derivation of equations governing steady-state operation of circuits.

Week 4: Design example of switch mode power supply. Step-up switch-mode power supplies.

Week 5: Reasons for adopting 3-phase generation and transmission. Phasor diagram construction for balanced star and delta systems. Phase and line voltage and current relationships. Power measurement and calculation in 3-phase systems.
Justification for rotating field pattern produced by a 3-phase winding. Operating principle of an induction machine. Justification of equivalent circuit of induction machine.

Week 6: Calculation of torque and power in 3-phase induction machine. Determination of torque-speed characteristic.

Week 7: Examples Classes

Week 8: Factors affecting energy available from sunlight. The photo-electric effect. Photo-voltaic cell technology. Power conversion and maximum power point tracking

Week 9: Circuits for DC to AC power conversion. Sinusoidal PWM and frequency spectra.
Properties of cables and overhead lines. Examination of relationship between real and reactive power flow with voltage magnitude and angle.

Week 10 Characteristics of synchronous generators. Explanation of synchronisation of multiple generators and control of frequency.

Topic List

1. The Electricity Supply Industry
    - 1.1 Power System Functions
    - 1.2 Transmission and Distribution
    - 1.3 Electricity Grid Operation
    - 1.4 Energy Sources and Use
    - 1.5 Revision of AC Power Calculation
2. Switch-Mode Power Supplies
    - 2.1 Linear versus Switch-Mode Conversion
    - 2.2 Buck SMPS
    - 2.3 Output Voltage Ripple
    - 2.4 Power Losses in Semiconductors
    - 2.5 Design of an SMPS
    - 2.6 Boost SMPS
    - 2.7 Control of Output Voltage
3. Three-Phase Power Systems
    - 3.1 A 3-Winding or 3-Phase Machine
    - 3.2 Star Connection
    - 3.3 Delta Connection
    - 3.4 Power Calculation and Measurement
4. Induction Machines
    - 4.1 General Features
    - 4.2 Flux Pattern
    - 4.3 Principle of Operation
    - 4.4 Equivalent Circuit
    - 4.5 Power Flow Diagram
    - 4.6 Torque Characteristic
5. Photo-Voltaic Energy
    - 5.1 Energy from the Sun
    - 5.2 Operating principle of PV Cell
    - 5.3 Construction of PV Cells and Panels
    - 5.4 Power Conversion
    - 5.5 Maximum Power Point Tracking
6. DC/AC Conversion
    - 6.1 Single Phase Inverters
    - 6.2 Three Phase Inverters
7. Power Flow in Lines and Cables
    - 7.1 Transmission Line Parameters
    - 7.2 P/ δ and Q/V
    - 7.3 Maximum Power Transfer
    - 7.4 Voltage Control
    - 7.5 DC versus AC
8. Synchronous Generators
    - 8.1 Principle of Operation
    - 8.2 Synchronisation

Analogue Electronics II *Dr.* T. G. Constandinou: **t.constandinou@imperial.ac.uk**
Course web page: http://cas.ee.ic.ac.uk/people/tc298/E22/index.html

Week-by-week course content

Week 2:	L1	Overview and fundamentals
Week 3:	L2-3	MOSFET devices and single stage MOSFET amplifiers
Week 4:	L4	BJT devices and single stage BJT amplifiers
	PS1	Problem Sheet 1 (Lectures 1-4)
	L5	Cascodes, current mirrors and reference circuits (1/2)
Week 5:	L6	Cascodes, current mirrors and reference circuits (2/2)
	PS2	Problem Sheet 2 (Lectures 5-6)
	L7	Differential amplifiers (1/2)
Week 6:	L8	Differential amplifiers (2/2)
	PS3	Problem Sheet 3 (Lectures 7-8)
Week 8:	L9-10	Frequency response
	PS4	Problem Sheet 4 (Lectures 9-10)
Week 9:	L11-12	Feedback and stability
	PS5	Problem Sheet 5 (Lectures 11-12)
Week 10:	L13	Integrated circuit technology
	PS6	Problem Sheet 6 (Lecture 13)
	L14	Operational amplifiers (as black boxes)
Week 11:	L15	Case study: design of a 2-stage op-amp in CMOS technology
	PS7	Problem Sheet 7 (Lectures 14-15)

Tutorial Problems

Weeks 2 & 3: (10/10 to 21/10)		Interview
Weeks 4 & 5: (24/10 to 04/11)	Digital Power	Tutorial Problem 1 Tutorial Problem 1
Weeks 6 & 7: (7/11 to 18/11)	Analogue Digital Power	Tutorial Problem 1 Tutorial Problem 2 Tutorial Problem 2
Weeks 8 & 9: (21/11 to 02/12)	Analogue Digital	Tutorial Problem 2 Tutorial Problem 3
Weeks 10 & 11: (05/12 to 16/12)	Analogue Power	Tutorial Problem 3 Tutorial Problem 3

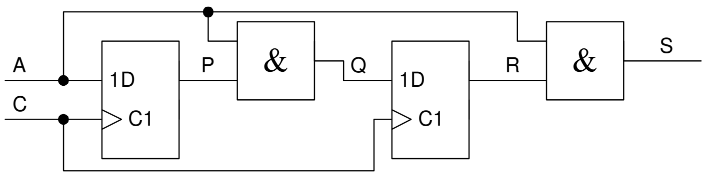
Students should collect the tutorial booklet from the copy room on Level 6

DIGITAL Week 4/5 – 24 Oct to 4 Nov

1. In the circuit below the propagation delay of the flipflops may vary between 4 and 7 ns while the propagation delay of the gates may vary between 2 and 6 ns.

   Calculate the minimum and the maximum propagation delays from each of A and C to each of P, Q and R and S.

   If the flipflops have a setup time of 5 ns, what is the maximum frequency of C?



SOLUTION

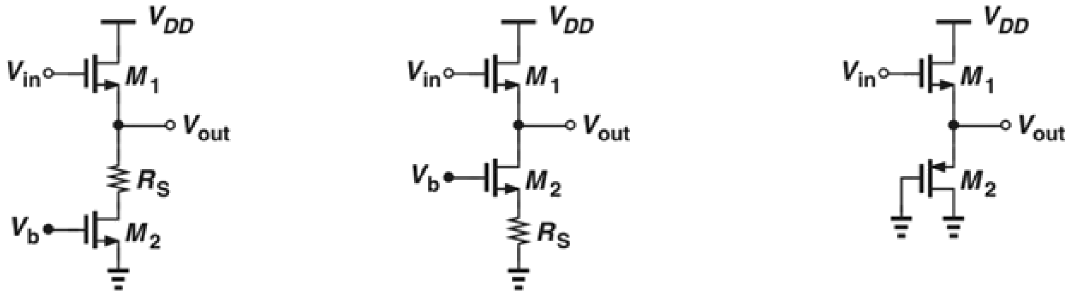
POWER Week 4/5 – 24 Oct to 4 Nov

1) A buck SMPS is required for a 5V power supply operating from an input that varies in the range 12 V ±25%. The output current of the SMPS will vary between 0.25 A when a small load is connected and 2.5 A when the maximum load is connected. The switching frequency is 10 kHz.
   (i) What range of duty-cycle is required?
   (ii) What inductor value should be chosen to keep the converter in continuous conduction even with the smallest load?
   (iii) If the output voltage ripple is not to exceed 50 mV (peak to peak) choose a capacitor such that 90% of the ripple is across the effective series resistance and 10% across the capacitance.

SOLUTION

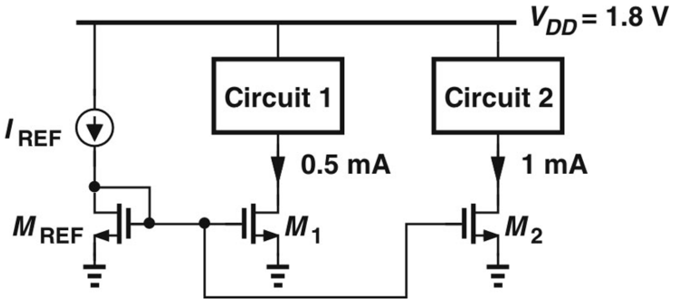
ANALOGUE Week 6/7 – 7 Nov to 18 Nov

1. Determine the voltage gain of the stages shown below. Assume λ≠0.



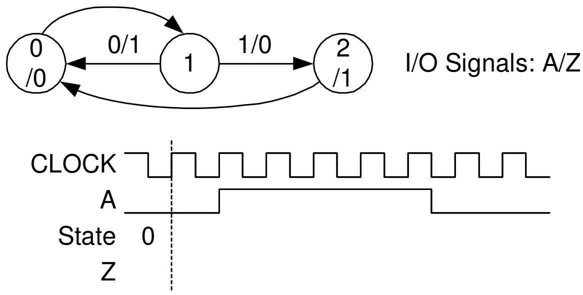
(a) (b) (c)

(d) In the arrangement below, M_1 and M_2 serve as current sources for Circuits 1 and 2. Design the circuit for a power budget of 3mW.



SOLUTION

2. The state diagram for a state machine is shown below. All state transitions occur on the rising edge of CLOCK. Complete the timing diagram be showing the sequence of states and the value of the output signal Z. Transitions in A occur slightly after the CLOCK edges.



SOLUTION

POWER Week 6/7 – 7 Nov to 18 Nov

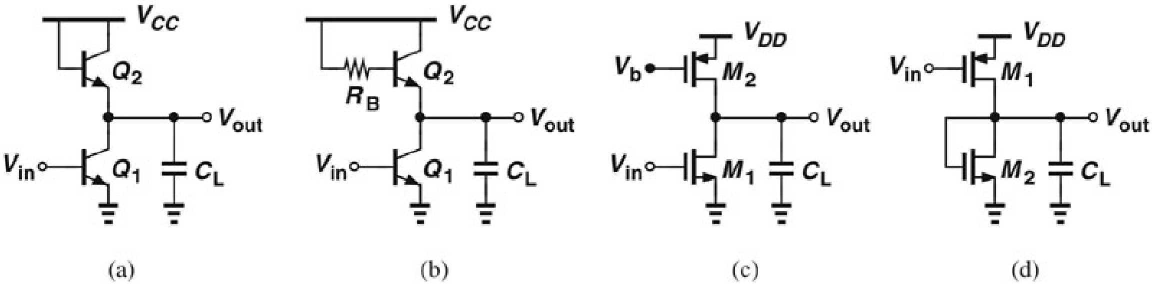
2) A set of three impedances of $(50 + j20)\ \Omega$ are connected via switches to a 1000 V three-phase supply. The switches allow the impedances to be connected in either star or delta.

   (i) Calculate the line currents and power dissipation in each configuration.

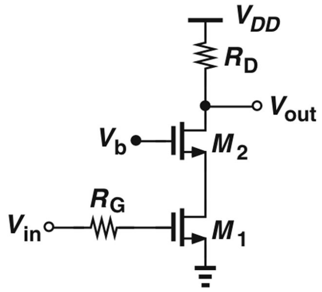
   (ii) What is the ratio between the currents and powers of the two configurations and is this result general.

SOLUTION

2. Determine the -3dB bandwidth of the circuits shown below. Assume $V_A=\infty$ but $\lambda>0$. Neglect other capacitances.



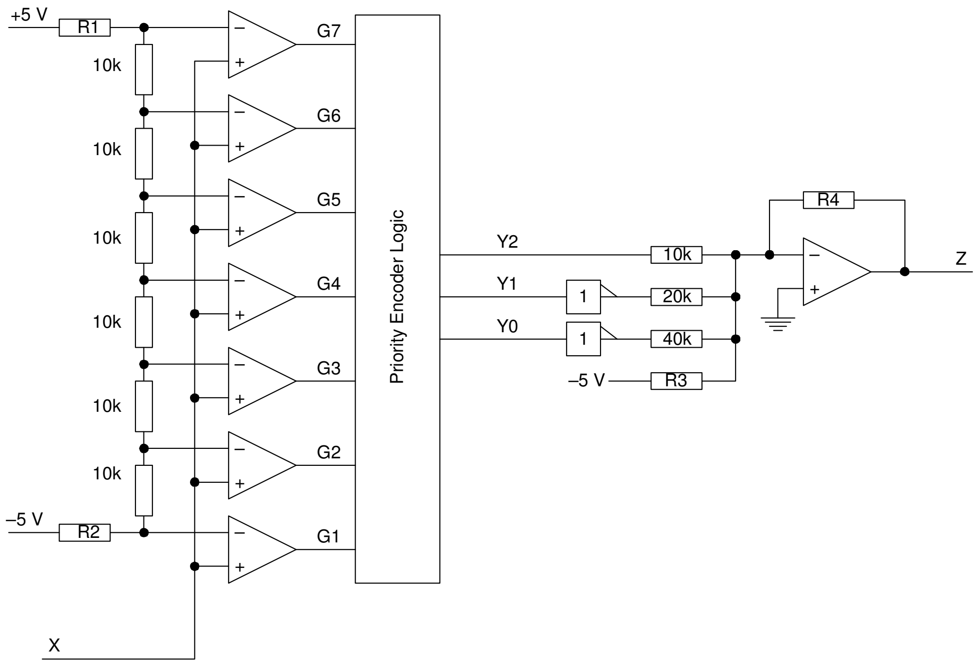
(e) We wish to design the MOS cascode shown below for an input pole of 5GHz and an output pole of 10GHz. Assume M_1 and M_2 are identical, I_D=0.5mA $C_{GS}=(2/3)WLC_{ox}$, $C_{ox}=12\text{fF}/\mu\text{m}^2$, $\mu_nC_{ox}=100\mu\text{A/V}^2$, $\lambda=0$, L=0.18um and $C_{GD}=C_0W$, where $C_0=0.2\text{fF}/\mu\text{m}$ denotes the gate-drain capacitance per unit width. Determine the maximum allowable values of R_G, R_D and the voltage gain. Use Miller's approximation for C_{GD1}. Assume an overdrive voltage of 200mV for each transistor.



SOLUTION

3. The circuit shows a flash A/D converter (which converts an input voltage X into a 3-bit signed number Y2:0) followed by a 3-bit D/A converter (which converts Y2:0 into an output voltage Z). The input and output scaling is arranged so that if *y* is the value of Y2:0, then Z = *y* = round(X) where X and Z are in volts, round() converts to the nearest integer and -4.5 < X < +3.5. The logic block has $Y2 = \overline{G4}$, $Y1 = G6 + G2 \cdot \overline{G4}$, $Y0 = G7 + G5 \cdot \overline{G6} + G3 \cdot \overline{G4} + G1 \cdot \overline{G2}$ and the logic levels are 0 and +5 volts.

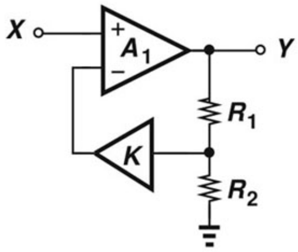
   Determine the values of R1, R2, R3 and R4.



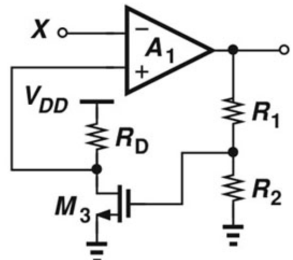
SOLUTION

ANALOGUE   Week 10/11 – 5 Dec to 16 Dec

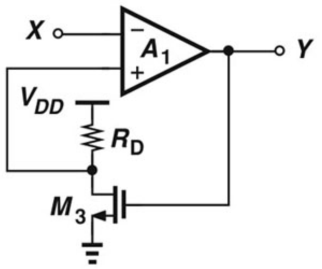
3. Calculate the loop gain of the circuits illustrated below. Assume the Op-amp exhibits an open loop gain of A1, but is otherwise ideal. Also, λ=0.



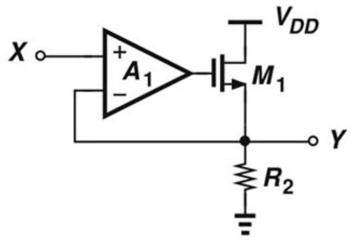
(a)



(b)

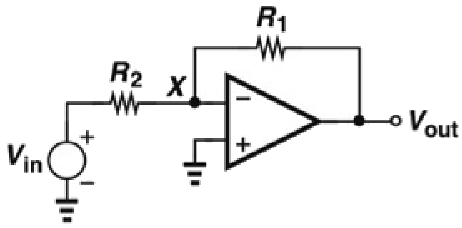


(c)



(d)

(e) Design the inverting amplifier shown below for a nominal gain of 8 and a gain error of 0.1%. Assume R_{out}=100Ω.



SOLUTION

3) A 4-pole, 3-phase, 50 Hz induction motor is rated to give 5 kW net output power. It has been estimated that the windage and friction loss of the machine is 200W; that the stator resistance is 0.4 Ω and that the rotor resistance referred to the stator is 0.5 Ω (the resistances are per-phase). The magnetising current can be assumed negligible.

Find the following.

i) The synchronous speed.

ii) The slip at a rotor speed of 1425 rpm and the frequency of the induced rotor currents.

iii) The rotor current (per-phase) if the rated power output is delivered at 1425 rpm.

iv) The rotor and stator copper losses and overall efficiency

SOLUTION

General Information

This document sets out the assessment structure of degrees awarded in Electrical and Electronic Engineering including the criteria for progression and the criteria for award of an honours degree. The degrees are composed of parts corresponding to the years of the course: four parts for an M.Eng. and three for a B.Eng. At the end of each year, except the final year, a decision is made on progression to the next part.

The Board of Examiners has the responsibility for setting and marking examinations and considering progression and award of honours. The Board of Examiners includes Departmental, College and External Examiners. It takes into account the marks awarded to each candidate in formal examinations and for other work, together with any other relevant information including statements from tutors. The board also considers examination prizes, admissibility to Part 3 of an M.Eng. course and supplementary tests to be taken by students failing marginally at Part 1, Part 2 and Part 3 (M.Eng. only).

Marks are not divulged to students by assessors or the Board of Examiners. The Registrar will release marks confirmed at Examiners' Meetings to individual students in accordance with the procedures of Imperial College.

All marks are held in the database to full machine precision. Occasionally, and for display purposes only, the marks will be rounded up to 0, 1 or 2 decimal places. The final course overall mark will be calculated from the database marks and not from the displayed marks.

Please note that marks for any examination, project, coursework, or other assessed work may be scaled (up or down) if deemed appropriate by the relevant Board of Examiners. This applies to marks for work completed at Imperial College London; and also marks for work completed at overseas institutions as part of a year abroad. You should treat marks gained at any other institution with particular caution as they are likely to be moderated before being incorporated into your overall results.

All work which is marked and graded must be retained. It may be required for re-submission to the Examiners at the end of the academic year.

The grade letters, mark boundaries and honours classes are as follows:

A - excellent	1st class standard	$A \geq 70\%$
B - very good	Upper 2nd class standard	$60 \leq B < 70$
C - competent	Lower 2nd class standard	$50 \leq C < 60$
D - adequate	3rd class standard	$40 \leq D < 50$
E - unsatisfactory		$30 \leq E < 40$
F - very unsatisfactory		$F < 30$

The year weightings applied in calculating the overall mark for a degree are as follows:

Year Weightings	B.Eng	M.Eng
Pt 1	1/6	1/8
Pt 2	1/3	1/4
Pt 3	1/2	5/16
Pt 4		5/16

Any information concerning factors which may have influenced students’ performance during the year (extenuating circumstances such as illness, personal problems) must be submitted to the Senior Tutor as soon as possible after the factor arises and in good time to be considered by the end of year Examiners’ Meeting. Evidence not brought to the attention of the examiners before the examiners meeting cannot be considered unless there is a good reason why it could not have been presented earlier

Also read:
Guidance Notes on Academic Progress
https://workspace.imperial.ac.uk/electricalengineering/public/Academic%20Progress%20v4.pdf

Part 2 Assessment

1. Lecture Modules

		Weighting (%)	ECTS Points	Assessment Method
E2.8 / E2.9	Mathematics	17.5	7	3-hour exam plus 2-hour exam
E2.1	Digital Electronics II	5.3	5	2-hour exam
E2.2	Analogue Electronics II	5.3	5	2-hour exam
E2.3	Power Engineering	5.3	5	2-hour exam
E2.4	Communication Systems	5.3	5	2-hour exam
E2.5	Signals and Linear Systems	5.3	5	2-hour exam
E2.6	Control Engineering	5.3	5	2-hour exam
E2.18 / E2.19	Algorithms and Data Structures / Computer Architecture	8	5	Two 1.5-hour exams
EE2-10A	Fields			
EE2-10B	Devices			
EE2-10C	Algorithms and complexity			
	Humanities Option	10	6	Varies and may include coursework
	Total	**70**	**50**	

Note: Students must take one humanities option for credit, and may choose to take an additional option not for credit with the agreement of the senior tutor. If two humanities options are chosen, the one in which the better mark is obtained will be credited in the Part 2 assessment.

2. Practical Work

		Weighting (%)	ECTS Points
	Electrical Laboratory	18	
	Computing Laboratory	5	
	Group Design Project	7	
	Total	**30**	**10**

3. Weighting of Part 2

The weighting of Part 2 is 1/3rd for B.Eng. and 1/4th for M.Eng.

4. Pass Mark and Progression Criteria

In order to progress to Part 3 of B.Eng., candidates are normally required to achieve the following:

a) 40% in each of the modules separately listed in (1) above
b) 40% in the aggregate of the practical work items listed in (2) above

In order to progress to Part 3 of M.Eng. (Technical or Management streams) candidates must meet the B.Eng. requirements plus achieve at least 50% in Mathematics **and** in the aggregate of the EE courses **and** a 50% overall mark for Part 2 **and** no SQTs.

In order to progress to Part 3 of M.Eng. (Year Abroad stream) candidates must meet the B.Eng. requirements plus achieve at least 50% in Mathematics **and** in the aggregate of the EE courses **and** a 55% overall mark for Part 2 **and** no SQTs.