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A novel 3D embedded gate FET Device concepts and modeling

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- Device geometry
  - Planar multi-gate structure
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- DC characteristics
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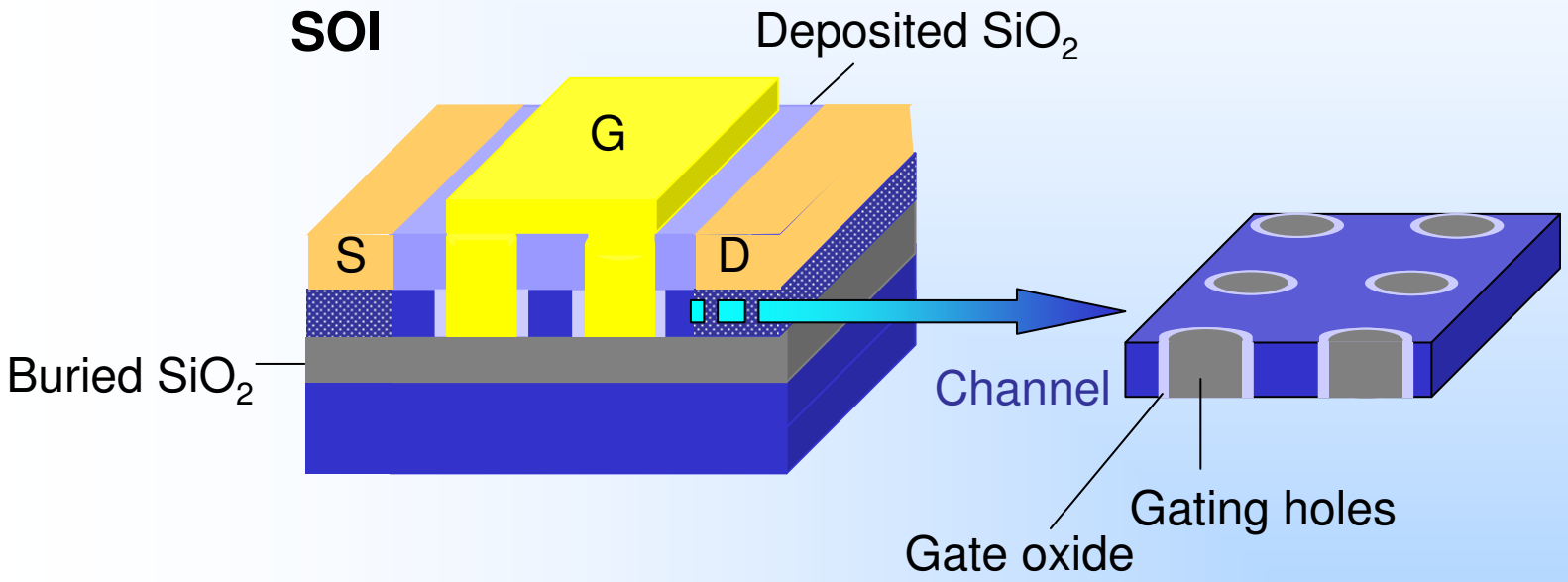
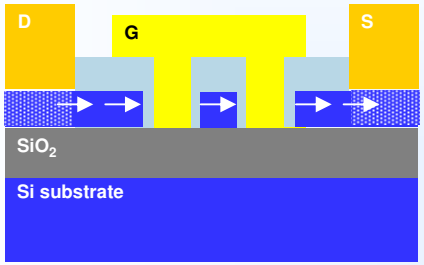
- AC characteristics
  - Planar structure
- Conclusions

Device geometry

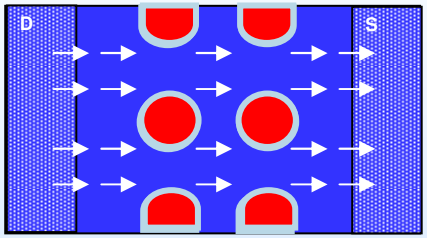


Planar structure
Multi gate control
Two rows of gate holes

Screen-Grid FET (SGFET)



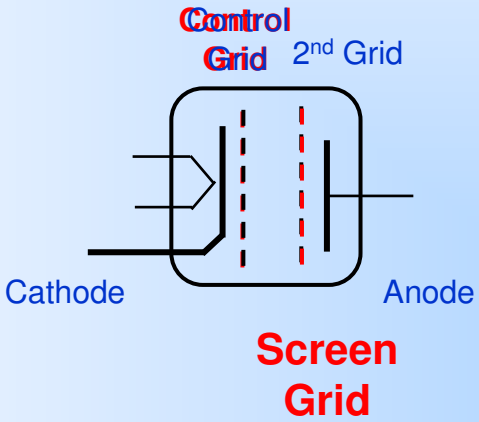
Side view cross section



Top view cross section

- Buried oxide
- Thermal oxide
- Silicon channel
- Contact
- Silicon substrate
- Current flow

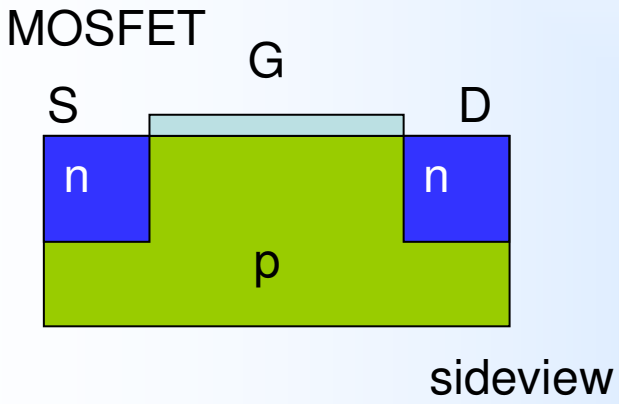
Tetrode

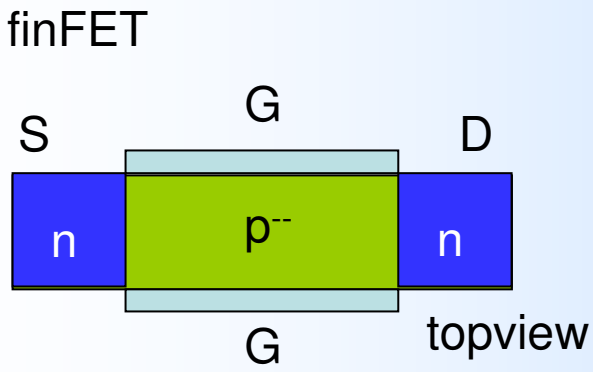


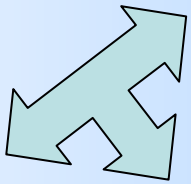
SG – 'Screen Grid' principle from vacuum tube technology

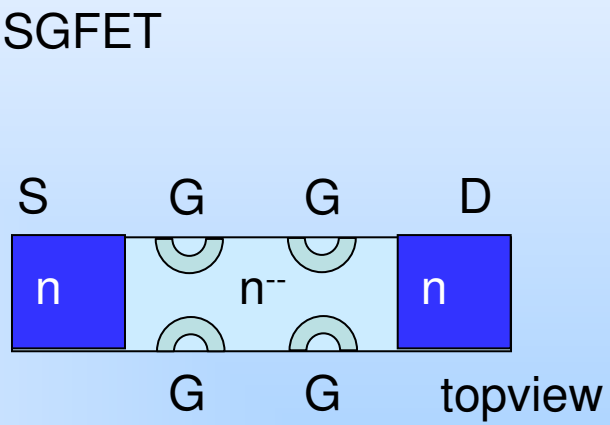
What sets the SGFET apart from other FETs?

1) Doping type of channel compared to ohmic contacts





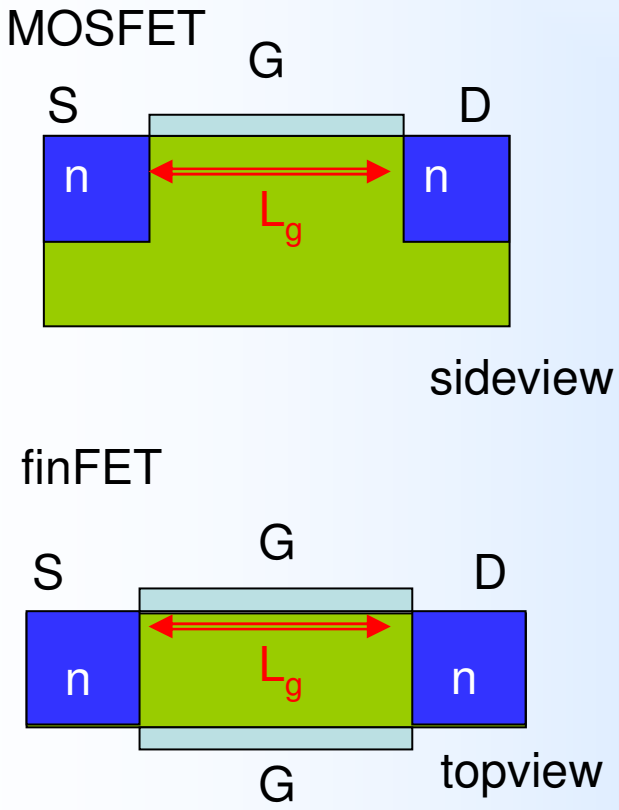


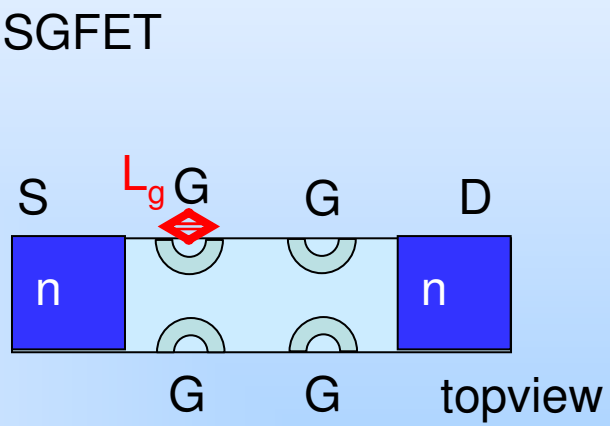


Work best with ***un-doped*** channel

What sets the SGFET apart from other FETs?

2) source-drain distance and channel length uncoupled



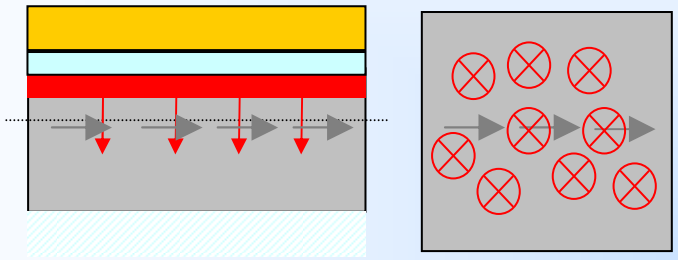


Gate length and source-drain distance
un-coupled

Operation of the SGFET.

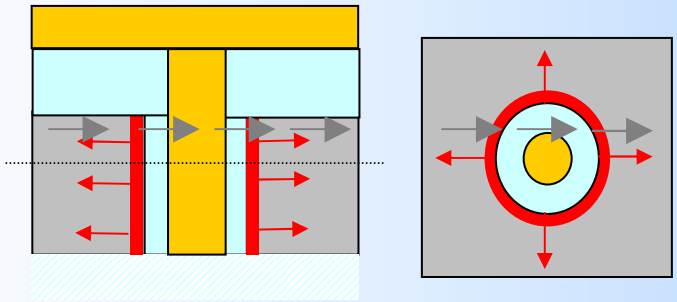
Gating Effect:

- **Conventional MOSFET gating**

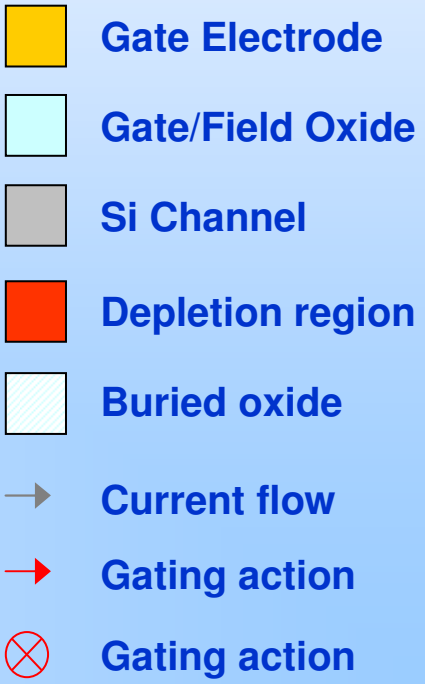


Side View **Top View**

- **SGFET gating**



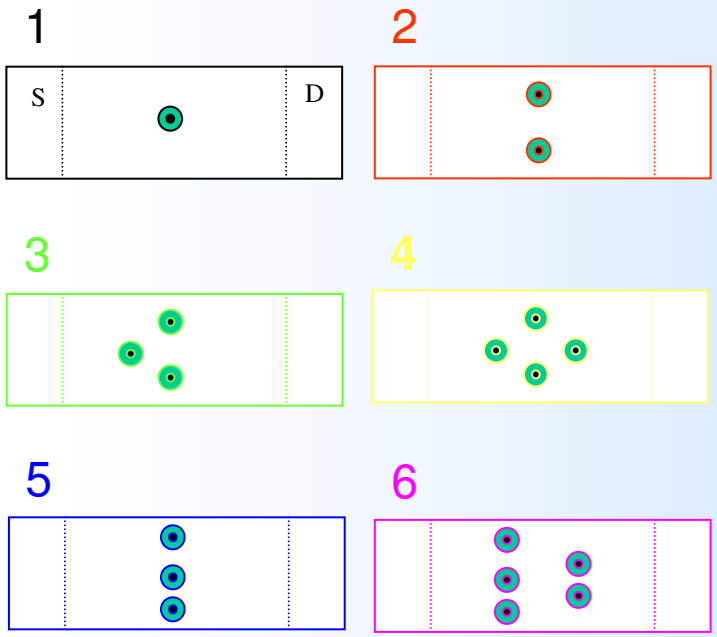
Side View **Top View**

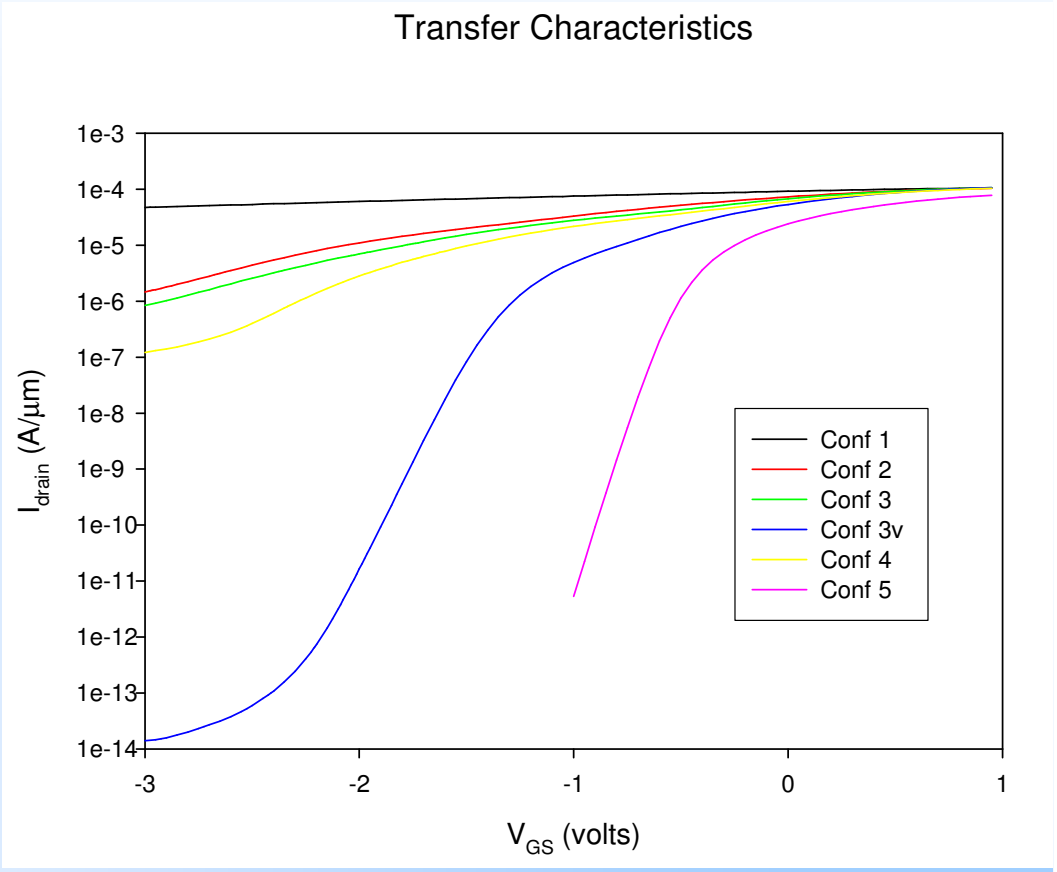


Operation of the SGFET.

Simulated depletion region V_D=0.05V, V_G=0V to -1V

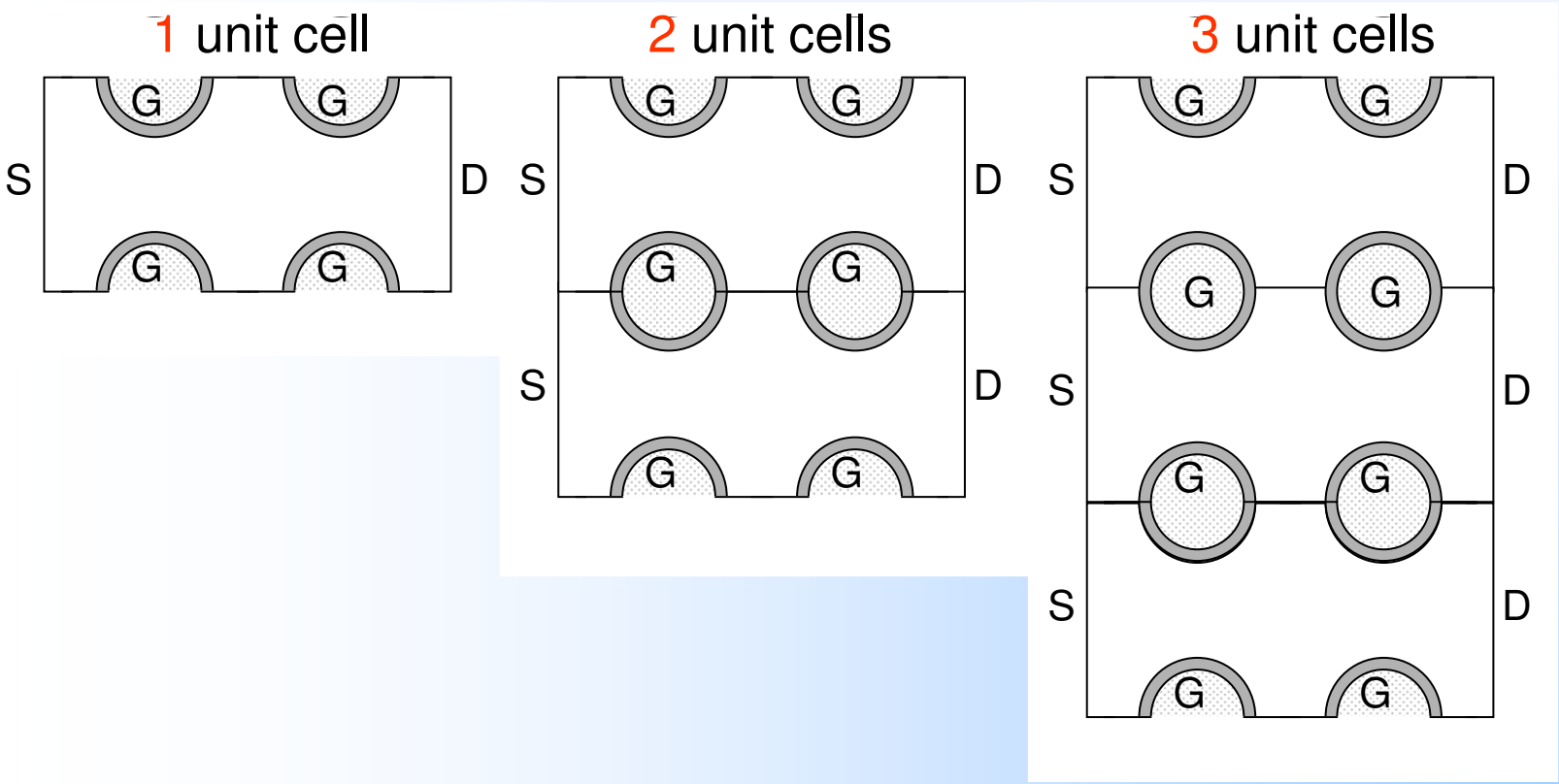
DC characteristics alternative gate configurations





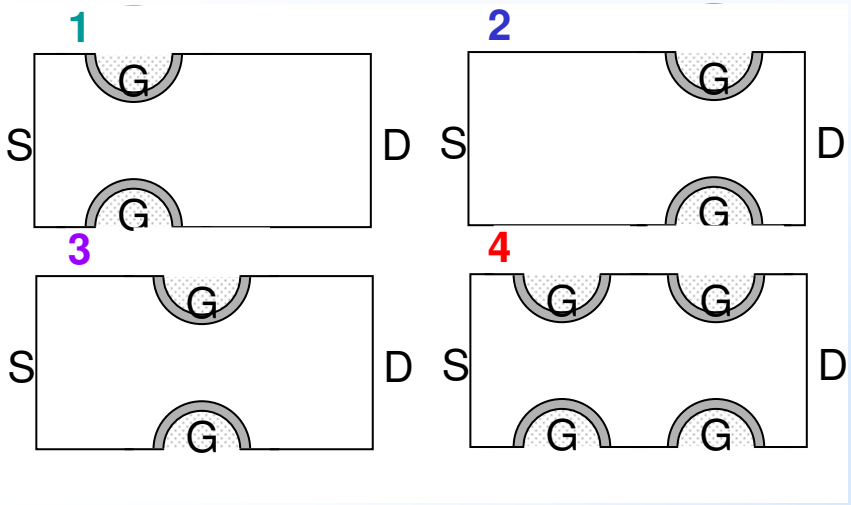
Optimal gate configuration

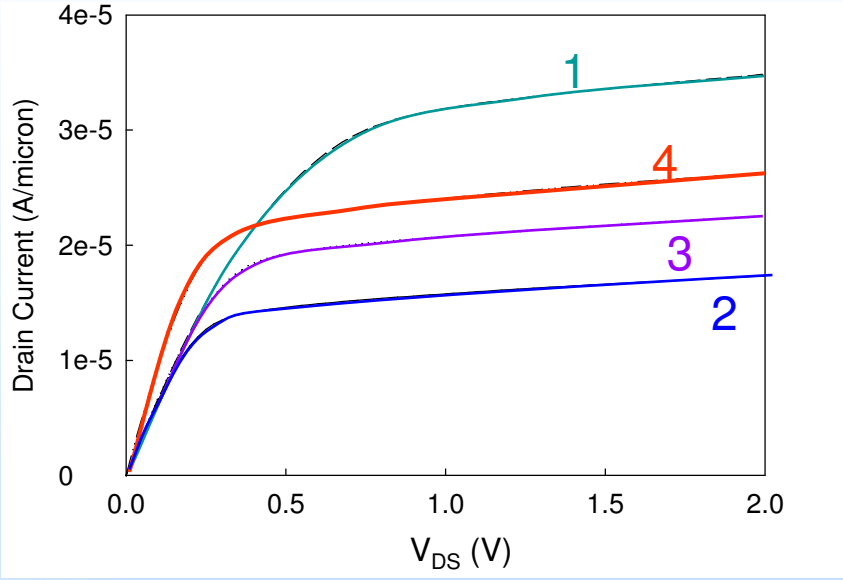
Principle of unit cell



$1I_{DS}$ $2I_{DS}$ $3I_{DS}$ nI_{DS}

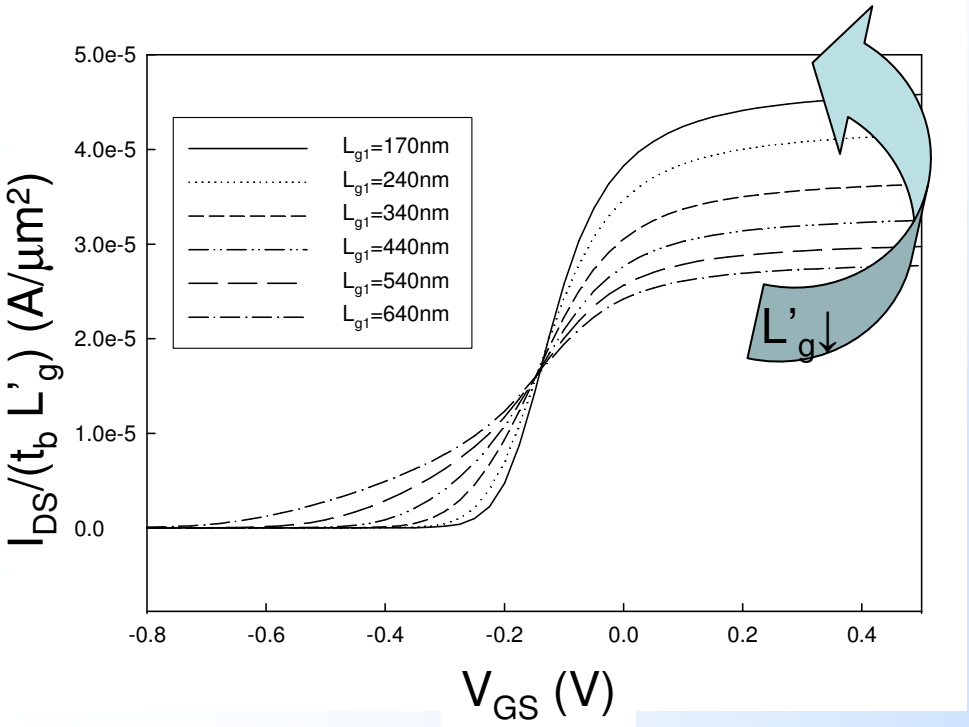
Influence of gate position

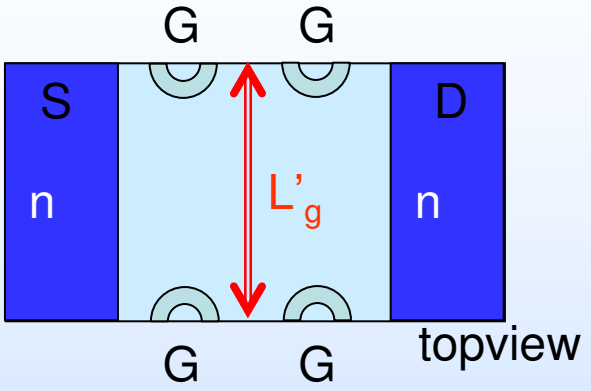


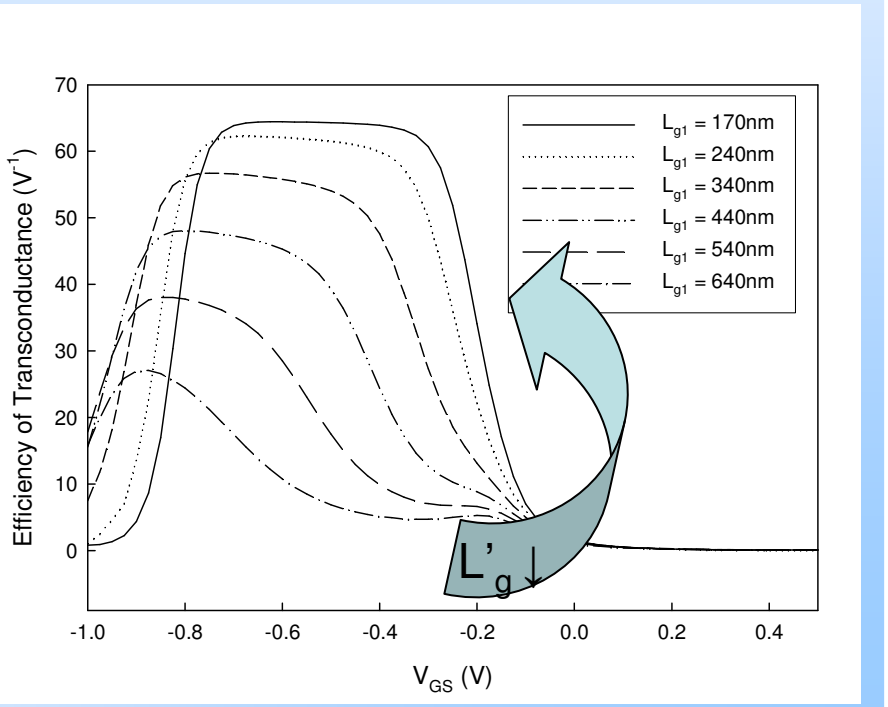


Configuration no	1	2	3	4
position of rows	1 row near source	1 row near drain	1 row middle	**2 rows**
DIBL (mV/V)	59.8	100.8	79.5	**42.4**
S (mV/dec) @V_{DS}=0.1V	71.3	70.7	70.0	**63.0**
g_{mmax}(S/μm^2) @V_{DS}=0.1V	1.17e-4	9.49e-5	1.07e-4	**1.55e-4**
g_{dmin}(μS/μm^2) @ V_{GS}-V_{th}=0V	0.846	0.397	0.487	**0.152**

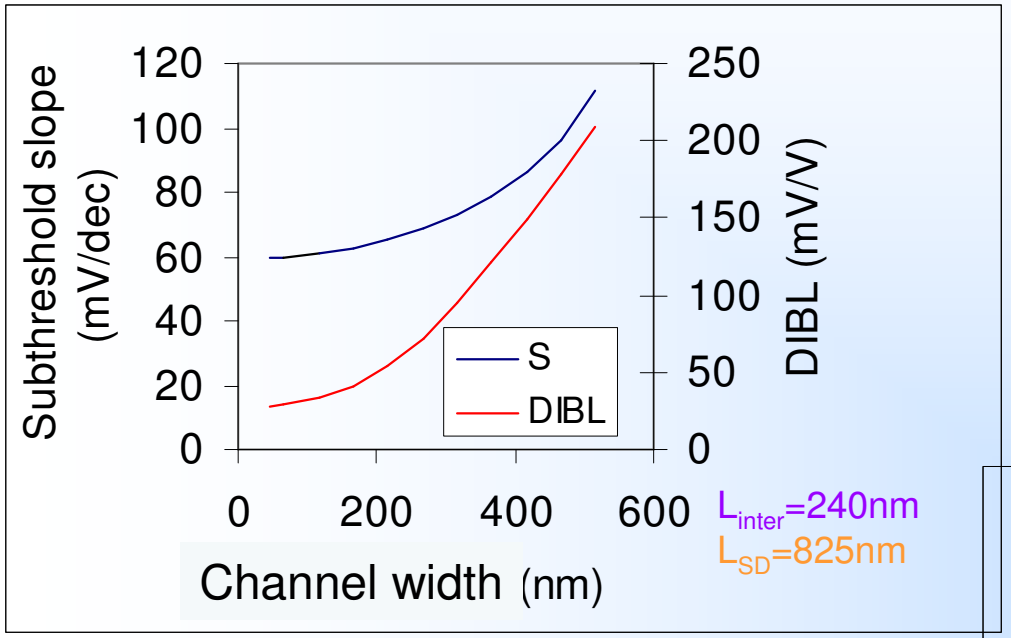
DC characteristics

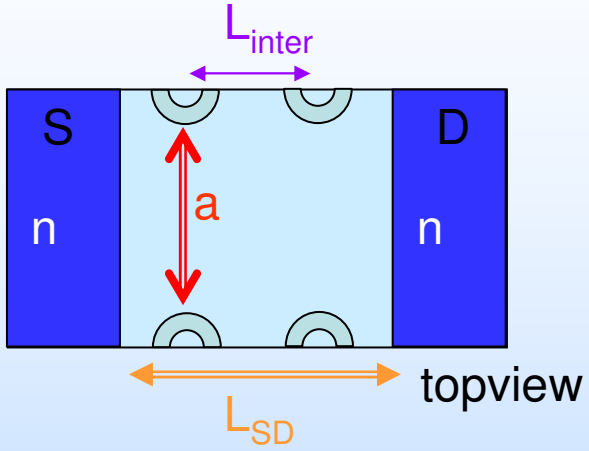






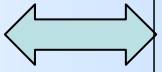
DC characteristics

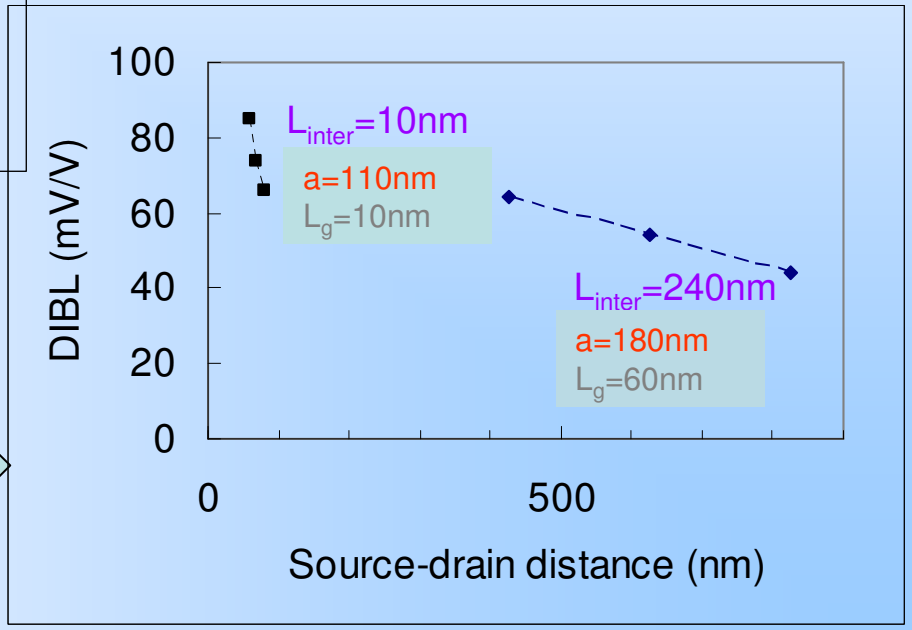




DIBL & S↓ for a ↓

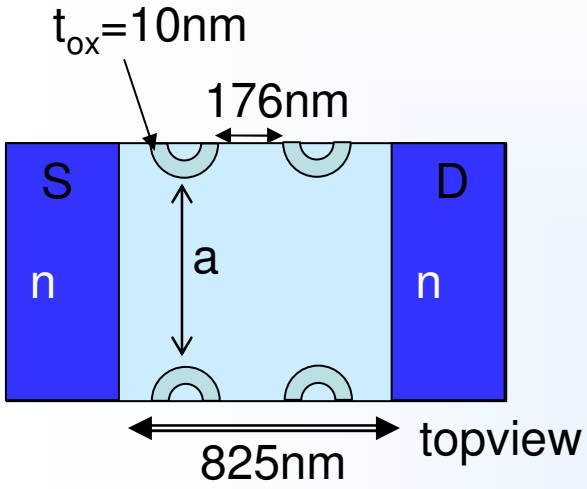
DIBL↑ for L_{SD}↓ but controlled by L_{inter}



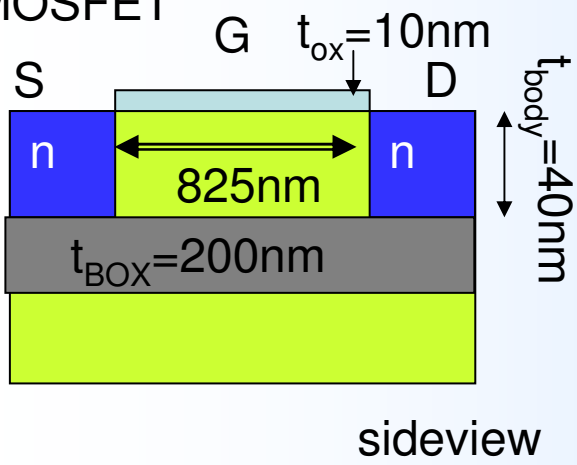


AC characteristics

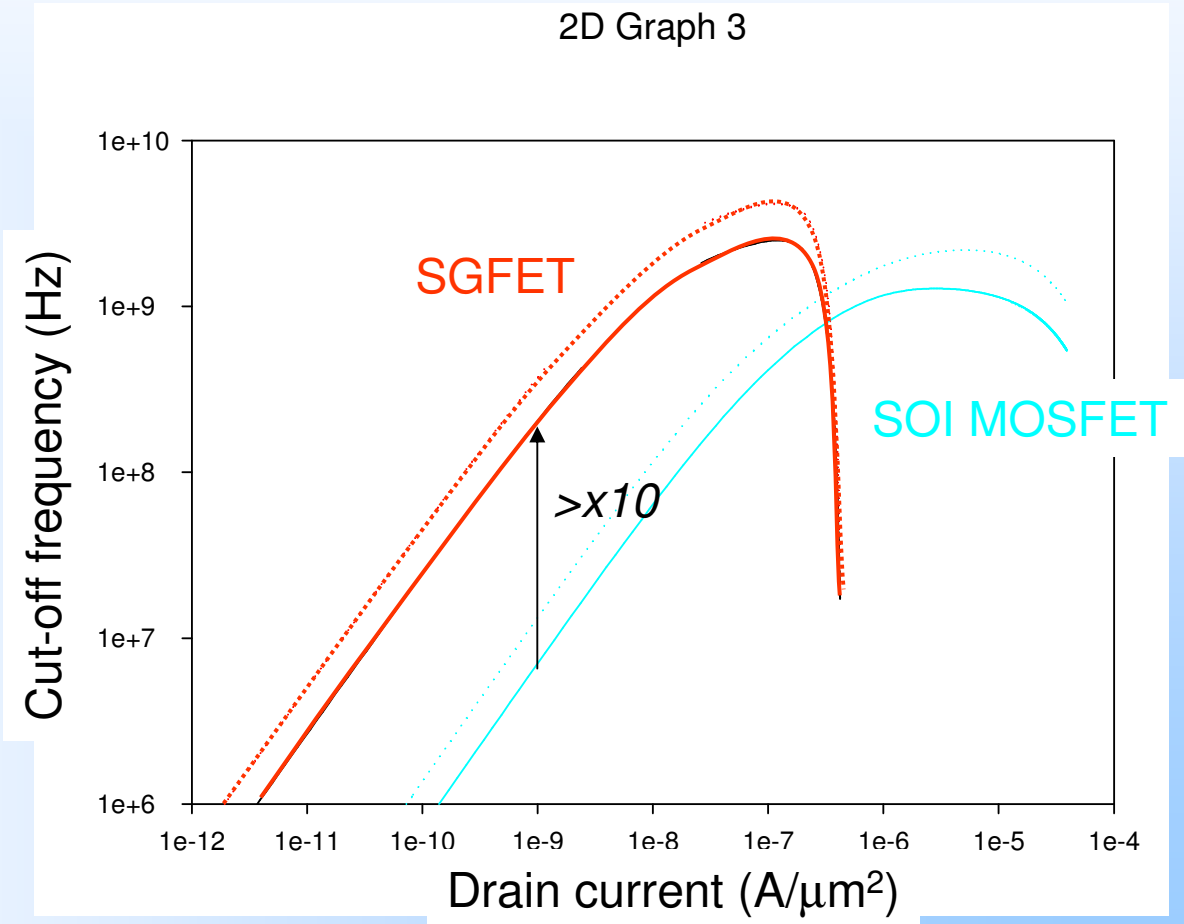
SGFET



MOSFET



$N_{channel}=10^{15}$ cm^{-3}



Conclusions

- Novel planar multi gated FET is proposed with a gating configuration similar to the tetrode → screen-grid FET
- Gate length and source-drain distance un-coupled leading to an alternative control of short channel effects:
- Second gating row acts as DIBL control and reduces S
- SGFET shows promising low power AC characteristics compared to a FDSOI MOSFET

- *Next stage*:
  - Digital characteristics: gate delay vs power information
  - Fabrication via e-beam and photo-lithography (INNOS, UK)