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3-D Modelling of the Novel Nanoscale Screen-Grid Field Effect Transistor (SGFET)

Pei W. Ding, Kristel Fobelets

Department of Electrical Engineering, Imperial College London, U.K.

J. E. Velazquez-Perez

Departamento de Fisica Aplicada, Universidad de Salamanca, Spain

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Outline

- Objectives/Motivation
- Proposed SGFET Structure
- Simulation Results
- Proposed Fabrication Steps
- Conclusions

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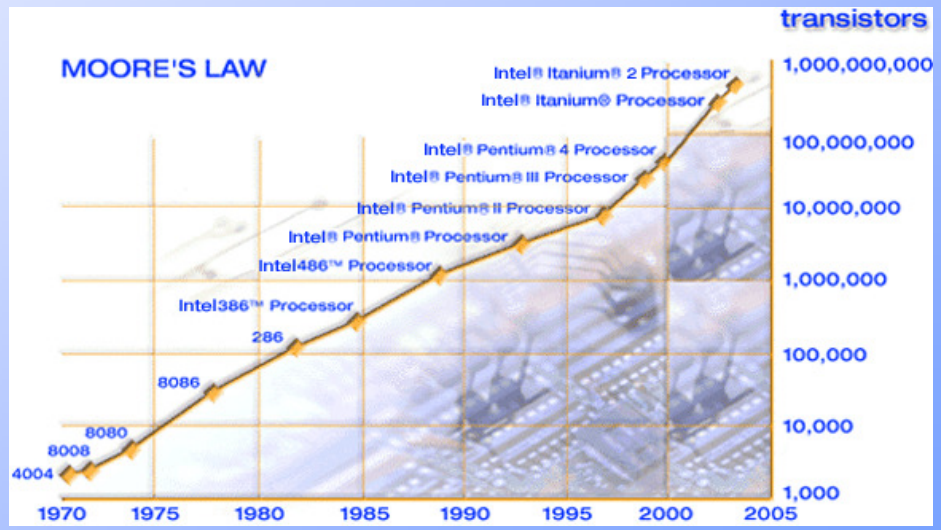
Objectives

To propose a novel 3-dimensional FET structure which overcomes the fundamental limitations of sub-micron FETs for future device scaling.

Current Requirements:

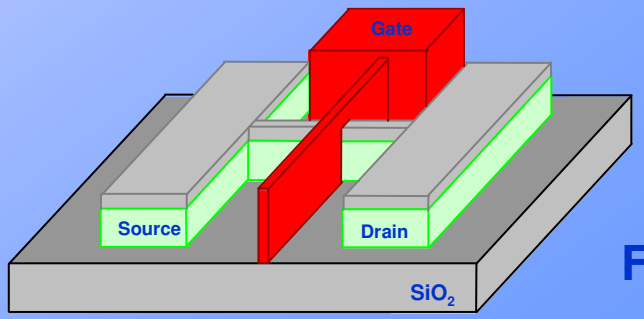
- High Operation Speed
- High packing density
- Low power consumption



Source: Logic Technology Development, Intel Corporation

Short channel effects:

- High electric field
- High leakage current
- High power consumption



FinFET

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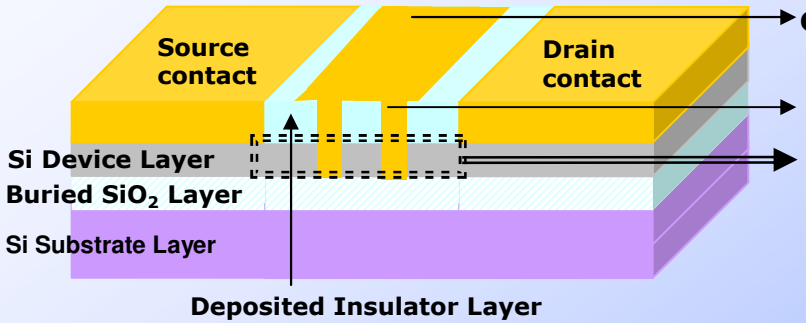
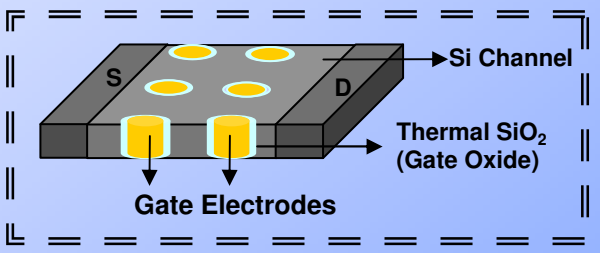
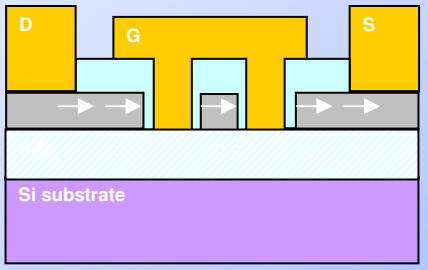
Proposed Structure

SGFET: a novel approach to 3-D gating

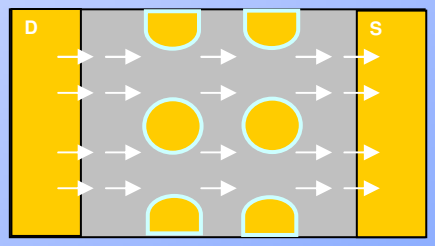


3-D view cross section





Side view cross section



Top view cross section

- Buried oxide
- Thermal oxide
- Silicon channel
- Contact
- Silicon substrate
- Current flow

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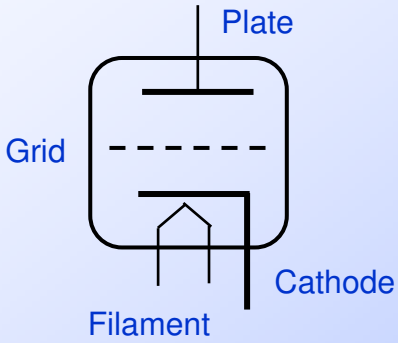
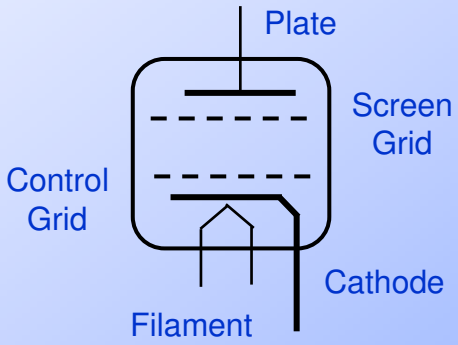
Proposed Structure

Why SGFET?

SG – 'Screen Grid' principle from vacuum tube technology



Triode



Tetrode

To reduce the capacitance and act as electrostatic shield between the control grid and the anode

SGFET:

Screen-Grid refers to the extra row of gate cyclinders that we add in to screen the effect of drain-induced barrier lowering, DIBL

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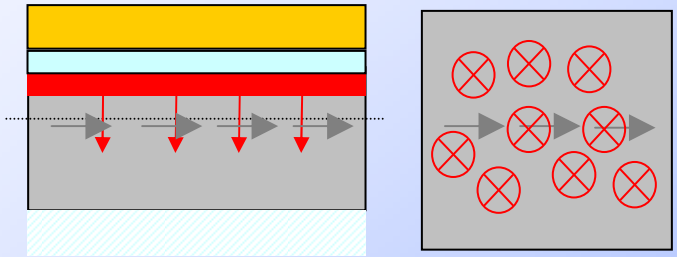
Proposed Structure

Gating Effect:

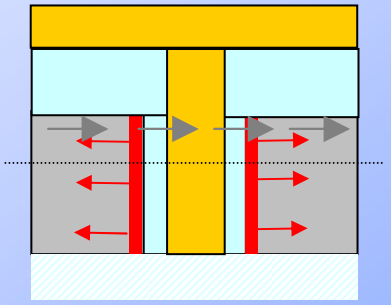
- Conventional MOSFET gating



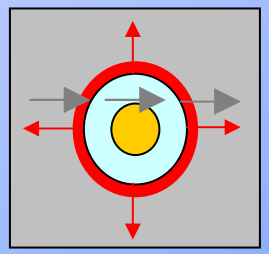
Side View

Top View

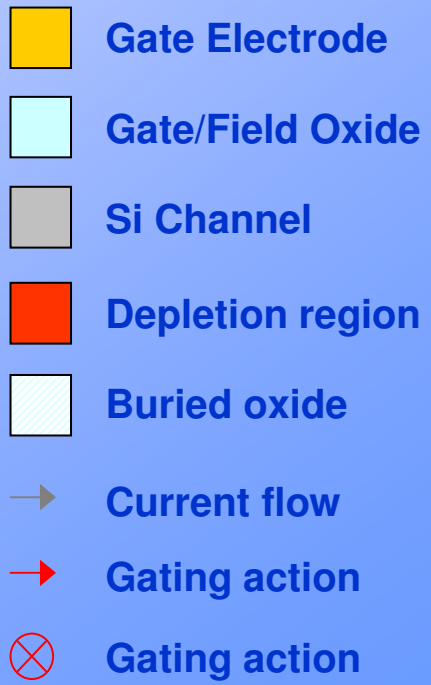
- SGFET gating



Side View



Top View



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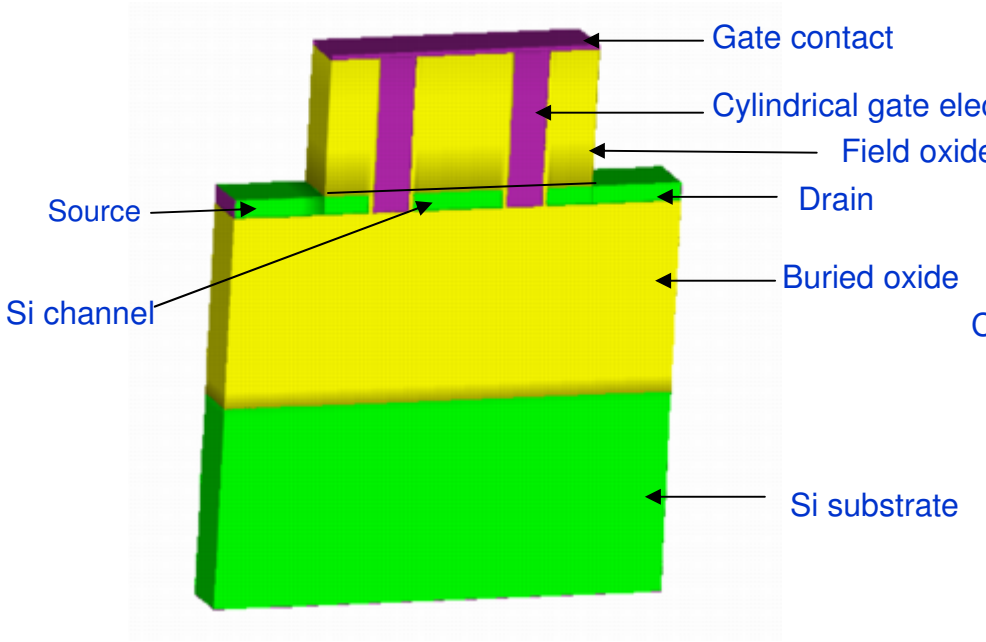
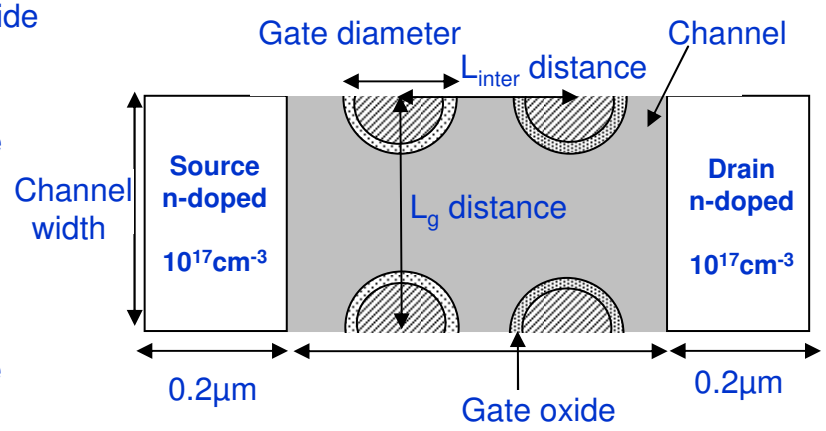
3-D Simulations

SGFET: TAURUS™ Simulation



3-D view

Simulation Structure



Top cross-sectional view

General dimensions:

Si channel thickness=40nm . buried oxide thickness=460nm . field oxide thickness=300nm
Lg=130nm . Linter=300nm . S-D distance=600nm . gate diameter=100nm
gate oxide thickness = 10nm . source and drain regions doping density=1 x $10^{17}cm^{-3}$(n-type)

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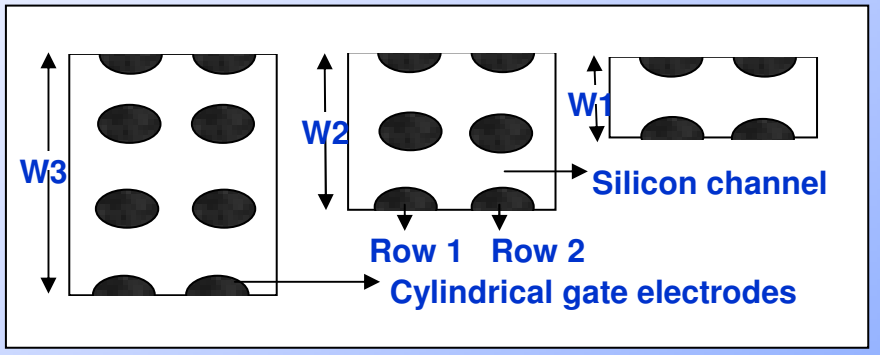
3-D Simulation Results

Influence of Channel Width



1) Linear operation region V_{DS} = 0.05V

	I_{DS} @ V_{GS} = 0V (A)	I_{DS} (A/μm)	V_T (V)	S (mV/decade)
Single W1	1.92×10^{-7}	1.48×10^{-6}	-0.29424	62.57
Double W2	3.88×10^{-7}	1.49×10^{-6}	-0.29346	62.55
Triple W3	5.81×10^{-7}	1.49×10^{-6}	-0.29345	62.51

2) Saturated operation region V_{DS} = 3.00V

	I_{DS} @ V_{GS} = 0V (A)	I_{DS} (A/μm)	V_T (V)	S (mV/decade)
Single W1	9.59×10^{-7}	7.37×10^{-6}	-0.23049	61.88
Double W2	1.93×10^{-6}	7.42×10^{-6}	-0.22962	61.88
Triple W3	2.89×10^{-6}	7.41×10^{-6}	-0.22962	61.81

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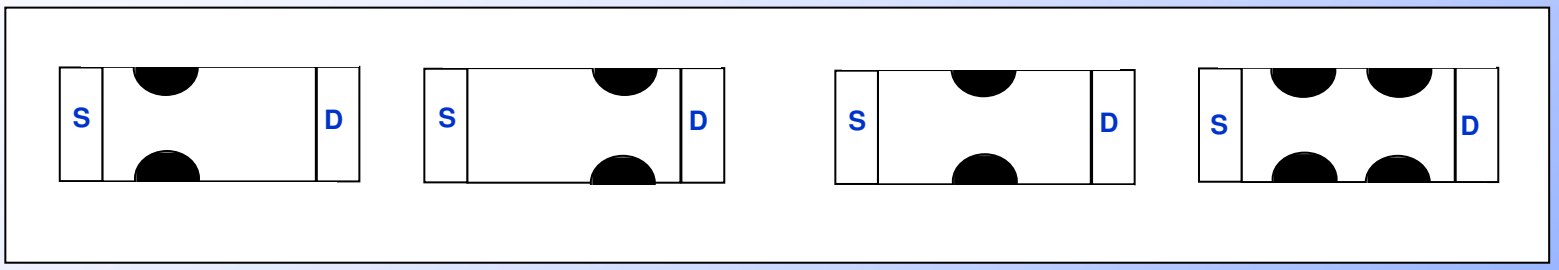
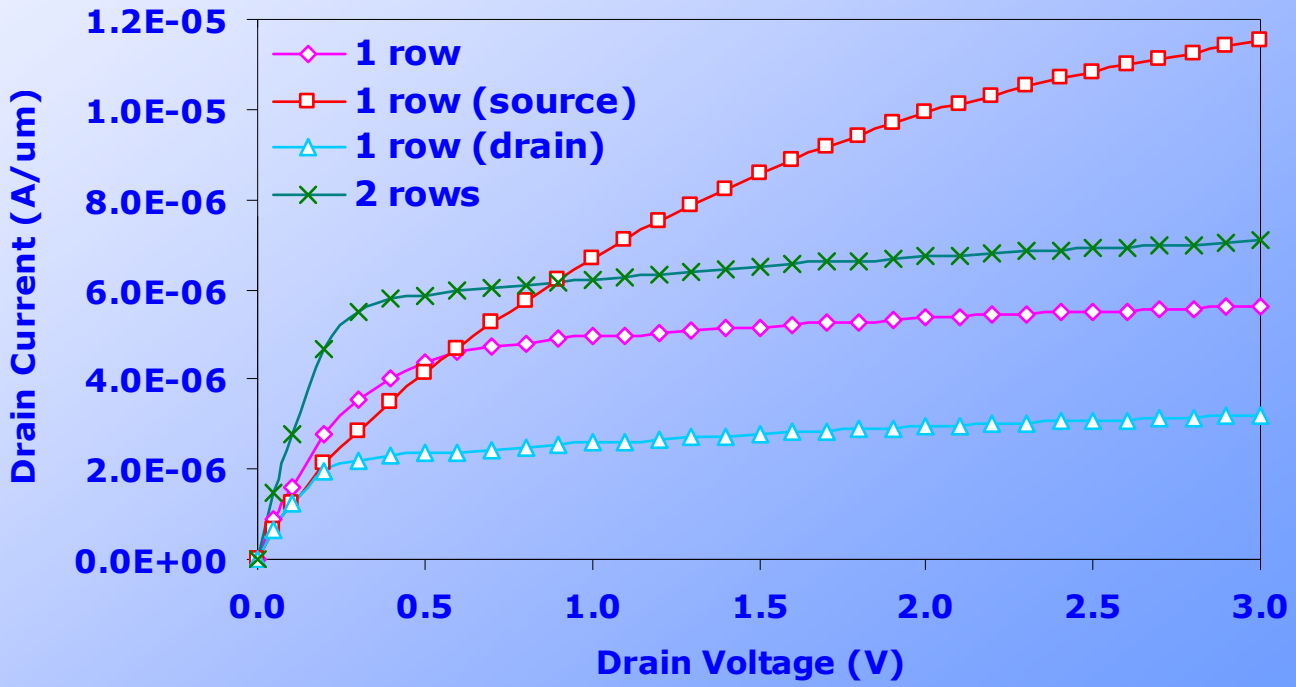
3-D Simulation Results

Influence of Geometrical Structure (Number of Rows/Arrangement)





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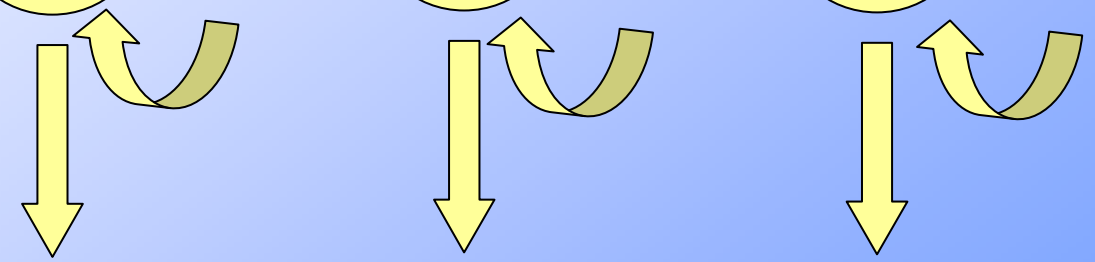
3-D Simulation Results

Influence on DIBL reduction (Threshold Voltage Shift)

S-D distance (nm)	80		70		60	
Number of rows	2 rows	1 row	2 rows	1 row	2 rows	1 row
$\Delta V_T/\Delta V_D$(mV/V)	-66.3	-142.7	-74.4	-182.4	-84.95	-207.08



Row 2 acts as screen grid to DIBL effect!

"SGFET"

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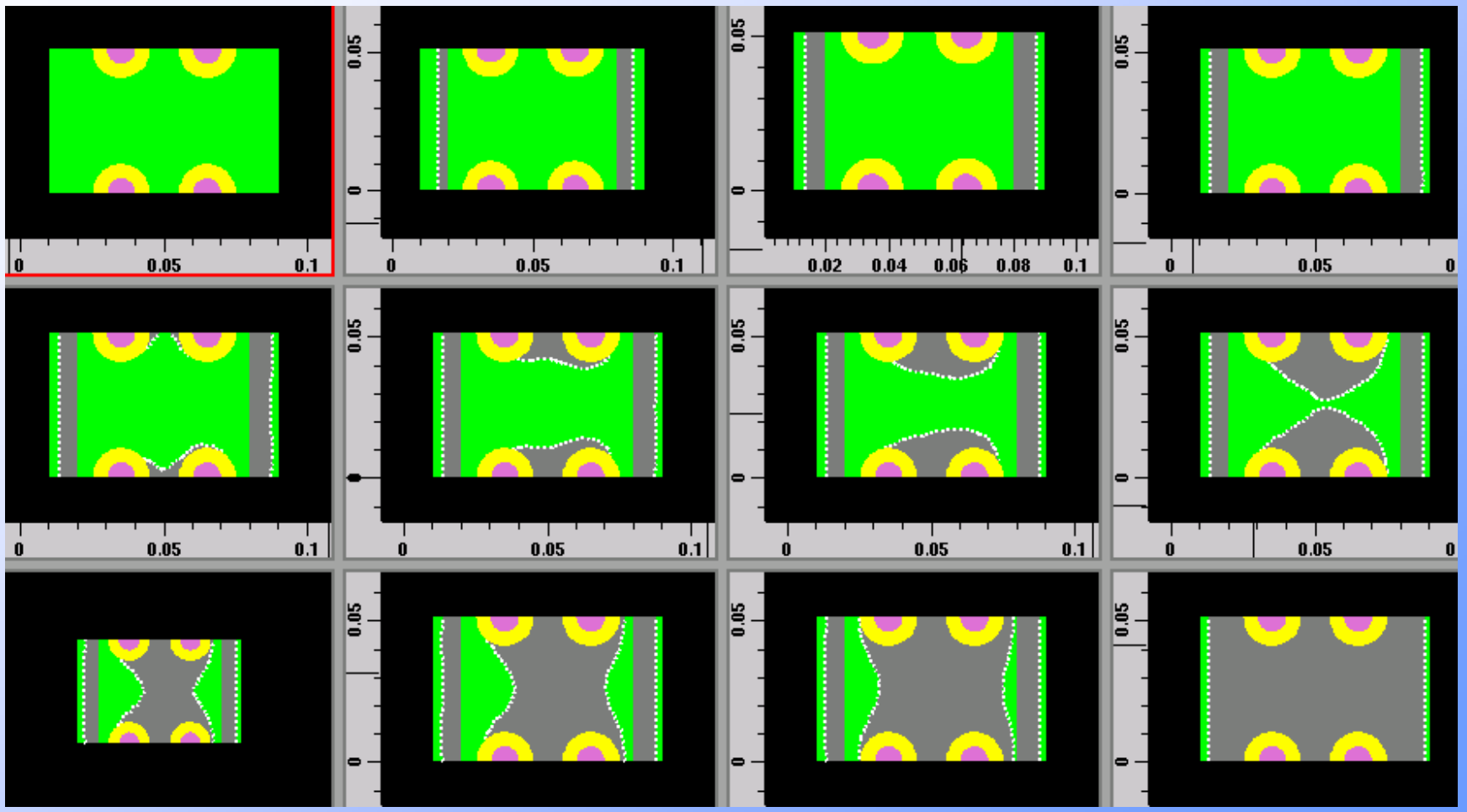
3-D Simulation Results

Simulated depletion region V_D=0.05V, V_G=0V to -1V



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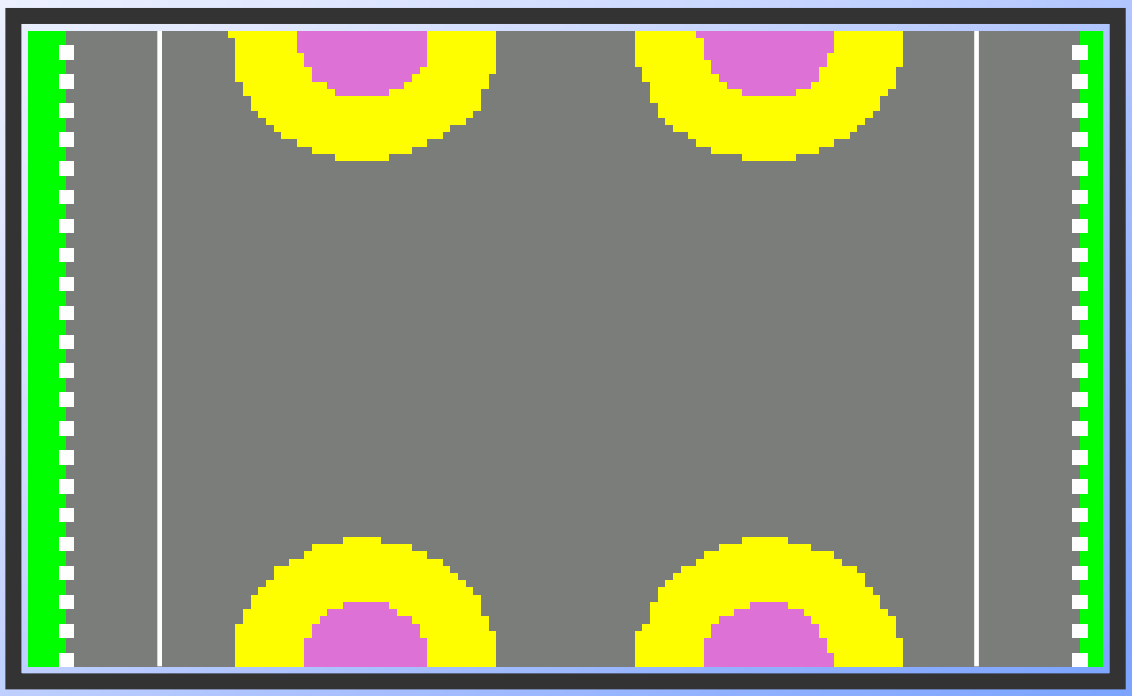
3-D Simulation Results

Simulated depletion region V_D=0.05V, V_G=0V to -1V



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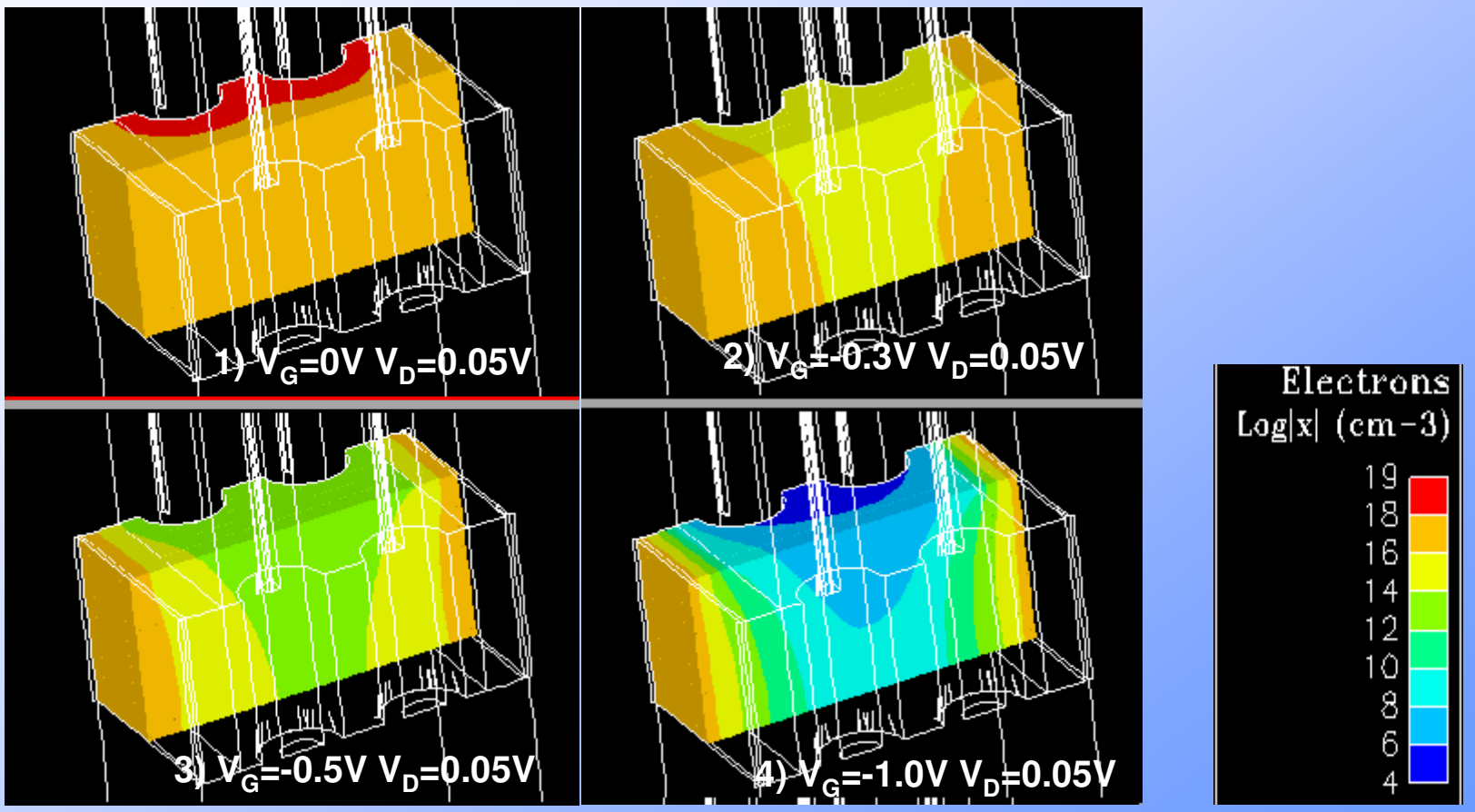
3-D Simulation Results

Simulated electron concentrations



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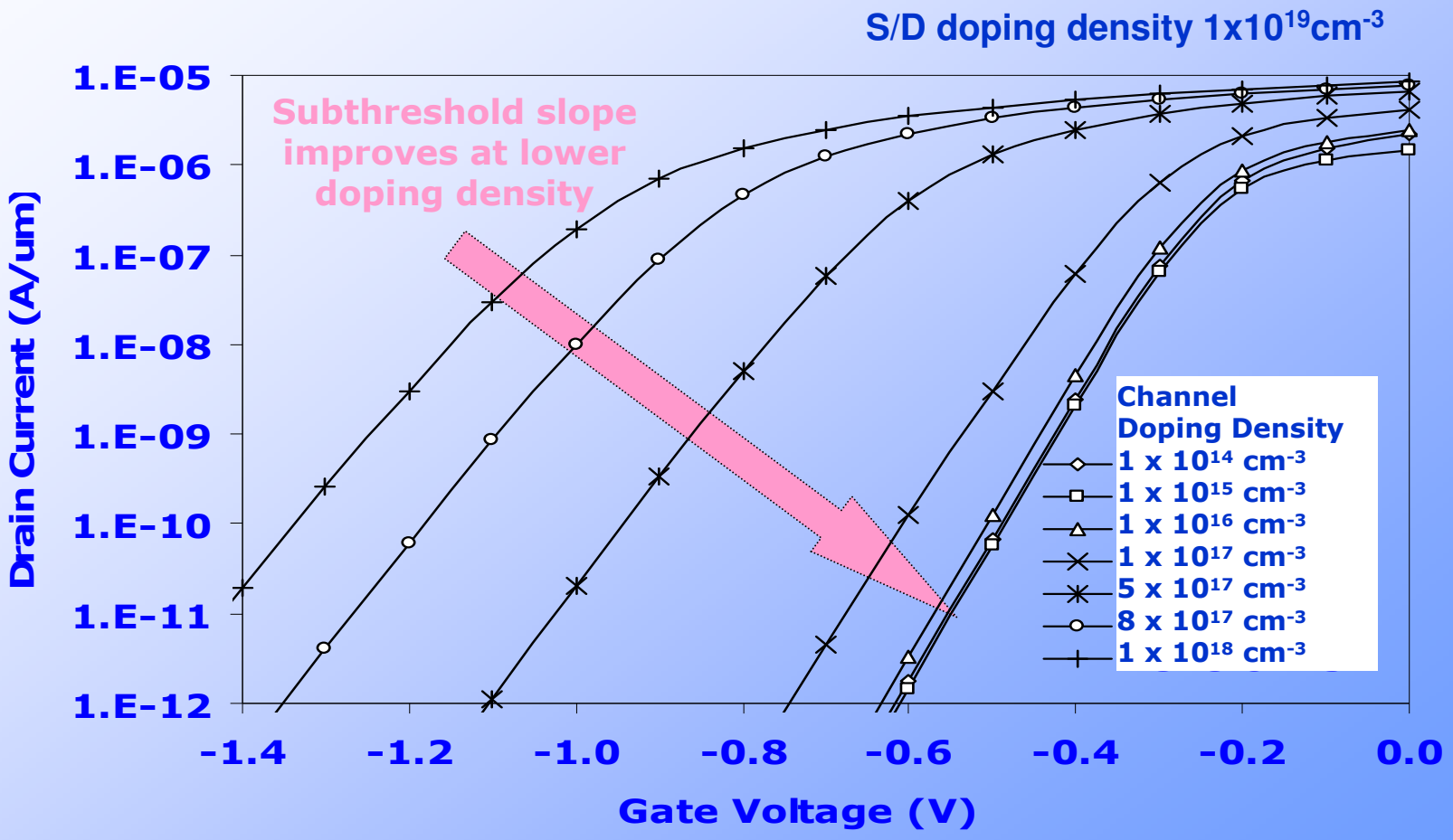
3-D Simulation Results

Influence of Channel Doping Concentration



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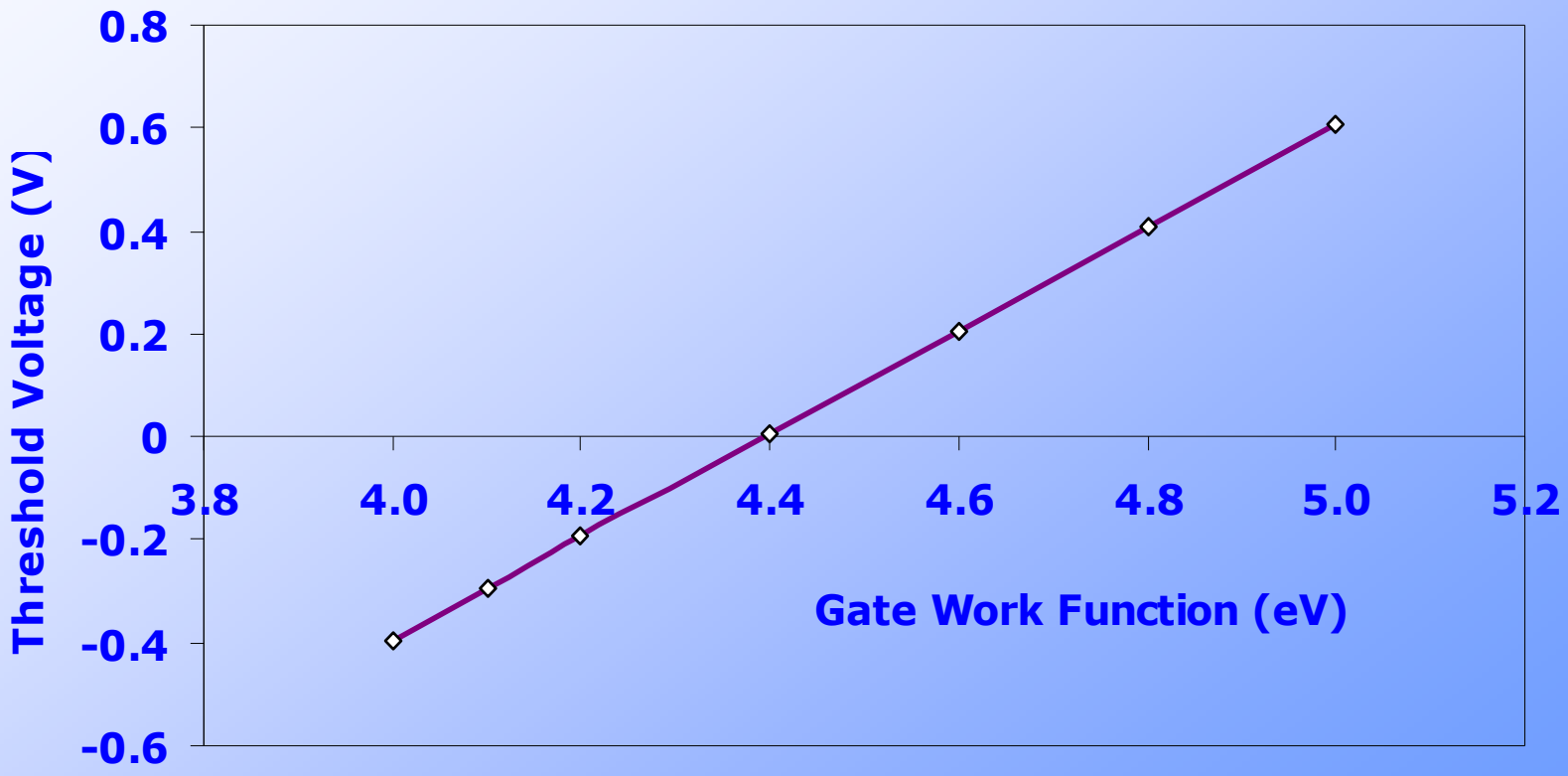
3-D Simulation Results

Threshold voltage variation by variation in gate work function



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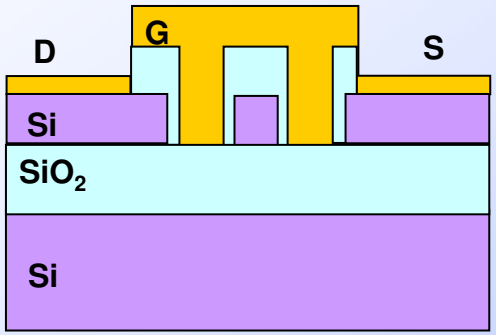
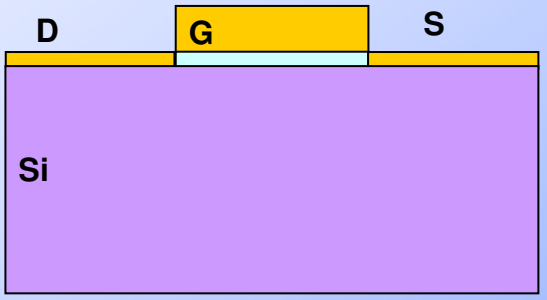
3-D Simulation Results

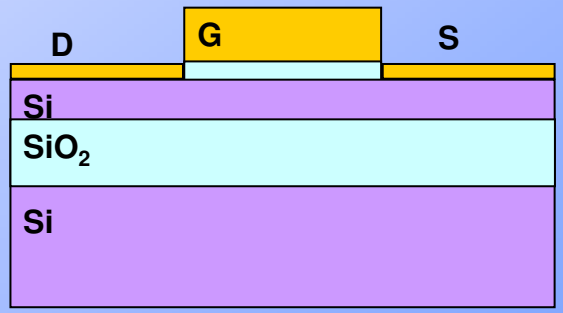
Comparison Study between SGFET, bulk MOSFET, SOI MOSFET



SGFET



Bulk MOSFET



SOI MOSFET

General dimensions for all devices:

S-D distance 60nm/600nm

gate oxide thickness 5nm

channel doping density $1x10^{14}$ cm^{-3}

channel width 50nm

S/D doping density $1x10^{17}cm^{-3}$

SOI wafer 40nm Si channel thickness

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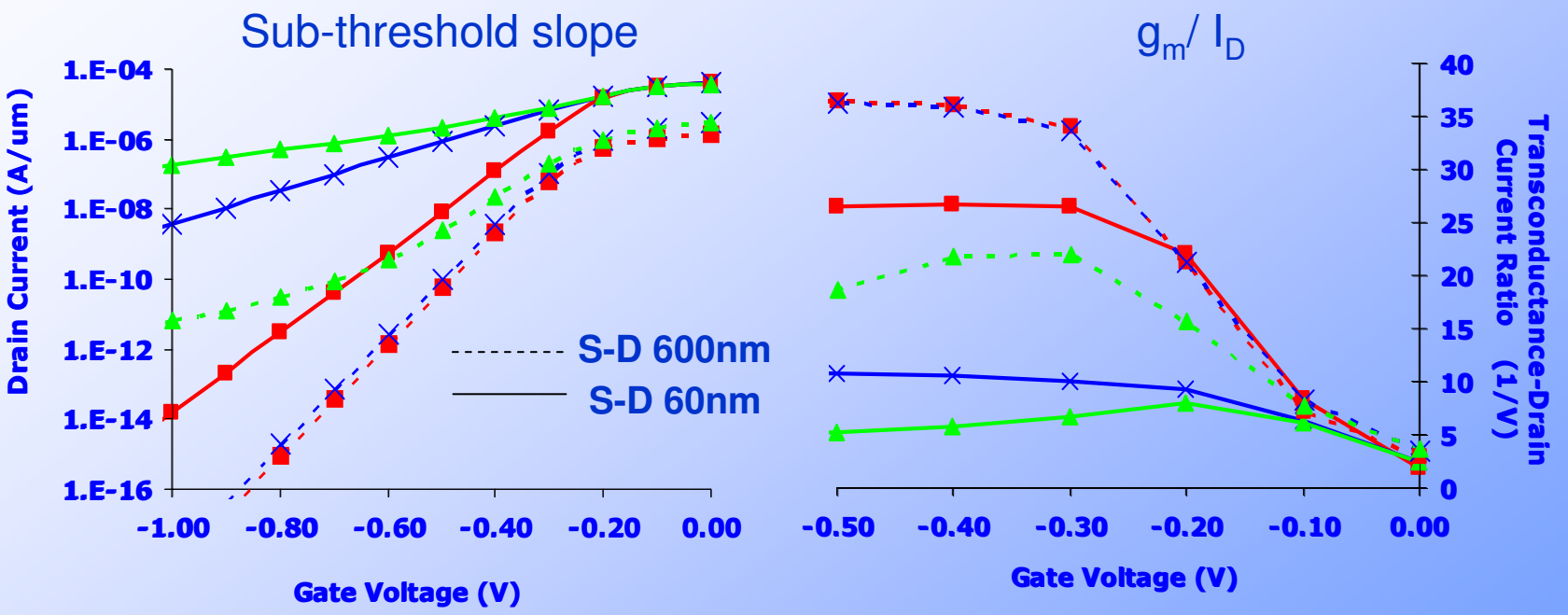
3-D Simulation Results

Comparison Study between SGFET, bulk MOSFET, SOI MOSFET



SGFET

Good Sub-threshold Characteristic

High Transconductance Efficiency

- SGFET
- Bulk MOSFET
- X SOI MOSFET

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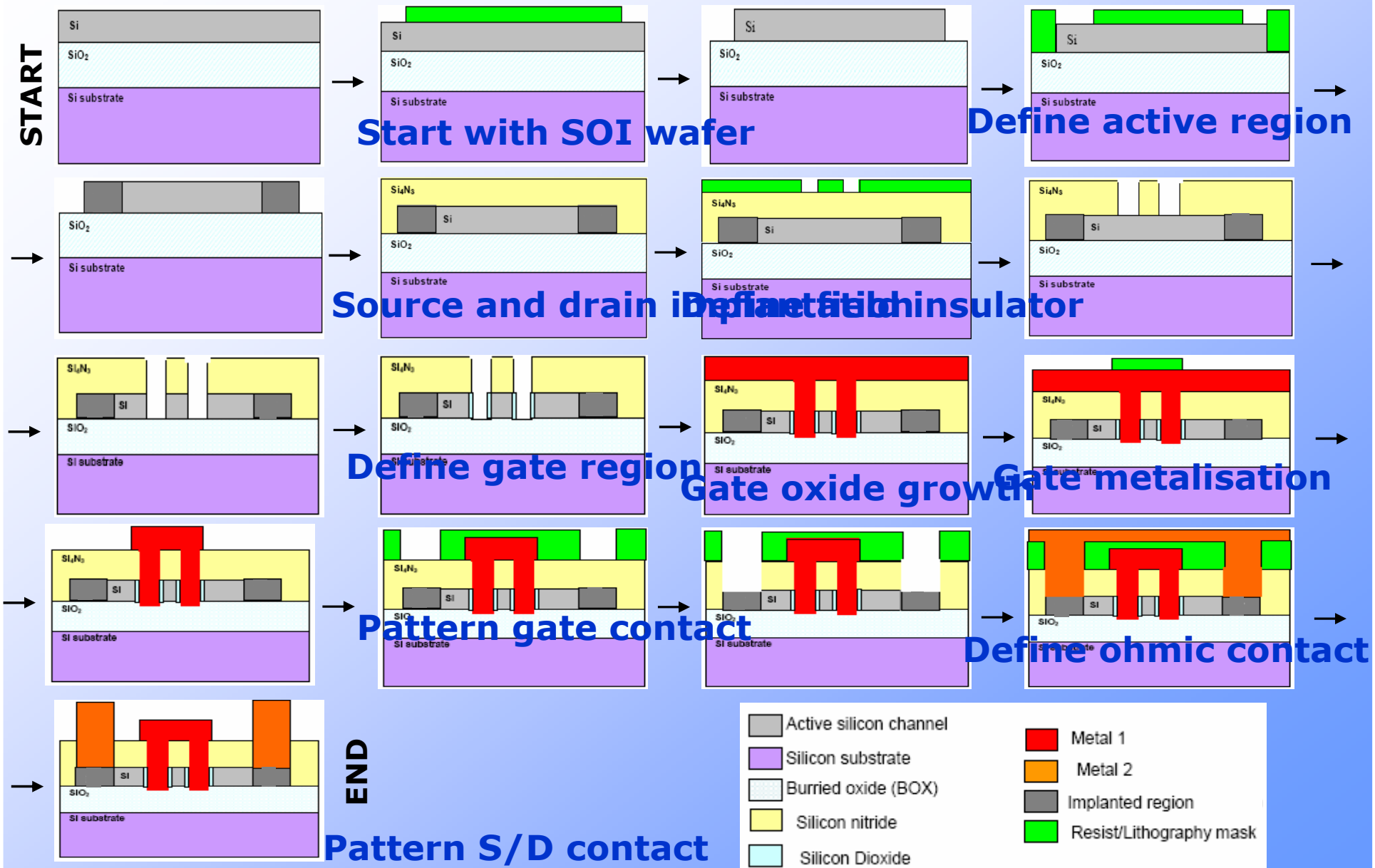
Planned Fabrication Steps



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Conclusions

- 2nd row gate fingers act as screen-grid to reduce DIBL effect.
- SGFET works well with channel at low doping levels - without loss in carrier mobility.
- Reduction in device length does not drastically degrade device's performances compared to SOI or bulk MOSFET.
- Therefore SGFET offers the possibility of downscaling without degrading the output characteristic.

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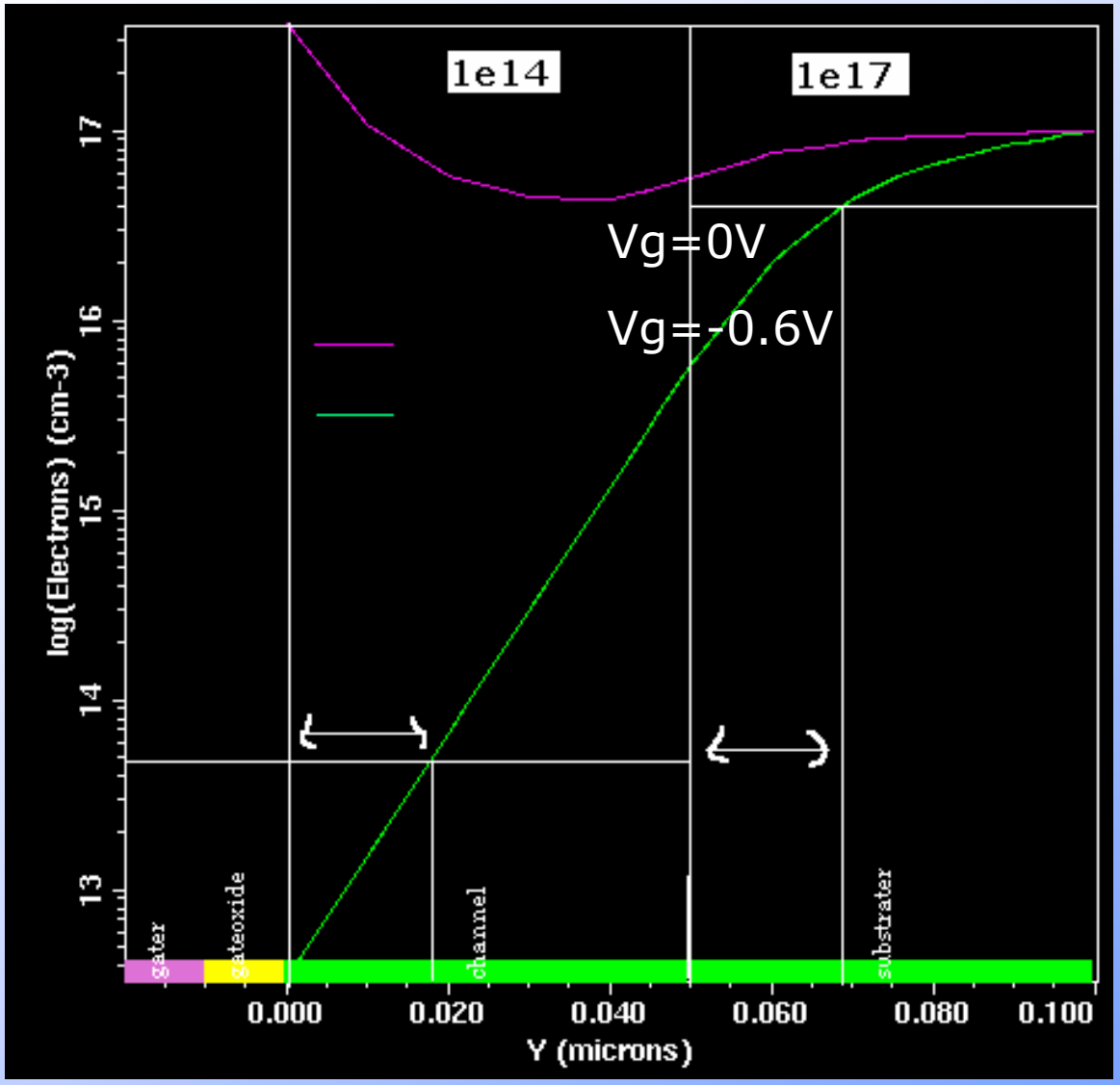
Electron concentration plot for n^+n^- junction



Depletion Region
(½ of background doping)