3-D Modelling of the Novel Nanoscale Screen-Grid Field Effect Transistor (SGFET)

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Outline

- Objectives/Motivation
- Proposed SGFET Structure
- Simulation Results
- Proposed Fabrication Steps
- Conclusions
Objectives

To propose a novel 3-dimensional FET structure which overcomes the fundamental limitations of sub-micron FETs for future device scaling.

Current Requirements:

• High Operation Speed
• High packing density
• Low power consumption

Short channel effects:

• High electric field
• High leakage current
• High power consumption

Source: Logic Technology Development, Intel Corporation
SGFET: a novel approach to 3-D gating

Proposed Structure

**3-D view cross section**

- Source contact
- Drain contact
- Gate contact
- Gate Electrode
- Gate Electrodes
- Deposited Insulator Layer
- Si Device Layer
- Buried SiO$_2$ Layer
- Si Substrate Layer
- Si Channel
- Thermal SiO$_2$
- Contact

**Side view cross section**

**Top view cross section**

- Buried oxide
- Thermal oxide
- Silicon channel
- Current flow

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Why SGFET?

SG – ‘Screen Grid’ principle from vacuum tube technology

**Triode**

**Tetrode**

**SGFET:** Screen-Grid refers to the extra row of gate cylinders that we add in to screen the effect of drain-induced barrier lowering, DIBL
Gating Effect:

- Conventional MOSFET gating
- SGFET gating

Proposed Structure
3-D Simulations

**SGFET: TAURUS™ Simulation**

**Simulation Structure**

**Top cross-sectional view**

**3-D view**

**General dimensions:**

Si channel thickness = 40nm . buried oxide thickness = 460nm . field oxide thickness = 300nm

$L_g = 130$nm . $L_{inter} = 300$nm . S-D distance = 600nm . gate diameter = 100nm

Gate oxide thickness = 10nm . source and drain regions doping density = $1 \times 10^{17}$cm$^{-3}$ (n-type)
### 3-D Simulation Results

#### Influence of Channel Width

1) Linear operation region $V_{DS} = 0.05V$

<table>
<thead>
<tr>
<th></th>
<th>$I_{DS} @ V_{GS} = 0V$ (A)</th>
<th>$I_{DS}$ (A/µm)</th>
<th>$V_T$ (V)</th>
<th>$S$ (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single W1</td>
<td>$1.92 \times 10^{-7}$</td>
<td>$1.48 \times 10^{-6}$</td>
<td>$-0.29424$</td>
<td>62.57</td>
</tr>
<tr>
<td>Double W2</td>
<td>$3.88 \times 10^{-7}$</td>
<td>$1.49 \times 10^{-6}$</td>
<td>$-0.29346$</td>
<td>62.55</td>
</tr>
<tr>
<td>Triple W3</td>
<td>$5.81 \times 10^{-7}$</td>
<td>$1.49 \times 10^{-6}$</td>
<td>$-0.29345$</td>
<td>62.51</td>
</tr>
</tbody>
</table>

2) Saturated operation region $V_{DS} = 3.00V$

<table>
<thead>
<tr>
<th></th>
<th>$I_{DS} @ V_{GS} = 0V$ (A)</th>
<th>$I_{DS}$ (A/µm)</th>
<th>$V_T$ (V)</th>
<th>$S$ (mV/decade)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single W1</td>
<td>$9.59 \times 10^{-7}$</td>
<td>$7.37 \times 10^{-6}$</td>
<td>$-0.23049$</td>
<td>61.88</td>
</tr>
<tr>
<td>Double W2</td>
<td>$1.93 \times 10^{-6}$</td>
<td>$7.42 \times 10^{-6}$</td>
<td>$-0.22962$</td>
<td>61.88</td>
</tr>
<tr>
<td>Triple W3</td>
<td>$2.89 \times 10^{-6}$</td>
<td>$7.41 \times 10^{-6}$</td>
<td>$-0.22962$</td>
<td>61.81</td>
</tr>
</tbody>
</table>
3-D Simulation Results

Influence of Geometrical Structure (Number of Rows/Arrangement)

- 1 row
- 1 row (source)
- 1 row (drain)
- 2 rows

Drain Voltage (V) vs. Drain Current (A/um)

Diagram showing the relationship between drain voltage and drain current for different configurations of rows and arrangements.
### 3-D Simulation Results

**Influence on DIBL reduction (Threshold Voltage Shift)**

<table>
<thead>
<tr>
<th>S-D distance (nm)</th>
<th>80</th>
<th>70</th>
<th>60</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of rows</td>
<td>2 rows</td>
<td>1 row</td>
<td>2 rows</td>
</tr>
<tr>
<td>( \frac{\Delta V_T}{\Delta V_D} ) (mV/V)</td>
<td>-66.3</td>
<td>-142.7</td>
<td>-74.4</td>
</tr>
</tbody>
</table>

Row 2 acts as screen grid to DIBL effect!

“SGFET”
Simulated depletion region $V_D=0.05\text{V}$, $V_G=0\text{V}$ to $-1\text{V}$
Simulated depletion region $V_D=0.05V$, $V_G=0V$ to $-1V$
3-D Simulation Results

Simulated electron concentrations

1. $V_G=0V \ V_D=0.05V$
2. $V_G=-0.3V \ V_D=0.05V$
3. $V_G=-0.5V \ V_D=0.05V$
4. $V_G=-1.0V \ V_D=0.05V$
Influence of Channel Doping Concentration

Subthreshold slope improves at lower doping density.

S/D doping density $1 \times 10^{19} \text{cm}^{-3}$
Threshold voltage variation by variation in gate work function
3-D Simulation Results

Comparison Study between SGFET, bulk MOSFET, SOI MOSFET

SGFET

Bulk MOSFET

SOI MOSFET

General dimensions for all devices:
- S-D distance 60nm/600nm
- gate oxide thickness 5nm
- channel doping density $1 \times 10^{14} \text{ cm}^{-3}$
- channel width 50nm
- S/D doping density $1 \times 10^{17} \text{ cm}^{-3}$
- SOI wafer 40nm Si channel thickness
Comparison Study between SGFET, bulk MOSFET, SOI MOSFET

Sub-threshold slope

\( g_m/ I_D \)

Transconductance-Drain Current Ratio (A/V)

SGFET
Good Sub-threshold Characteristic
High Transconductance Efficiency

SGFET
Bulk MOSFET
SOI MOSFET
Planned Fabrication Steps

1. Start with SOI wafer
2. Define active region
3. Source and drain implantation
4. Define field insulator
5. Define gate region
6. Gate oxide growth
7. Gate metalisation
8. Pattern gate contact
9. Define ohmic contact
10. Pattern S/D contact

Legend:
- Active silicon channel
- Silicon substrate
- Buried oxide (BOX)
- Silicon nitride
- Silicon Oxide
- Metal 1
- Metal 2
- Implanted region
- Resist/Lithography mask
Conclusions

- 2nd row gate fingers act as screen-grid to reduce DIBL effect.

- SGFET works well with channel at low doping levels - without loss in carrier mobility.

- Reduction in device length does not drastically degrade device’s performances compared to SOI or bulk MOSFET.

- Therefore SGFET offers the possibility of downscaling without degrading the output characteristic.
Electron concentration plot for n⁺n⁻ junction

Depletion Region
(½ of background doping)