Analog performance of the Screen Grid Field Effect Transistor

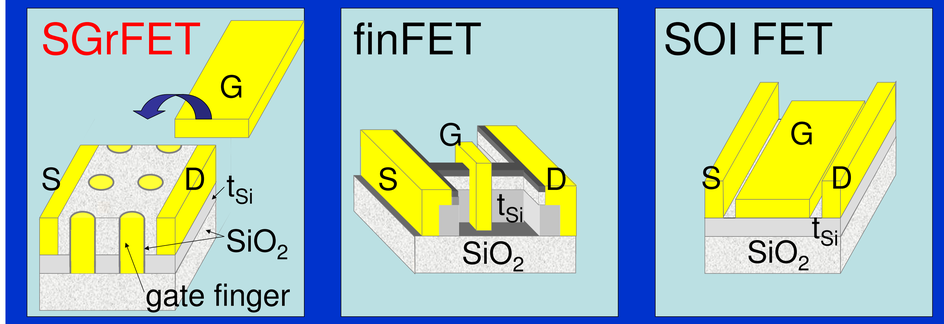
P.W. Ding, K. Fobelets, and J.E. Velazquez-Perez

Imperial College London

University of Salamanca

EPSRC

Novel gating geometry/ 3D view

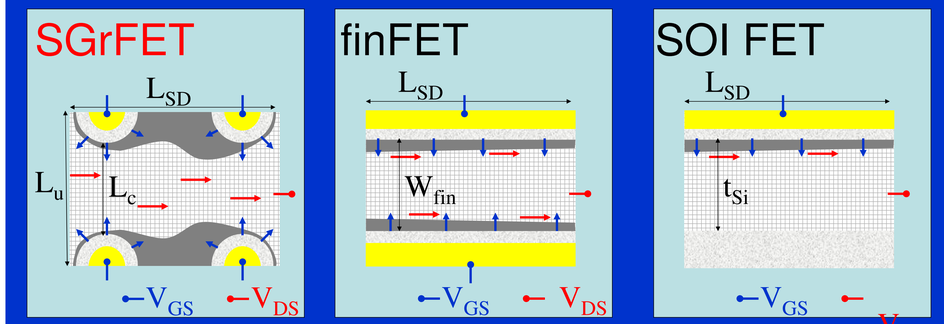


In-plane transport
Large SD contact

⊥-plane transport
Small SD contact

In-plane transport
Large SD contact

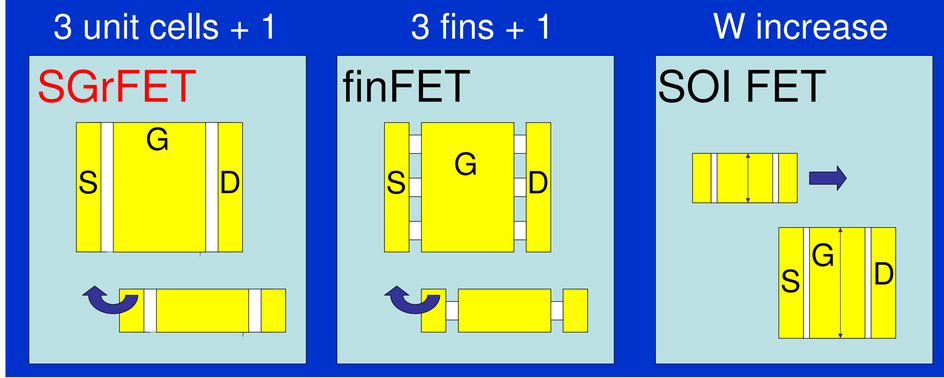
Basic transport principle/ 2D cross section



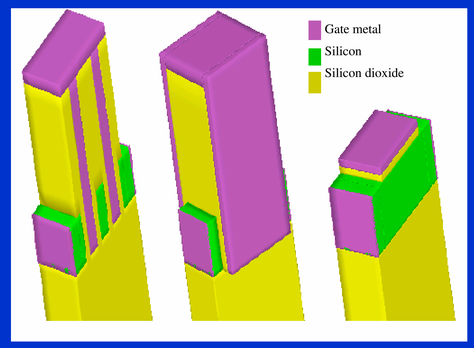
1 channel
Depletion control
High carrier μ
DIBL control

2 channels
Inversion
Low carrier μ
DIBL control

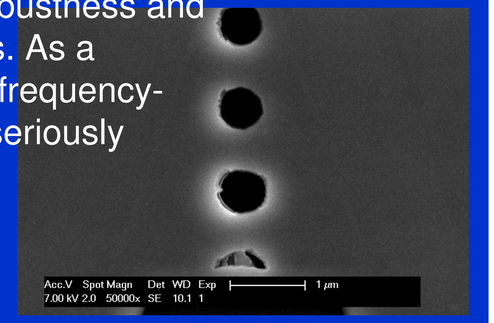
1 channel
Inversion
Low carrier μ



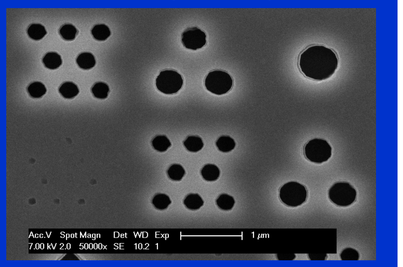
3D TCAD performance Taurus (Synopsys)



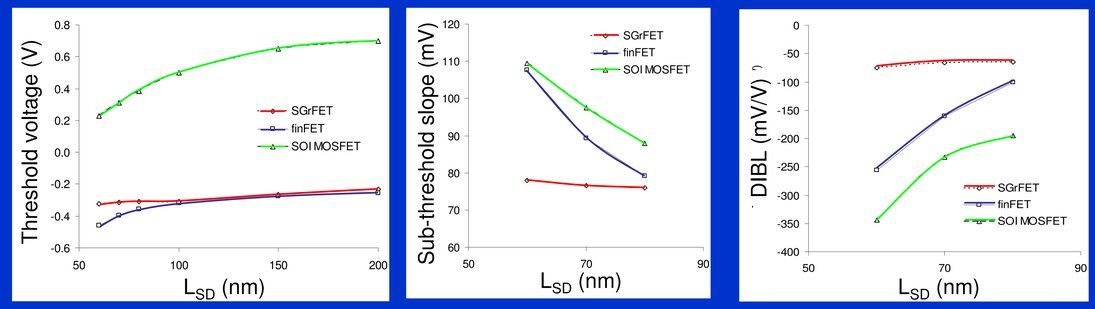
The SGrFET is a novel FET structure in SOI with a gate that is formed by cylindrical fingers perpendicular into the channel region. This FET shows excellent downscaling robustness and low power characteristics. As a consequence the cut-off frequency-voltage gain trade off is seriously relaxed in the SGrFET.



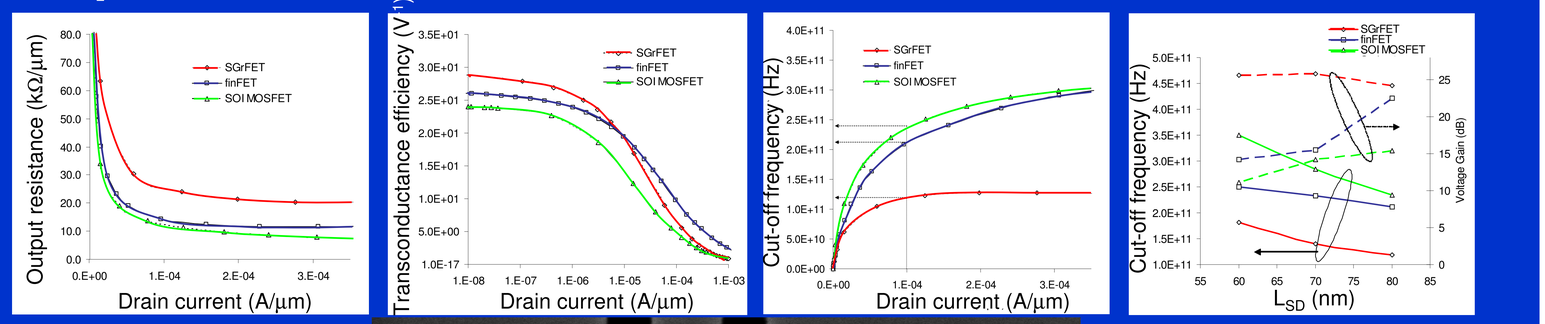
Fabrication/SEM by Mir Enterprises



Downscaling robustness



RF performance



t_{ox} = 5 nm
L_{SD} = 80 nm
L_U = 30 nm
t_{Si} = 40 nm

	g_m (μS/μm)	g_m/I_{DS} (V^{-1})	r_o (kΩ.μm)	g_m/g_{ds} (dB)	f_T (GHz)
SGrFET	650	29.4	25.0	24.2	118
finFET	960	26.5	14.0	22.5	210
SOI MOSFET	470	24.0	12.0	15.4	240

Performance at 10^{-4} A/μm
SOI MOSFET highest f_T
SGrFET highest $A_V = g_m/g_{ds}$