Digital Electronics II

Mike Brookes

Please pick up: Notes from the front desk

1. What does Digital mean ?

2. Where is it used ?

3. Why is it used ?

4. What are the important features of a digital system ?

Lecture List

- Notation, Cause and Effect
  - 1: Notation, Cause and Effect, Flipflops, Counters
- Interfacing Digital Systems
  - 2: Synchronous bit-serial Interfacing
  - 3. Asynchronous bit-serial interfacing
  - 4,5: Microprocessor-to-Memory Interface
- Synchronous State Machines
  - 6: Shift Register control and sequencing
  - 7. Data Decoding with a counter
  - 8. Synchronous state machine analysis
  - 9. Synchronous state machine design
- Digital ↔ Analog Conversion
  - 10: Digital-to-Analog conversion
  - 11. Analog-to-Digital Conversion: Flash and dither
  - 12. Analog-to-Digital Conversion: Successive approximation
- Addition Circuits
  - 13: Adders and propagation delays
  - 14. Fast Adders: bit inversion & carry lookahead
  - 15. Fast adders: Carry skip and carry save

Lecture Notes

Very concise - ensure you understand each sentence.

Book

Tocci, Widmer & Moss, “Digital Systems: Principles & Applications”, Pearson, 11th ed, 2010.
ISBN 0130387932

Covers most of the course though not in the same order. I do not follow any book closely.

Problem Sheets

- Problems graded:
  - everyone should do A, B and C
  - D and E are harder
- Solutions are included
- Problems Class: Room 509:
  - Fri 16:00 (week 3) and Tue 3:00 (weeks 4 – 11)
- Tutorial questions

URL

http://www.ee.ic.ac.uk/hp/staff/dmb/courses/dig2/dig2.htm

Discussion Group

http://learn.imperial.ac.uk

Office Hours

Room 812: Mon 10:00-11:00 and Fri 15:00-16:00

Lecture 1

Notation, Cause and Effect

Objectives

- Introduce the IEC standard notation for logic symbols
- Emphasize the notion of cause and effect in digital circuits
- Remind you what a flipflop does
- Look at the propagation delays of a ripple counter and a synchronous counter

Notation

Logic Levels

A logic 1 (or high) is always the most positive of the two voltage levels.

e.g. CMOS: 0 & 5V, ECL –1.75 & –0.9V

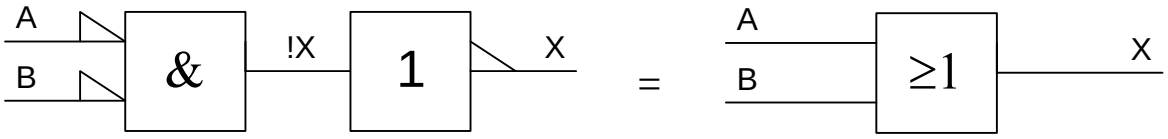
Gates

The label indicates how many of the inputs must be high to make the output high:

&	AND gate: all inputs high
≥1	OR gate: one or more inputs high
=1	Exclusive-OR: exactly one input high
2n	Even Parity: even number of inputs high

Inversion Triangles

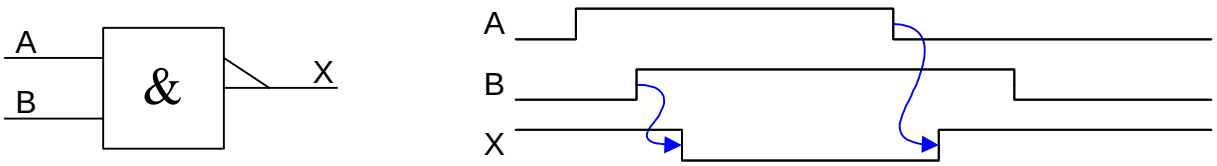
We can invert signals on the way in or on the way out:



$\overline{X}$ or !X denotes the inverse of X.

0

Cause & Effect



Input B going high causes X to go low

Input A going low causes X to go high

Propagation Delay:

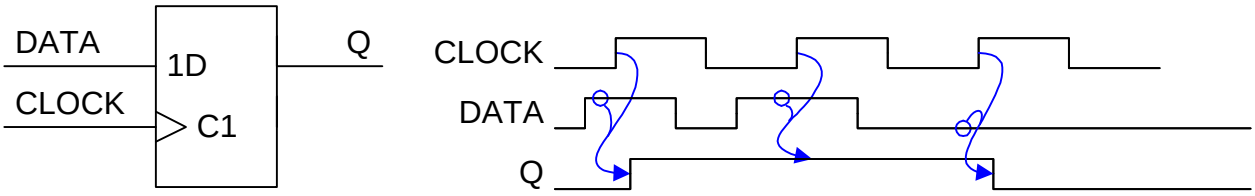
The time delay between a cause (an input changing) and its effect (an output changing).

Example: 74AC00: Advanced CMOS 2-input NAND gate

	min	typ	max	
A↑ to X↓ (t_{PHL})	1.5	4.5	6.5	ns
A↓ to X↑ (t_{PLH})	1.5	6.0	8.0	ns

t_{PHL} and t_{PLH} refer to the direction that the output changes: high-to-low or low-to-high.

D-Flipflop



Notation:

> input effect happens on the rising edge

C1 C ⇒ Clock input, 1 ⇒ This input *is* input number 1.

1D D ⇒ Data input,
1 ⇒ This input *is controlled by* input number 1.

The meaning of a number depends on its position:

A number *after* a letter is used to identify a particular input.
A number *before* a letter means that this input is controlled by one of the other inputs.

Cause and Effect:

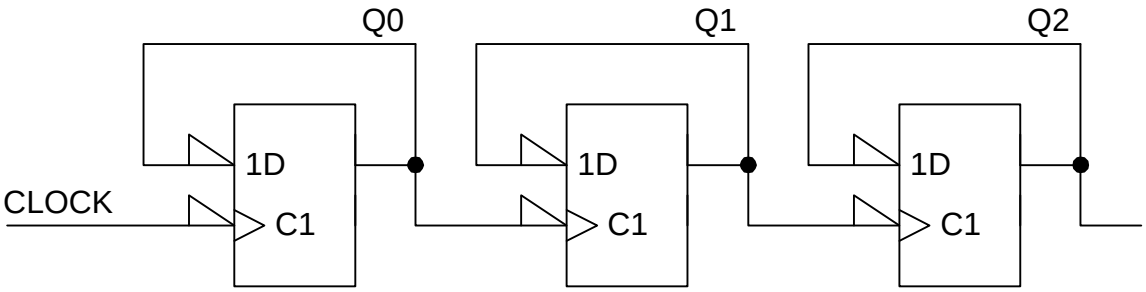
– CLOCK↑ causes Q to change after a short delay. This is the *only* time Q ever changes.

– The value of D *just before* CLOCK↑ is the new Q.

– Propagation delay CLOCK↑ to Q is typically 6 ns.

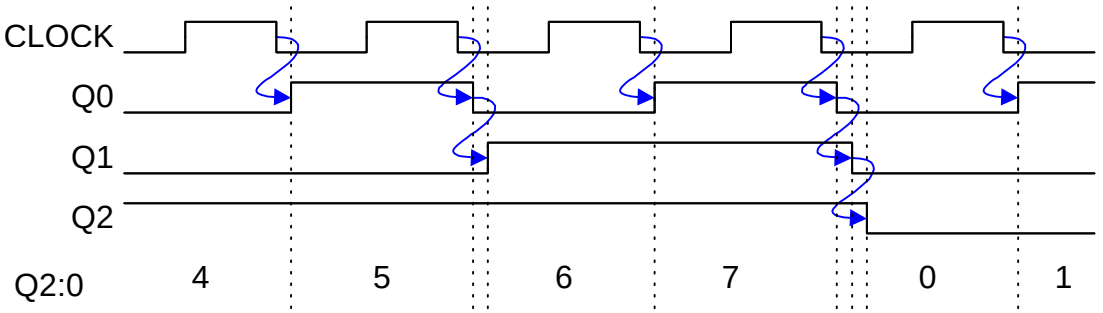
– Propagation delay DATA to Q **does not make sense** since DATA changing does not cause Q to change.

Ripple Counter

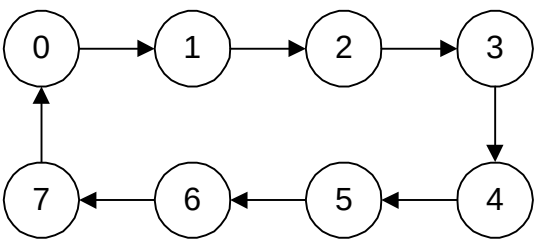


Notation:

- Notice inverters on the CLOCK and DATA inputs
- Least significant bit of a number is always labelled 0

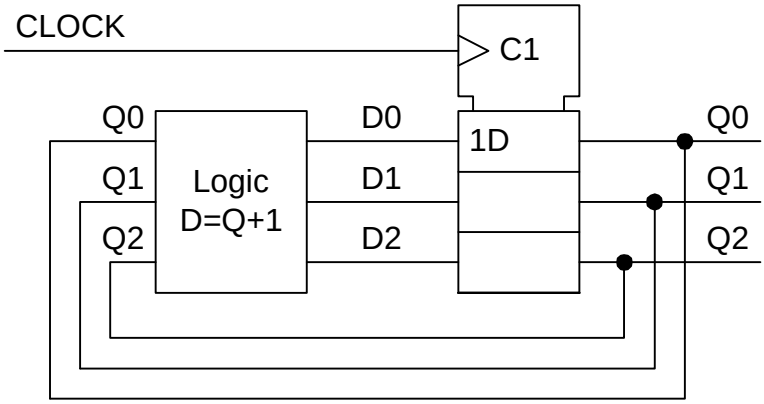


State Diagram (not including transient states):



Propagation Delay: CLOCK↓ to Q2 = 3 × 6 ns = 18 ns

Synchronous Counter

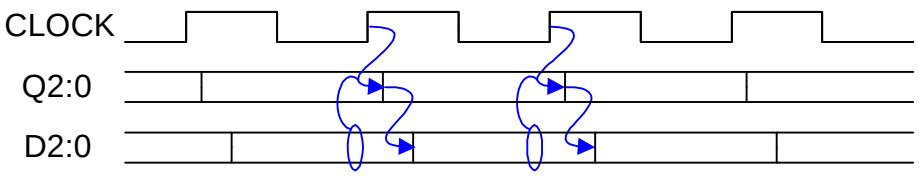


Notation:

- A *register* is a bunch of flipflops with the same CLOCK.
- The individual flipflops are rectangles stacked on top of each other. Only the top one is labelled.
- All shared signals (e.g. the CLOCK input) go to the notched *common control block* at the top of the stack.

The logic block must add 1 onto the current value of the counter, Q, to generate the next value of the counter, D. Suppose it has a propagation delay of 10 ns.

All flipflops change state within a fraction of a nanosecond.



Propagation Delays: CLOCK↑ to Qi = 6ns
CLOCK↑ to Di = 16ns

Dependency Notation

Input Labels:

Inputs are labelled with a function letter to show what effect they have on the circuit. They have this effect whenever they are high (i.e. at logic 1).

The function letter is usually followed by an identification number (which must be unique):

- C1 Clock number 1
- M7 Mode input number 7
- D Data input (no identification number)

Dependencies:

If an input is affected by one or more other signals, we list their identification numbers *in front* of the function letter:

- 3,2,5D Data input affected by input 3,2 and 5 in that order.

The identification number is used to show which of the other inputs are affected by putting it *in front* of their function letters (if any).

Device Types:

The overall function of a device is indicated at the top of its symbol. Anything unlabelled is a flipflop or register.

Function Letters for Input Signals

A	Address inputs for a memory circuit
CI,CO	Carry In and Out for an adder
C	Clock or Control input
CT=xx	Set contents of register or counter to xx
D	Data input to flipflop
EN	Enable tri-state outputs
G	"Gating" input: allows signals through when high
J,K,T	Inputs for JK and Toggle flipflops
M	Mode input: selects one of several operating modes (e.g. count up or count down)
P,Q	Input numbers for adders, multipliers etc.
R,S	Reset and Set inputs
V	Forces a signal to 1 when high
+, –	Increment or Decrement
$\leftarrow,\rightarrow$	Shift up (left) or shift down (right)

Device Types

&, $\geq$1, =1	Gates
(blank)	Latch, Flipflop or register
MUX	Multiplexer
Σ	Adder
Π	Multiplier
CTR	Counter
SRG	Shift Register
RAM	Read/Write memory

Note: These lists are for reference only. You are not expected to memorize them.

Quiz Questions

1. The voltage levels for the TTL logic family are 0.4 V and 2.8 V. Which one of these corresponds to logic 1?
2. If a gate is labelled ≥1, under what circumstances will the output be high?
3. What does the *propagation delay* of a circuit mean?
4. Why does it make no sense to talk about the propagation delay between a flipflop's DATA input and the flipflop's output?
5. A flipflop's inputs are labelled C1 and 1D respectively. Why does the 1 come after the C but before the D?
6. What is the meaning of the > sign just before the C1 in a flipflop's symbol?
7. What is the meaning of a triangle drawn where an input or output wire meets a logic symbol?
8. What is a *register*?

Answers are all in the notes.