Lecture 10

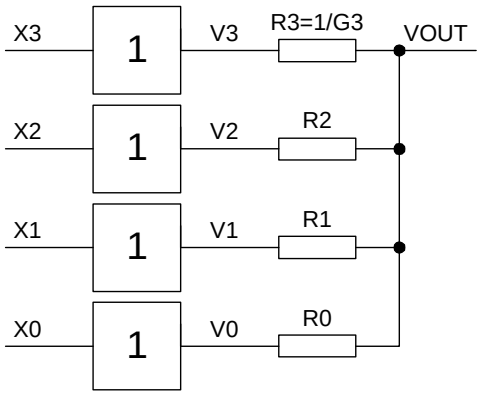
# Digital-to-Analog Conversion

Objectives

- Understand how a weighted-resister DAC can be used to convert numbers with binary or non-binary bit weightings
- Understand the meaning of the terms used to specify DAC accuracy
- Understand how an R-2R ladder can be used to convert both unsigned and signed binary numbers
- Understand the offset binary representation of negative numbers

# Digital-to-Analog Conversion

We want to convert a binary number into a voltage proportional to its value:




$$\left(V_3 - V_{OUT}\right)G_3 + \ldots + \left(V_0 - V_{OUT}\right)G_0 = 0$$

$$V_{OUT} = \frac{V_3G_3 + V_2G_2 + V_1G_1 + V_0G_0}{G_3 + G_2 + G_1 + G_0}$$

$$R_{Thevenin} = \frac{1}{G_3 + G_2 + G_1 + G_0}$$

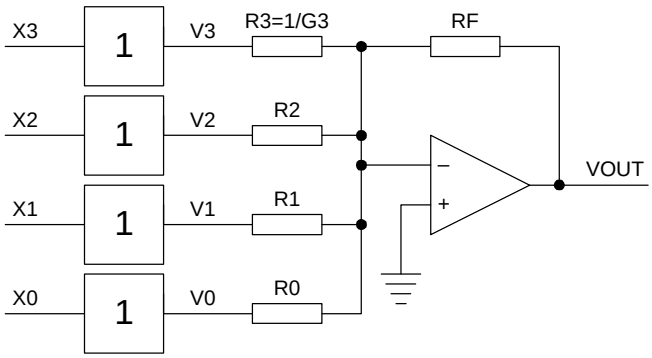
Hence $V_{OUT}$ is a weighted sum of $V_3$, …, $V_0$ with weights proportional to the conductances $G_3$, …, $G_0$.

- If X3:0 is a binary number we want conductances in the ratio 8:4:2:1.
- Very fast: gate slew rate ≈ 3 V/ns.
- We can scale the resistors to give any output impedance we want.

You do not have to use a binary weighting

- By using other conductance ratios we can choose arbitrary output voltages for up to five of the sixteen possible values of X3:0. May need additional resistors from VOUT to the power supplies.

# Output Op-Amp




$$V_{OUT} = \frac{-R_F}{R_{Thévenin}} \times V_{Thévenin} = -R_F\left(V_3G_3 + V_2G_2 + V_1G_1 + V_0G_0\right)$$

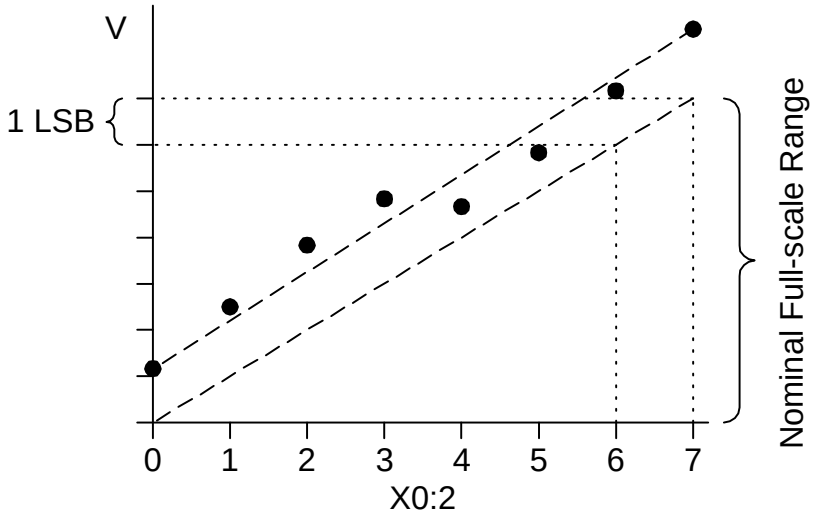
Adding an op-amp:

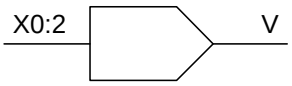
- The voltage at the junction of all the resistors is now held constant by the feedback
  - Hence current drawn from $V_3$ is independent of the other voltages $V_2$, …, $V_0$
  - Hence any gate non-linearity has no effect ⇒ more accurate.
- Lower output impedance
- Much slower: op-amp slew rate ≈ 1 V/μs.

Hard to make accurate resistors covering a wide range of values in an integrated circuit.

- Weighted-resistor DAC is no good for converters with many bits.

# DAC Jargon




Accuracy=1.8@X=3 Linearity=–0.7@X=4
Non-monotonic@3→4 Diff Linearity=–1.2@ 3→4
(all in units of LSB)

Resolution 1 LSB = $\Delta V$ when $X \rightarrow X+1$
= Full-scale range ÷ $(2^N – 1)$

Accuracy Worst deviation from nominal line

Linearity Worst deviation from line joining end points

Differential Linearity
Worst error in $\Delta V$ when $X \rightarrow X+1$
measures smoothness

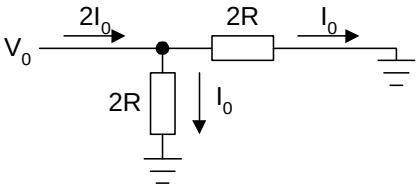
Monotonic At least $\Delta V$ always has the correct sign

Settling time Time taken to reach the final value to within some tolerance, e.g. ±½ LSB

# R-2R Ladder

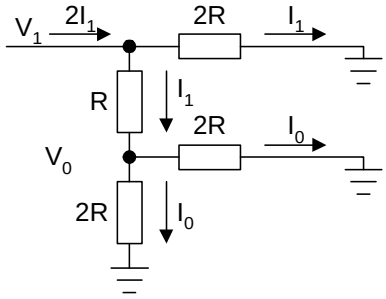
We want to generate currents $I_0$, $2I_0$, $4I_0$, …

– Two $2R$ resistors in parallel means that the $2I_0$ current will split equally.



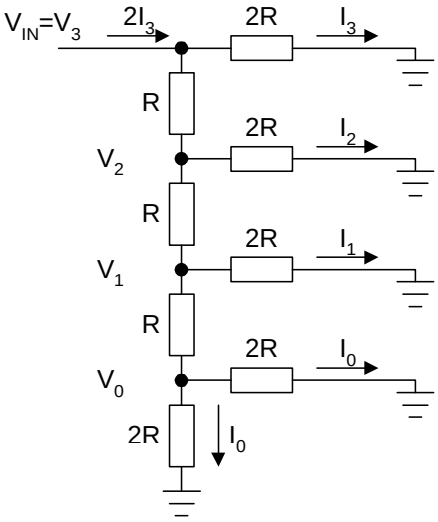

– The Thévenin resistances of the two branches at $V_1$ both equal $2R$ so the current into this node will split evenly.

We already know that the current into node $V_0$ is $2I_0$, so it follows that $I_1$=$2I_0$.

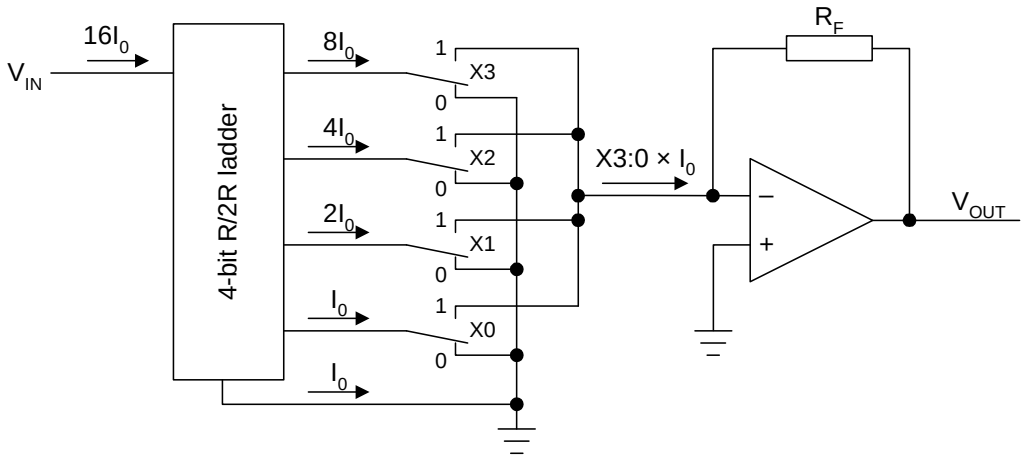



– We can repeat this process indefinitely and, using only two resistor values, can generate a whole series of currents where $I_n$=$2^nI_0$.

From the voltage drop across the horizontal resistors, we see that $V_n = 2RI_n = 2^{n+1}RI_0$ . For an $N$-bit ladder the input voltage is therefore $V_{in} = 2^NRI_0 \Rightarrow I_0$=$2^{-N}\ V_{in}/R$.



# Current-Switched DAC




– Total current into summing junction is $\mathrm{X3{:}0} \times I_0$
  Hence $V_{out} = \mathrm{X3{:}0} \times V_{\mathrm{in}} / 16R \times -R_f$

– We switch currents rather than voltages so that all nodes in the circuit remain at a constant voltage
  $\Rightarrow$ no need to charge/discharge node capacitances
  $\Rightarrow$ faster.

– Use CMOS transmission gates as switches: adjust ladder resistors to account for switch resistance.
  - Each 2-way switch needs four transistors

– As required by R/2R ladder, all the switch output terminals are at 0 V.
  - ladder outputs are always connected either to ground or to a virtual earth.

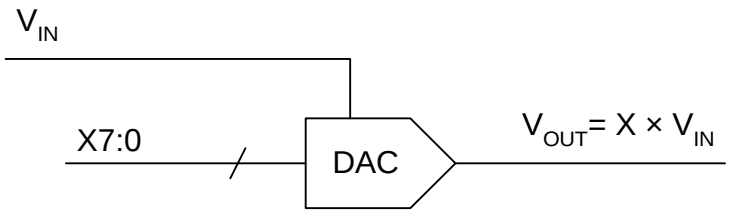
# Digital Attenuator

The output of the DAC is proportional to the *product* of an analog voltage ($V_{in}$) and a digital number (X3:0).

$$V_{out} = \text{X3:0} \times V_{\text{in}} /16R \times -R_f$$

It is called a *multiplying* DAC.

Can be used as a digital attenuator:




Here the digital number X7:0 controls the gain of the circuit.

# Bipolar DAC

A bipolar DAC is one that can give out both positive and negative voltages according to the sign of its input. There are two aspects of the circuit that we need to change:

## Number Representation

Normally we represent numbers using *2's complement* notation (because we can then use the same addition/subtraction circuits).

For converters it is more convenient to use *offset-binary* notation.

## Positive and Negative Currents

We need to alter our R-2R ladder circuit so that we can get an output current that can be positive or negative according to the sign of the input number.

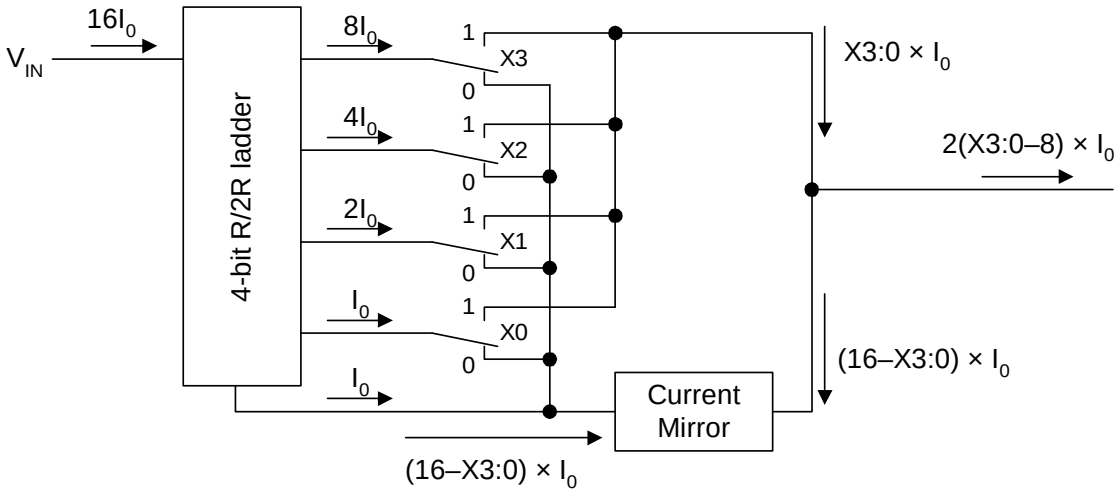
To do this, we will use a *current mirror*.

# Signed Numbers

| Value (v) | 2's complement (y) | Offset Binary (x) | (u=v+8) |
|---|---|---|---|
| –8 | 1000 | 0000 | 0 |
| –7 | 1001 | 0001 | 1 |
| –6 | 1010 | 0010 | 2 |
| –5 | 1011 | 0011 | 3 |
| ... | ... | ... | |
| –1 | 1111 | 0111 | 7 |
| 0 | 0000 | 1000 | 8 |
| 1 | 0001 | 1001 | 9 |
| ... | ... | ... | |
| 6 | 0110 | 1110 | 14 |
| 7 | 0111 | 1111 | 15 |

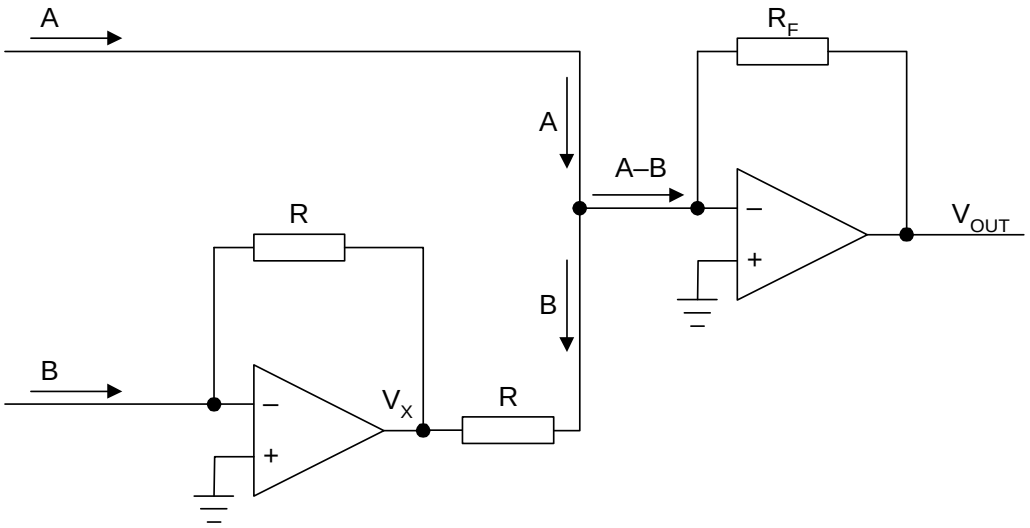
- Obtain offset binary from 2's complement by inverting the MSB
- 2's complement: $v = -8y_3+4y_2+2y_1+y_0$
- Unsigned X3:0 $u = +8x_3+4x_2+2x_1+x_0$
- Offset Binary: $v = +8x_3+4x_2+2x_1+x_0-8 = u-8$

# Signed number DAC




- Collect up all the unused currents from the R-2R ladder:
  - Total current into the ladder = $16I_0$
  - Hence total current out of the ladder = $16I_0$
  - Hence unused currents add up to $(16–\mathrm{X3{:}0})I_0$
- Send unused currents into a current mirror to reverse direction
- Add to original current to give $2(\mathrm{X3{:}0}–8)I_0$.
- If Y3:0 is a signed 2's complement number, $v$, we set {X3, X2, X1, X0} to {!Y3, Y2, Y1, Y0} which gives $v = u – 8$ where $u$ is X3:0 as an unsigned number.
- Output current is now $2\,y\,I_0$
- To invert Y3, we can just reverse the switch contacts.

# Current Mirror




The lower op-amp acts as a current mirror:

- Input current $B$ all flows through the feedback resistor.
- Hence $V_X = -BR$ since –ve input is a virtual earth.
- Hence second resistor has a voltage of $BR$ across it since –ve input of 2nd op-amp is also a virtual earth.
- Hence current through second resistor is $B$

Thus $V_{OUT} = -(A - B)\, R_F$

Alternatively, in an integrated circuit, use a long-tailed pair or Wilson current mirror.

# Quiz

- Why is a weighted-resistor DAC impractical for a 16-bit converter?
- What is a *multiplying* DAC ?
- Why is a current mirror circuit so-called?
- What is the value of the bit pattern 1001 in the following notations: (a) unsigned binary, (b) two's complement binary, (c) offset binary ?
- How do you convert a number from offset binary to two's complement notation ?

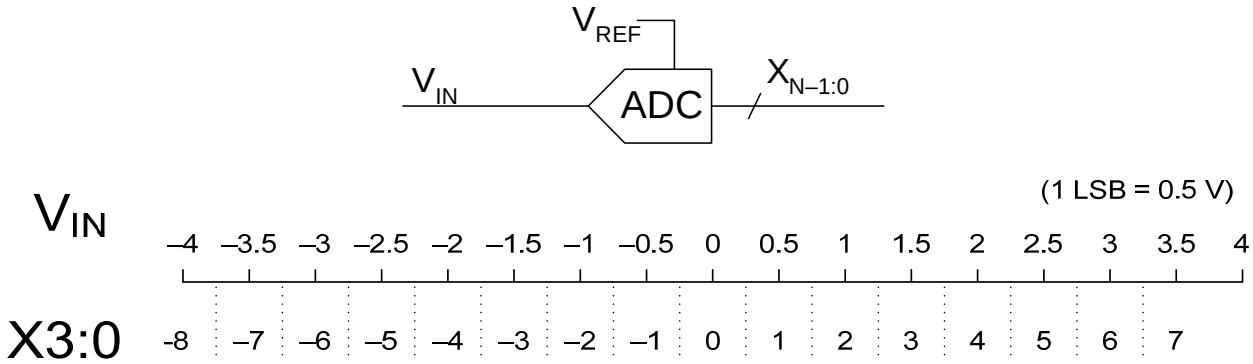
Lecture 11

# Analog-to-Digital Conversion (1)

Objectives

- Understand the relationship between the continuous input signal to an Analog-to-Digital converter and its discrete output
- Understand the source and magnitude of quantisation noise
- Understand how a flash converter works
- Understand how the use of dither can improve resolution and decorrelate the quantization noise

# Analog to Digital Conversion




Converters with ±ve input voltages are called *bipolar* converters and usually round ($V_{IN} \div$ 1LSB) to the *nearest* integer.

$$X = \text{round}\left(\frac{V_{IN}}{1\,\text{LSB}}\right)$$

Example:

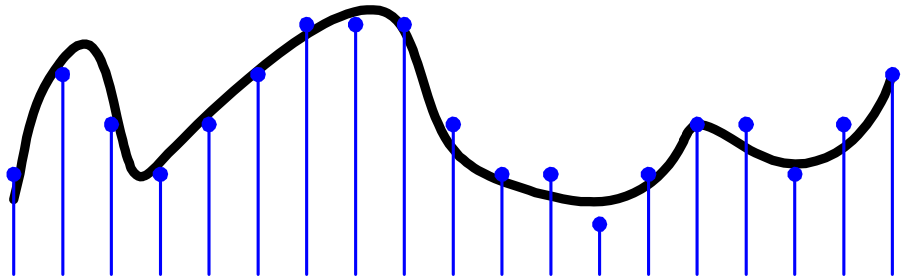
If 1 LSB = 0.5 V, then $V_{IN}$ = 2.8 V will be converted to:

$$X = \text{round}\left(\frac{2.8}{0.5}\right) = \text{round}(5.6) = 6$$

Analog to digital conversion destroys information: we convert a range of input voltages to a single digital value.

# Sampling

To process a continuous signal in a computer or other digital system, you must first sample it:



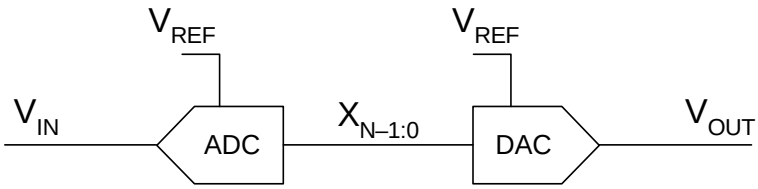
## Time Quantisation

- Samples taken (almost always) at regular intervals: sample frequency of $f_{\text{samp}}$.
- This causes *aliasing*: A frequency of $f$ is indistinguishable from frequencies $k f_{\text{samp}} \pm f$ for all integers $k$.
- No information lost if signal contains only frequencies below $\frac{1}{2} f_{\text{samp}}$ . This is the *Nyquist limit*.

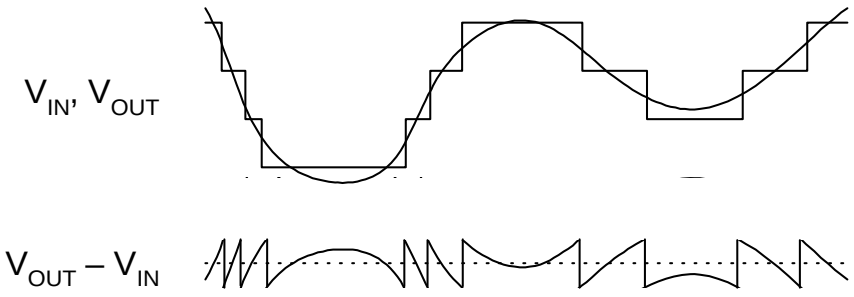
## Amplitude Quantisation

- Amplitude of each sample can only take one of a finite number of different values.
- This adds quantisation noise: an irreversible corruption of the signal.
- For low amplitude signals it also adds distortion. This can be eliminated by adding dither before sampling.

# Quantisation Noise




VOUT is restricted to discrete levels so cannot follow VIN exactly. The error, VOUT – VIN is the quantisation noise and has an amplitude of ± ½ LSB.




If all error values are equally likely, the RMS value of the quantisation noise is

$$\sqrt{\int_{-½}^{+½} x^2 dx} = \frac{1}{\sqrt{12}} = 0.3 \text{ LSB}$$

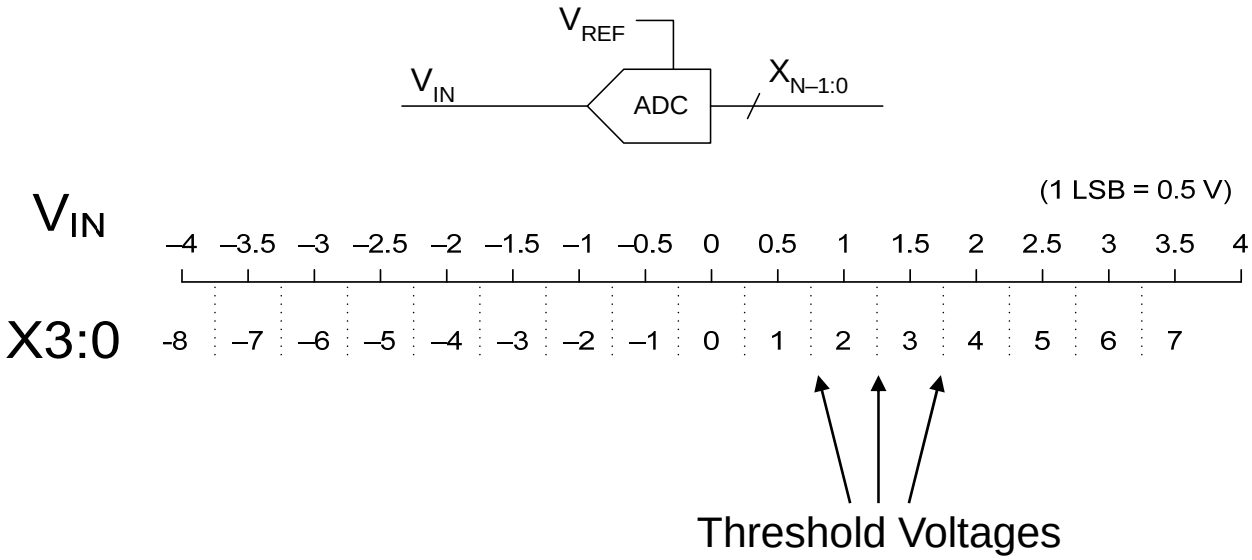
## Signal-to-Noise Ratio (SNR) for an n-bit converter

Ratio of the maximum sine wave level to the noise level:

- Maximum sine wave has an amplitude of $\pm 2^{n-1}$ which equals an RMS value of $0.71 \times 2^{n-1} = 0.35 \times 2^n$.
- SNR is:

$$20\log_{10}\left(\frac{0.35\times 2^n}{0.3}\right) = 20\log_{10}(1.2\times 2^n) = 1.8 + 6n \text{ dB}$$

# Threshold Voltages




Each value of X corresponds to a range of values of $V_{IN}$.

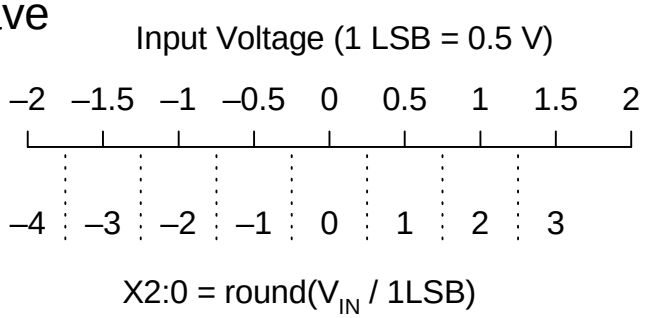
The voltage at which $V_{IN}$ switches from one value of X to the next is called a *threshold voltage*.

The task of an A/D converter is to discover which of the voltage ranges $V_{IN}$ belongs to. To do this, the converter must compare $V_{IN}$ with the threshold voltages.

The threshold voltages corresponding to X are at (X±½) LSB

# Flash A/D Converter

For an *n*-bit converter we have $2^n-1$ *threshold voltages*.

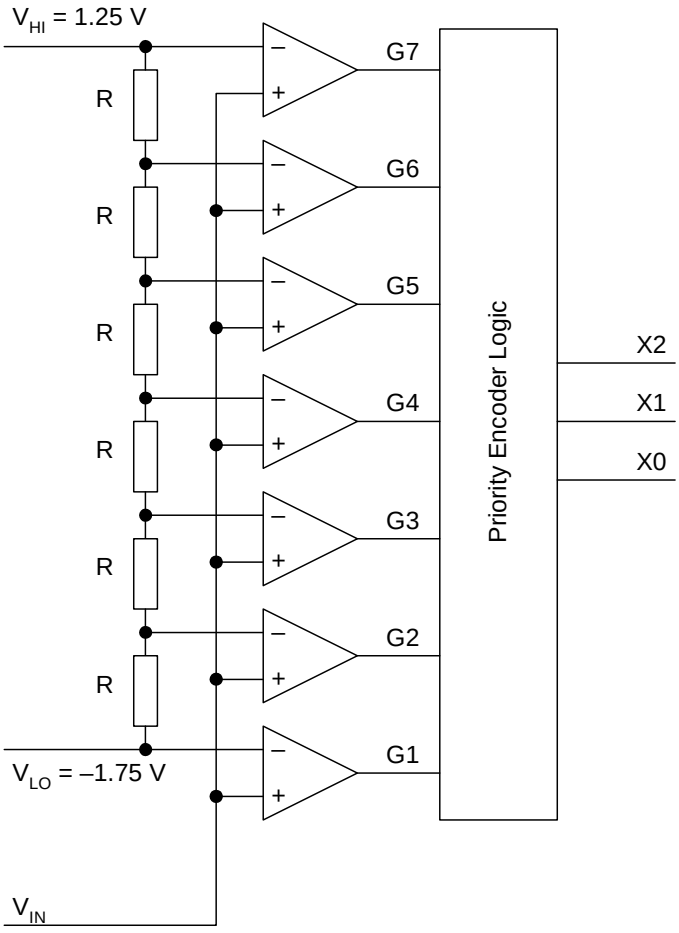



Use $2^n-1$ comparators:

Resistor chain used to generate threshold voltages.

Priority encoder logic must determine the highest Gn input that equals 1.

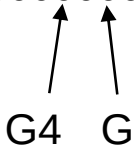
12-bit converter needs 4095 comparators on a single chip!



# Priority Encoder

G7:1 can have $2^7$ possible values but only 8 will occur:

| | G7:1 | X2:0 | Example: G2 • !G4 |
|---|---|---|---|
| $V_{IN} > 1.25$: | 1111111 | 011 =+3 | 0 |
| | 0111111 | 010 =+2 | 0 |
| | 0011111 | 001 =+1 | 0 |
| | 0001111 | 000 =+0 | 0 |
| | 0000111 | 111 =–1 | 1 |
| | 0000011 | 110 =–2 | 1 |
| | 0000001 | 101 =–3 | 0 |
| $V_{IN} < -1.75$: | 0000000 | 100 =–4 | 0 |




By inverting one comparator output and ANDing it with another one, we can generate a signal that is high for any group of consecutive X values.

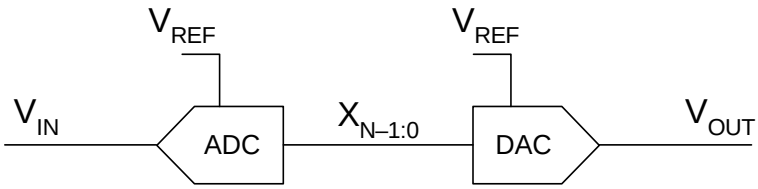
- Example: G2•!G4 is high for $-2 \leq X \leq -1$

Hence we can generate each of X2, X1 and X0 by ORing together a number of such terms:

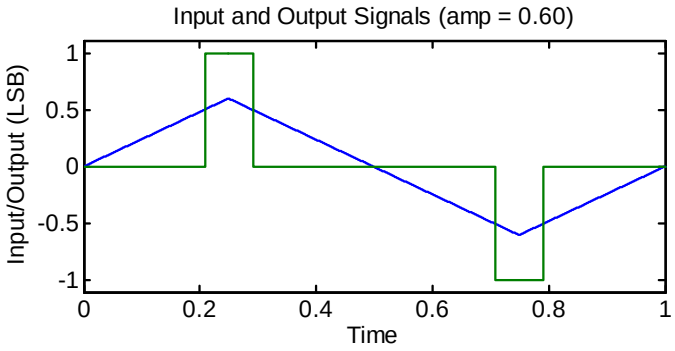
- X2 = !G4
- X1 = G6 + G2•!G4
- X0 = G7 + G5•!G6 + G3•!G4 + G1•!G2

1.11

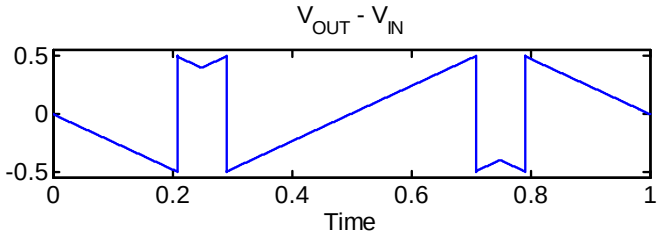
# Quantisation Distortion for Small Signals



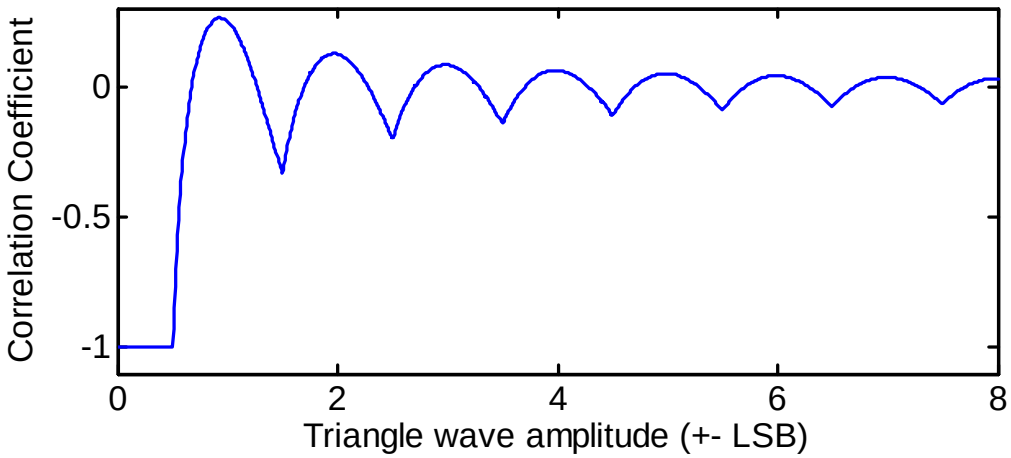

If $V_{IN}$ is a low amplitude triangle wave (±0.6 LSB):



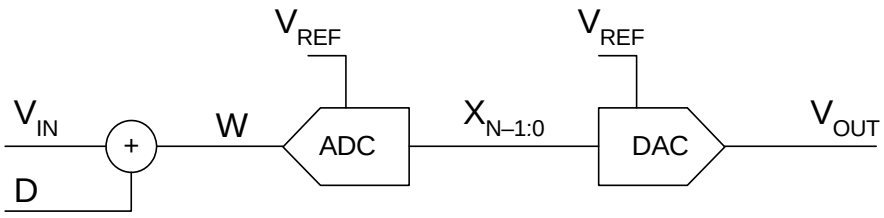

Error has strong negative correlation with $V_{IN}$ $\Rightarrow$ distortion




Correlation coefficient $\rightarrow$0 at high amplitudes:

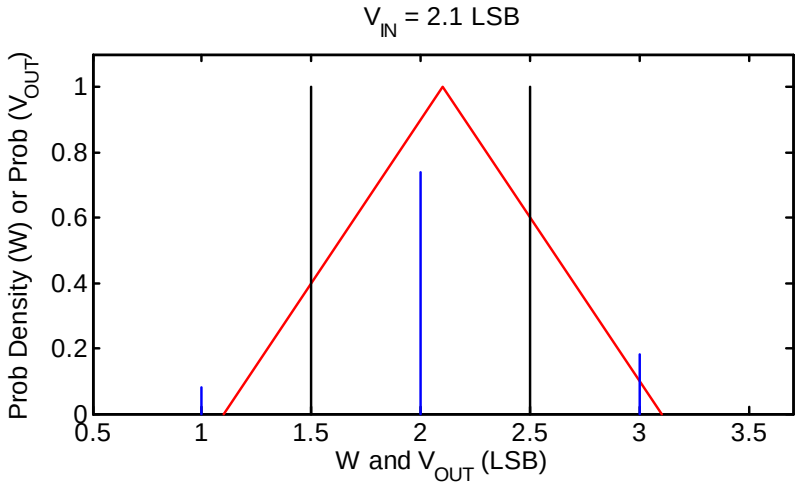


# Dither




Dither, D, is a random noise with a triangular probability density.

If $V_{IN}$ = 2.1 LSB, then W has a triangular distribution and VOUT takes three possible values:




$$V_{OUT} = \begin{cases} 1 & p(1) = p(W < 1.5) = 0.08 \\ 2 & p(3) = p(1.5 < W < 2.5) = 0.74 \\ 3 & p(3) = p(W > 2.5) = 0.18 \end{cases}$$

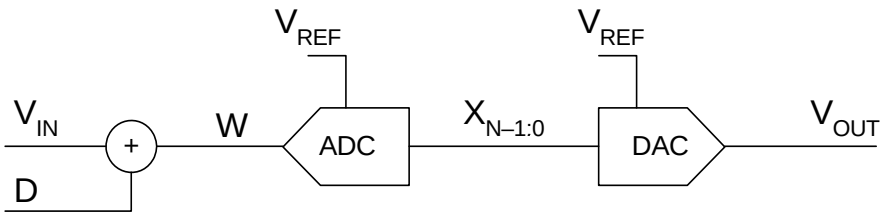
$$E(V_{OUT}) = 1 \times 0.08 + 2 \times 0.74 + 3 \times 0.18 = 2.1$$

$$Var(V_{OUT}) = 1^2 \times 0.08 + 2^2 \times 0.74 + 3^2 \times 0.18 - 2.1^2 = 0.25$$

$E(V_{OUT}) = V_{IN}$ and $Var(V_{OUT}) = 0.25$ for all values of $V_{IN}$

1.11

# Effects of Dither




## Dither should be added to a signal

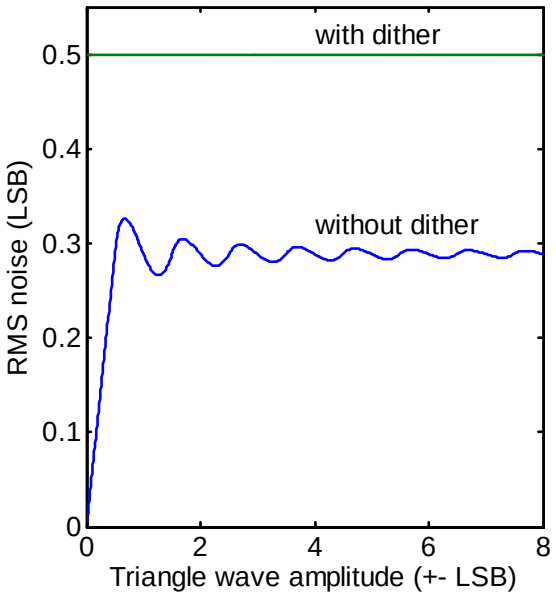
- before an ADC
- before reducing digital precision (e.g. 16 to 8 bits)
- Triangular pdf of amplitude ±1 LSB at new precision

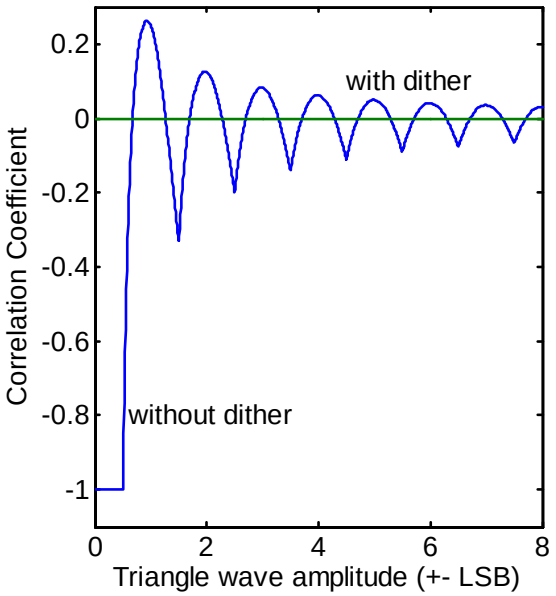
## Good consequences

- Quantisation noise level is constant independent of $V_{IN}$
- Quant noise is uncorrelated with VIN ⇒ no distortion
- Signal variations are preserved even when < 1 LSB

## Bad consequence

- RMS quantisation noise increases from 0.3 to 0.5 LSB



# Quiz

- What is a *bipolar* A/D converter ?
- What is the amplitude of the quantisation noise introduced by an A/D converter ?
- How many threshold voltages are there in an *n*-bit converter ?
- What is the function of a priority encoder ?
- What is the level of quantisation noise for large signal variations ?
- What are the good and bad consequences of adding dither to a signal before conversion to digital ?

Lecture 12

# Analog-to-Digital Conversion (2)

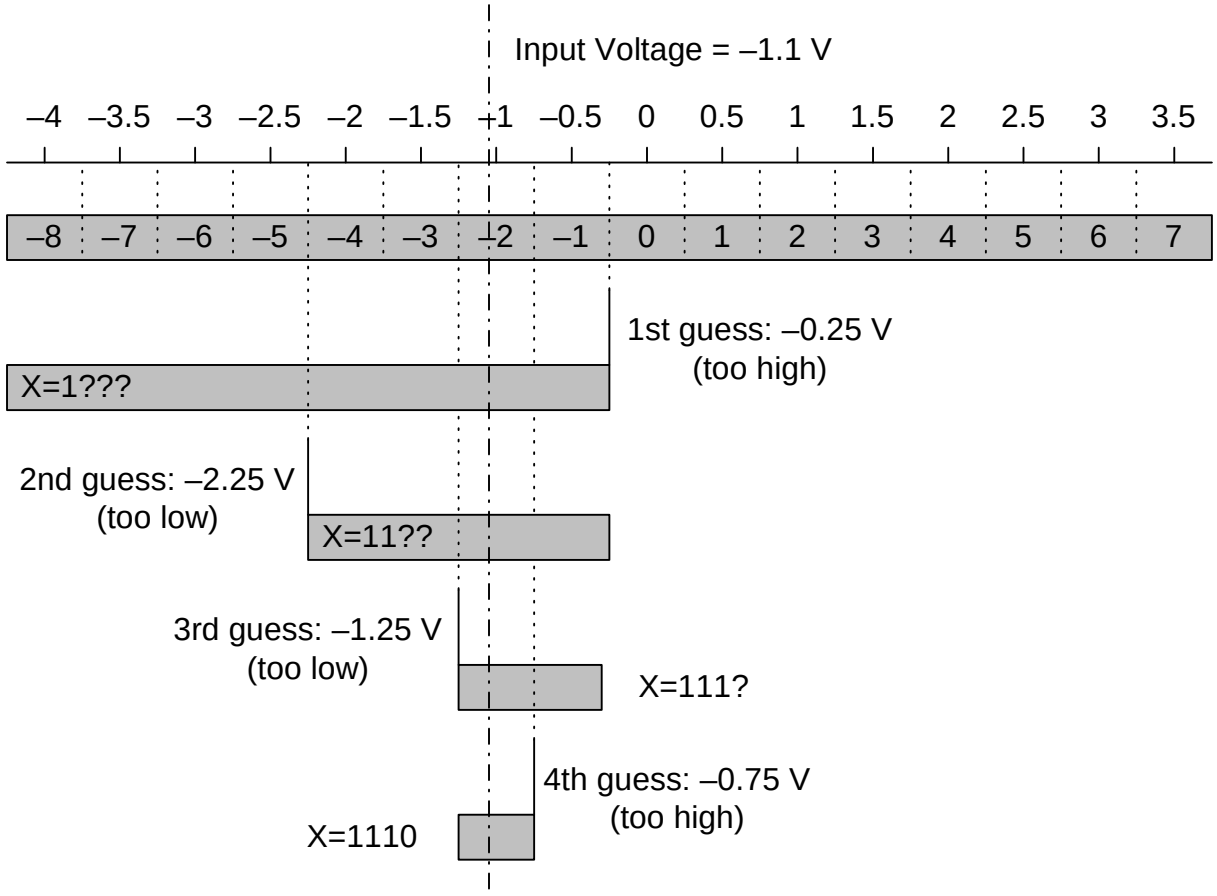
Objectives

- Understand the principles behind a successive approximation converter
- Understand how a successive approximation converter can be implemented using a state machine
- Understand the need for using a sample/hold circuit with a successive approximation converter
- Understand the origin of glitches at the output of a DAC and how they can be avoided.

# Successive Approximation Converter

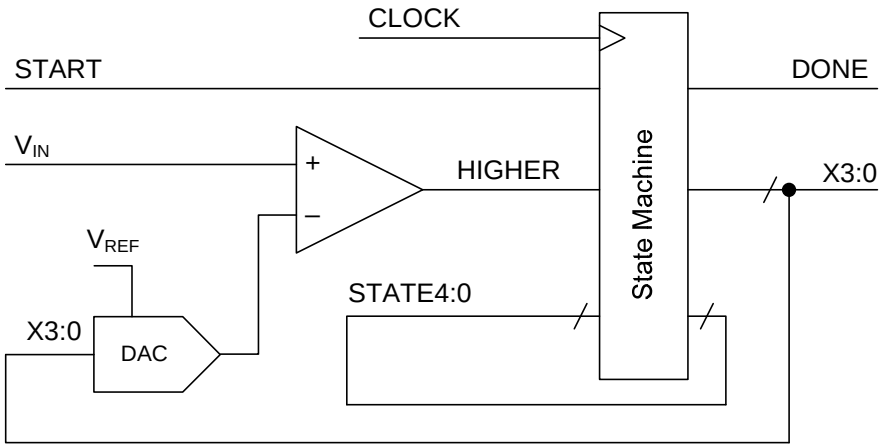
Make successive guesses and use a comparator to tell whether your guess is too high or too low.

Each guess determines one bit of the answer and cuts the number of remaining possibilities in half:




Use a DAC to generate the threshold voltages and a state machine to create the sequence of guesses. A DAC input of n generates the threshold between n–1 and n which equals (n–½) × 1 LSB

# Successive Approximation ADC

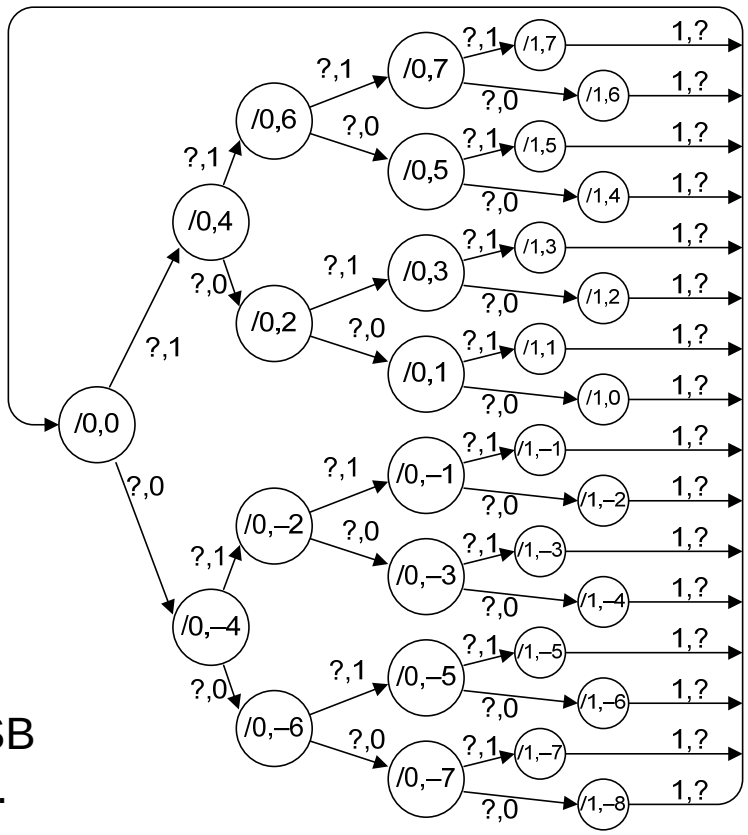



State Diagram:

A DAC input of *n* must generate the *threshold* between *n*–1 and *n*.

When the final column of states is reached, DONE goes high and the answer is X3:0.

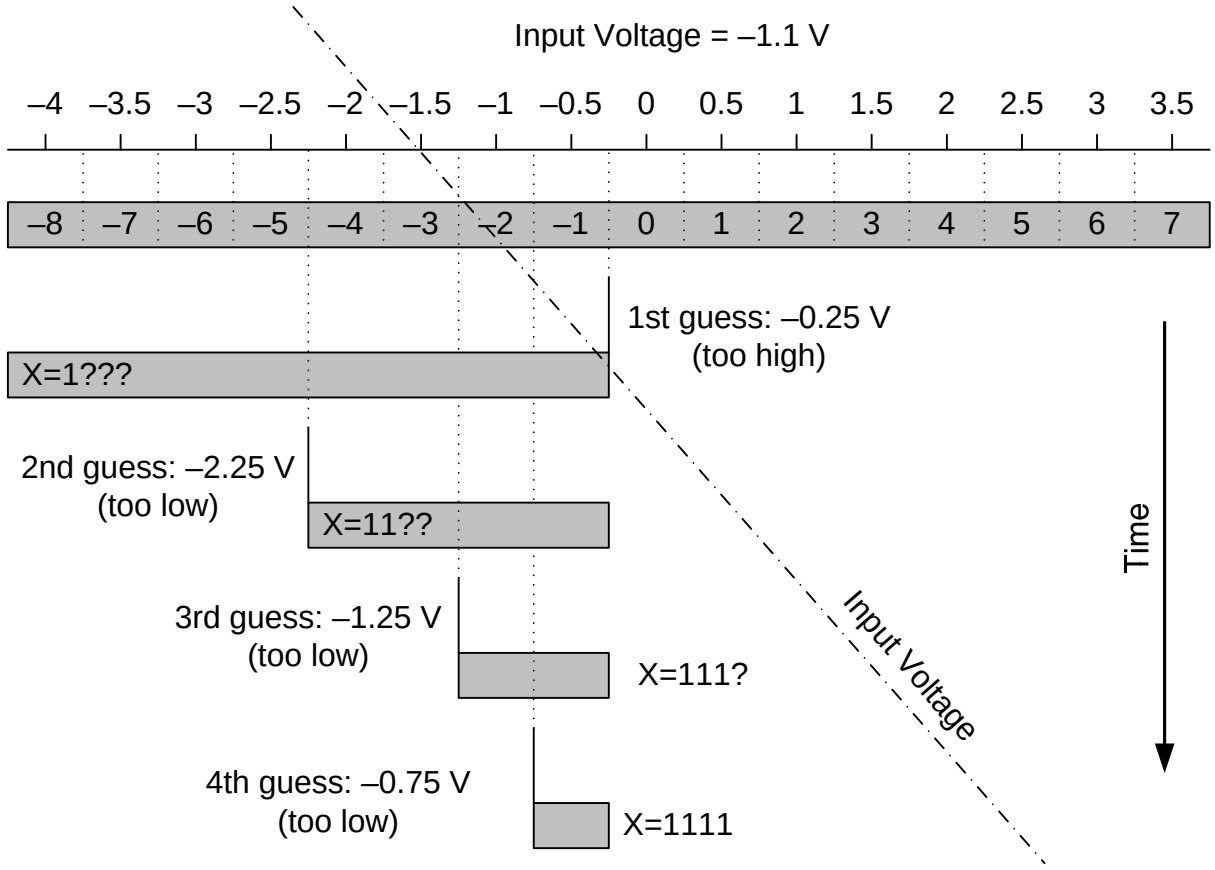
Note that it is possible to number the 31 states so that DONE is the MSB and X3:0 are the 4 LSB.




I/O Signals: START,HIGHER/DONE,X3:0

# Need for Sample/Hold

If the input voltage changes during conversion, the result is biased towards its initial value because the most significant bits are determined first.

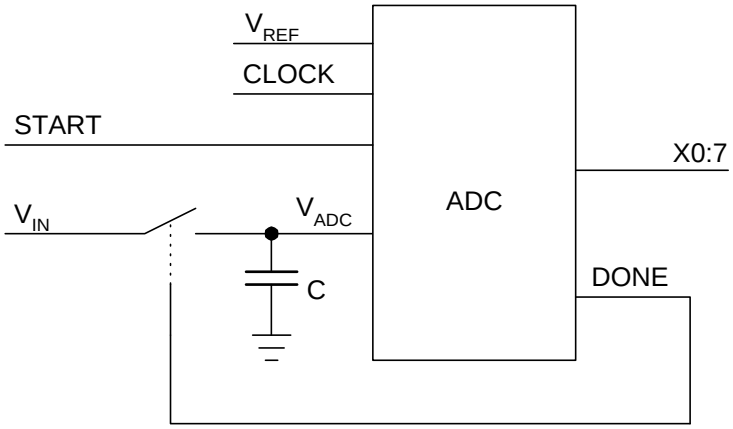



Increasing voltages will tend to be converted to values ending in …111. Decreasing voltages will tend to be converted to values ending in …000.

Consequences:

reduced precision, uncertain sample instant.

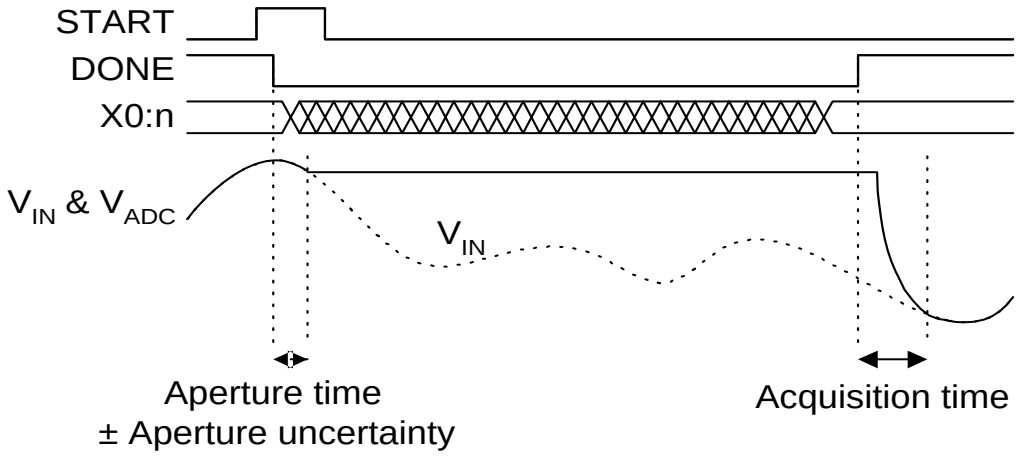
# A/D conversion with sample/hold



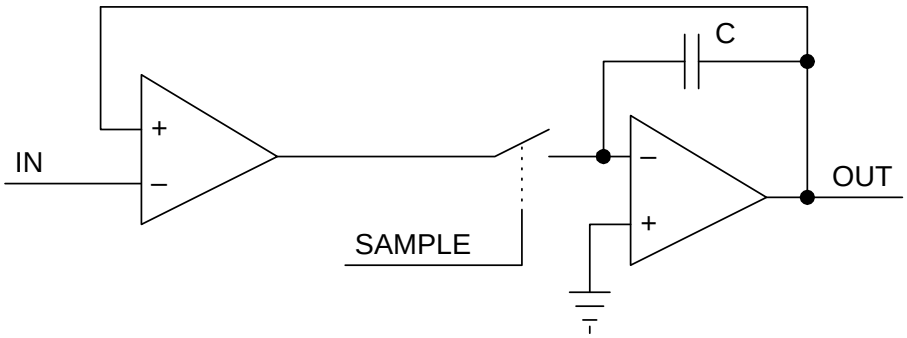

Input switch is opened during the conversion so $V_{ADC}$ remains constant.

Choice of $C$ is a compromise:

- Big $C$ keeps constant voltage despite leakage currents since $dV/dt = I_{leakage}/C$
- Small $C$ allows faster acquisition time for any given input current since $dV/dt = I_{in}/C$.



# Sample/Hold Circuit




When switch is open:

- Leakage currents through open switch and op-amp input will cause output voltage to drift up or down.
- Choose capacitor large enough that this drift amounts to less than 0.5 LSB during the time for a conversion
- Converters with high resolution or long conversion times need larger capacitors

When switch closes:

- Charge rate of capacitor is limited by the maximum op-amp output current. This determines the *acquisition time*: to acquire the signal to within ½LSB. It is typically of the same order as the conversion time.

Value of C is a compromise: big C gives slow acquisition, small C gives too much drift.

# Other types of Converter

## Sampling ADC

Many A/D converters include a sample/hold within them: these are *sampling* A/D converters.

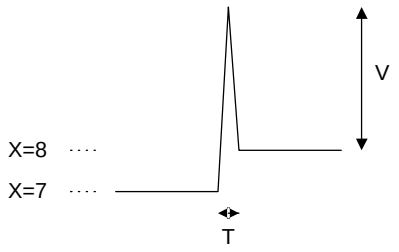
## Oversampling DAC and ADC

*Oversampling* converters (also known as ΣΔ or ΔΣ converters) sample the input signal many times for each output sample. By combining digital averaging with an error feedback circuit they can obtain up to 20 bits of precision without requiring a high accuracy resistor network (hence cheaper). A typical oversampling ratio is 128×, i.e. the input is sampled at 6.4MHz to give output samples at 50 kHz. Most CD players use an oversampling DAC.

# Glitches in DAC output voltages

Switches in DAC operate at different speeds ⇒ output glitches occur when several input bits change together:

0111 → 1000

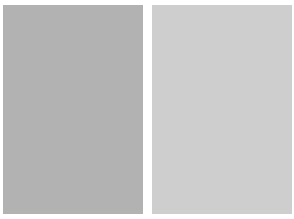



Cannot remove glitches: low pass filtering merely spreads out the glitch: the *glitch energy* = V × T remains constant.

Glitches are very noticeable on a video display:

Correct

With Glitchy DAC

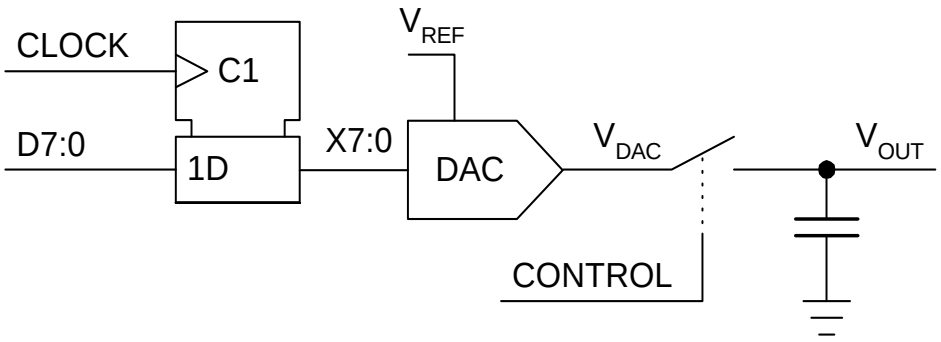


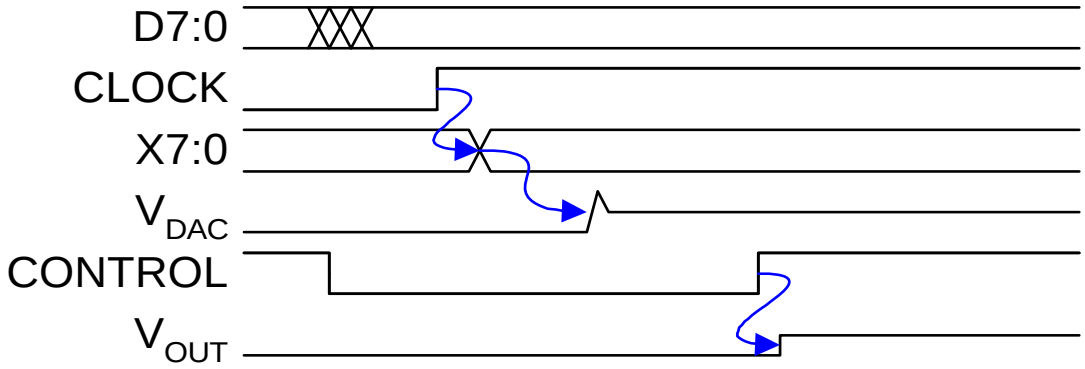
**Solution:** We use a sample/hold circuit to isolate the output from the DAC while the glitch is happening.

# Deglitching

To minimize the effect of glitches:

- Use a register to make inputs change as simultaneously as possible
- Use a sample/hold circuit to disconnect the DAC output while it is changing



# Summary

## D/A Converters:

- Weighted resistor: very fast (no op-amp), each bit can have an arbitrary weight, no good for big numbers.
- R-2R ladder: used for most converters, switch currents rather than voltages for higher speed. Multiplying DAC has an analog input as well.
- $\Sigma\Delta$ converters used for audio: very good linearity.

## A/D Converters:

- Flash converter: very fast (down to 1 ns), low precision (8 bits max), expensive and power hungry. A “pipeline” converter uses a DAC to subtract the converted value and measures the difference with another flash converter .
- Successive Approximation: medium speed (down to 0.1 µs), need to use sample/hold circuit to avoid input changing during conversion.
- $\Sigma\Delta$ converters dominate the medium to low speed market (down to 0.5 µs). Long been standard for audio: very good linearity (up to 24 bits). Very high speed sampling at low precision with dither, followed by low-pass digital filter and sub-sampling to desired sample rate.

# Quiz

- How many voltage comparisons are made by an *n*-bit successive approximation converter during the course of a conversion ?
- What is a *multiplying* DAC ?
- Why does the DAC in an *n*-bit successive approximation converter only need to to generate $2^n - 1$ different values rather than $2^n$ ?
- If a 12-bit successive approximation converter is used without a sample/hold, which of the output values 127, 128 and 129 are likely to occur least frequently ?
- What is the aperture uncertainty of a sample/hold circuit ?
- What two effects determine the acquisition time of a sample/hold circuit ?
- What happens if you try to improve a glitchy signal using a low-pass filter ?