Paper Number(s): **E2.1**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2006

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Monday, 12 June 2:00 pm

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): D.M. Brookes D.M. Brookes

Second Marker(s): T.J.W. Clarke T.J.W. Clarke

Information for Candidates:

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right.*

The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.

Unless otherwise stated, signed binary numbers are in 2's complement format.

1. [**Compulsory**]

(a) In the state machine shown in *Figure 1.1*, the state is represented by the value of the unsigned 2-bit number S1:0. The circuit is initially in state 0. Draw the state diagram for the circuit and complete the timing diagram shown in the figure by including the waveform of X and the state of the circuit during each clock cycle. Do not attempt to show gate propagation delays on your timing diagram. [8]

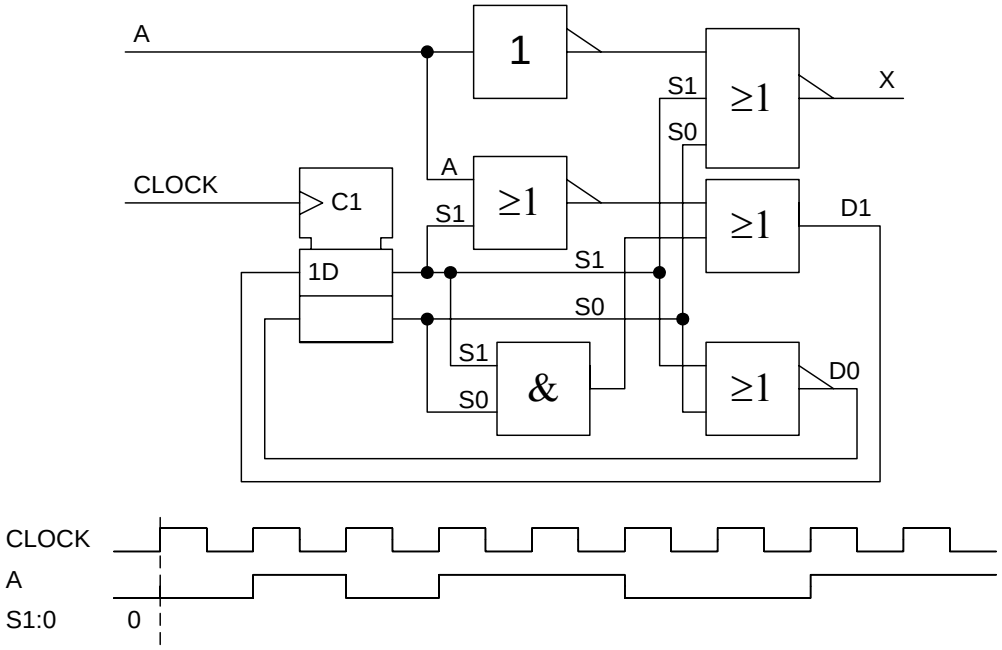
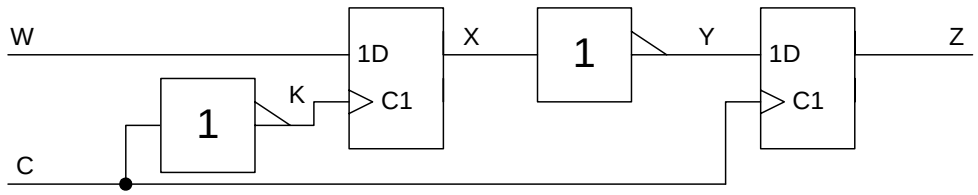


Figure 1.1

(b) In the circuit of *Figure 1.2*, the propagation delay of the flip-flops is $t_p = 8\text{ ns}$ while the setup and hold times are $t_s = 5\text{ ns}$ and $t_h = 2\text{ ns}$ respectively. The inverters have a propagation delay in the range $15\text{ ns} < t_g < 25\text{ ns}$. The clock signal C is symmetrical with period T. Write down the setup and hold inequalities that apply to the rightmost flip-flop and hence find the maximum clock frequency for the circuit.



[8]

Figure 1.2

(c) *Figure 1.3* shows a digital-to-analogue converter whose input, x, is a 2-bit unsigned number in the range 0 to 3 and whose output voltages are given in *Table 1.1*. The conductances of the four resistors are $G0$, $G1$, $G2$ and $G3$ respectively. The buffer output voltages are 0 V and 5 V for logic 0 and logic 1 inputs respectively. [8]

(i) Show that $Y = \dfrac{5(X0 \times G0 + X1 \times G1 + G3)}{G0 + G1 + G2 + G3}$.

(ii) If $G0 + G1 + G2 + G3 = 1\,\text{mS}$, find the values of $G0$, $G1$, $G2$ and $G3$.

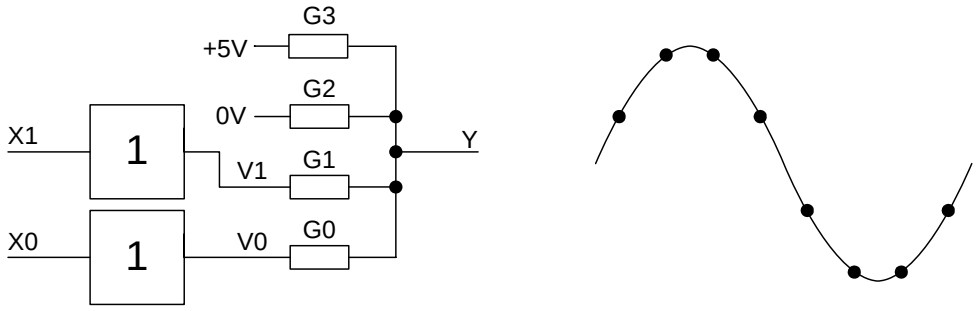


Figure 1.3

x	0	1	2	3
Y (volts)	0.190	1.543	3.457	4.810

Table 1.1: $Y = 2.5 + 2.5\sin(x \times 45° - 67.5°)$

(d) *Figure 1.4* shows the circuit of a 3-bit carry-skip adder. The worst-case propagation delays of the circuit elements are given in *Table 1.2*. [8]

(i) Determine the worst-case propagation delays to C2A from P0 and from C–1.

(ii) Explain briefly why C2A and C2B are identical except for propagation delays.

(iii) Determine the worst-case propagation delays to C2B from P0 and from C–1.

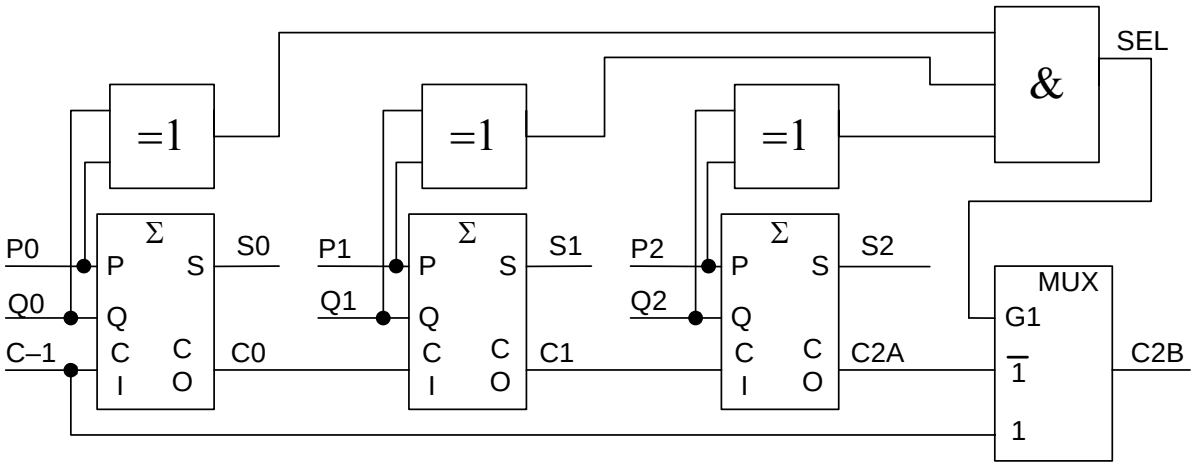


Figure 1.4

Device	Path	Delay
Adder	any input→S	3
	any input→CO	2
Multiplexer	SEL→output	3
	data inputs→output	2
XOR gate	any input→output	2
AND gate	any input→output	1

Table 1.2

(e) *Figure 1.5* shows part of a microprocessor system containing a Random Access memory (RAM), a Read-Only memory (ROM) and a serial input/output port. [8]

Determine simplified Boolean expressions for the three chip-enable signals CEA, CEB and CEC to ensure that the devices respond only to the address ranges given in *Table 1.3*.

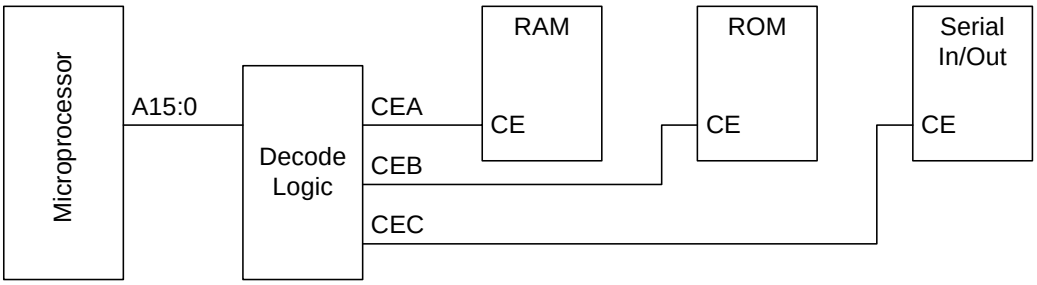


Figure 1.5

Device	Address Range (Hexadecimal)
RAM	0000 to BFFF
ROM	C000 to EFFF
Serial I/O Port	FF00 to FF07

Table 1.3

2. *Figure 2.1* shows a circuit consisting of a multiplexer, an 8-bit adder and an 8-bit register. The busses, K, N, P, Q and S represent the 8-bit twos complement signed numbers *k*, *n*, *p*, *q* and *s* respectively. The most significant bit of Q7:0 forms the output of the circuit and acts as the select input of the multiplexer. The CLOCK signal has a frequency of 1 MHz.

(a) For the particular case $n = 40$ and $k = -16$, complete the timing diagram shown in *Figure 2.1* by showing the values of *q*, *p* and *s* during each clock cycle and the waveform of Q7. The initial value of q is zero as shown. [10]

(b) Explain why, if *n* and *k* are held constant, the waveform of Q7 must be periodic. [2]

(c) In this part, you should assume that the initial value of q equals 0 and that the values of *n* and *k* are held constant and satisfy $n > -k > 0$. Define T to be the period of the Q7 waveform in clock cycles and α to be the fraction of clock cycles within a period for which Q7=1. [15]

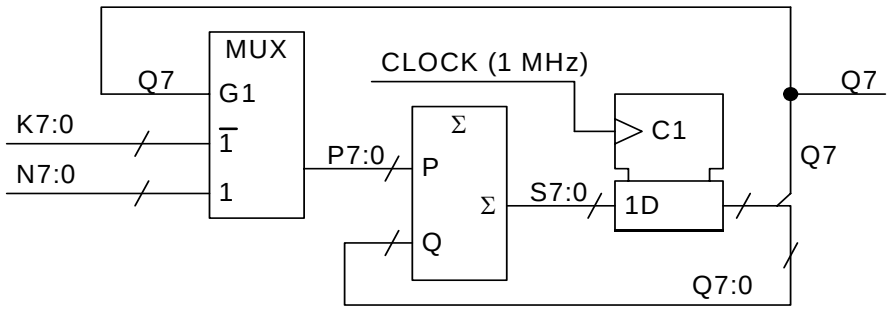
(i) Determine a relationship between α and the average value of *p* over an interval of *T* clock cycles.

(ii) Explain why it will always be true that $k \le q \le n-1$ and that Q7 can never be high in consecutive clock cycles.

(iii) Explain why the average value of *p* over T clock cycles must equal zero.

(iv) By combining your answers to parts (i), (ii) and (iii), derive an expression for the average pulse frequency of Q7 in terms of *n* and *k*.

(d) The propagation delays of the multiplexer, adder and register are 5 ns, 20 ns and 4 ns respectively and the register setup and hold times are 2 ns and 1 ns respectively. Determine the maximum frequency of CLOCK for correct circuit operation. [3]



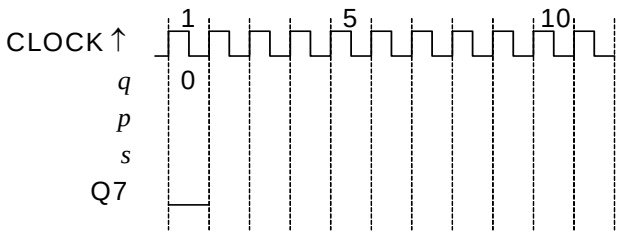


Figure 2.1

3. *Figure 3.1* shows part of the circuitry for receiving 6-bit asynchronous bit-serial data. Each data transmission consists of a start bit, six data bits and a stop bit each lasting for a nominal 16 μs. The data bits are transmitted with the least significant bit first and the start and stop bits are high and low respectively.

On the rising edge of the 1 MHz clock, the 7-bit counter (CTR7) is reset if $R = 1$ and increments otherwise. The 8-bit shift register (SRG8) shifts on the rising edge of the clock provided that SH=1. The contents of the logic blocks X and Y are defined by:

$$A = Q2 + Q3 + Q4 + Q5 + Q6 \qquad SH = Q0 \cdot Q1 \cdot Q2 \cdot \overline{Q3}$$

$$B = Q3 \cdot Q4 \cdot Q5 \cdot Q6 \qquad R = \overline{D} \cdot (\overline{A} + B)$$

(a) For each of the signals SH, A and B, define the values or range of values of q for which the signal is high where q denotes the unsigned value of Q6:0. [4]

(b) In the timing diagram in *Figure 3.1*, all signal transitions occur shortly after the CLOCK rising edge and times are given in μs relative to the first rising edge of D. The diagram shows a complete data transmission (lasting from 0 up to 128 μs) followed by a noise pulse followed by the start bit of the next data transmission. The diagram is not drawn accurately to scale.

(i) Determine the time of occurrence of each transition of A, B and R and the value of q immediately after the transition. You may assume that the initial value of q is zero and that propagation delays are negligible. [18]

(ii) State the contents of the shift register output, V7:0, at the time that B goes low and explain its relationship with the 6-bit transmitted value. [4]

(c) Assuming that each transmitted bit lasts precisely 16 μs, determine the maximum CLOCK frequency that will ensure that V7:0 has the correct value at the falling edge of B. You should neglect propagation delays and setup times but should not assume that the transmitted signal is synchronized with CLOCK. [4]

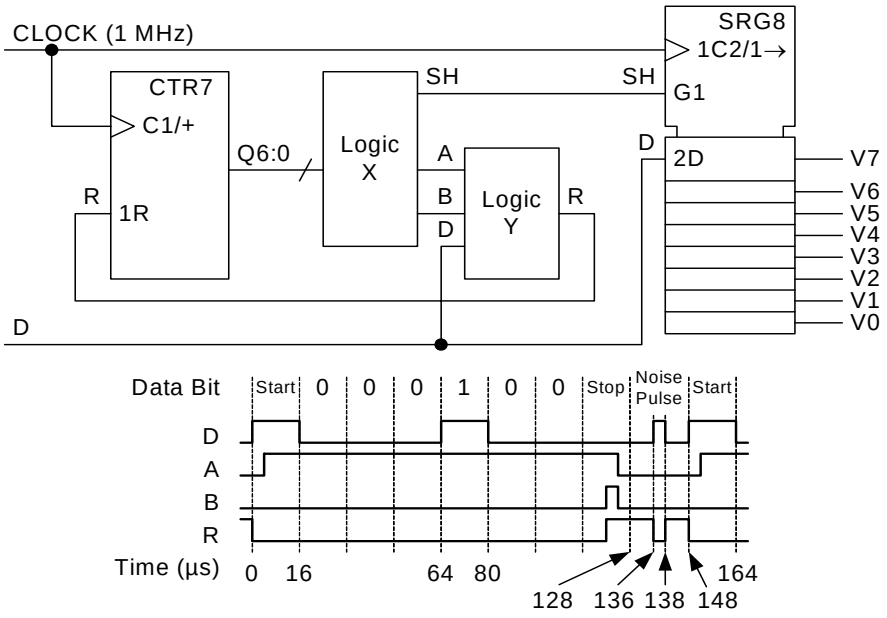


Figure 3.1

4. *Figure 4.1* shows part of the circuit of an integrating Analog to Digital converter. The analog circuitry comprises three switches, an integrator and a comparator. High voltages on the three digital signals REF, ZERO and IN cause the corresponding switches to close. You may assume the input offset voltages of the integrator and comparator to be negligible.

(a) The outputs of the logic block are shown in the timing diagram in *Figure 4.1* in which times are shown in ms. The 16-bit counter value goes to zero on the rising edge of ZERO and the counter period is 160 ms. Determine the input clock frequency and derive Boolean expressions for BK, ZERO and IN. [5]

(b) For the particular case $V_{REF} = 10\text{ V}$, $V_B = 5\text{ V}$, $V_{IN} = -2\text{ V}$ and $RC = 25\text{ ms}$, draw a timing diagram showing the waveforms of BK, ZERO, IN, REF, POS and the voltage V_X. Assume that the value of V_X is 0 V at the falling edges of BK and determine its value at each of the rising edges. [10]

(c) If the integrator output voltage is restricted to the range ±11 V, determine the maximum and minimum values of V_{IN} for which the circuit will function correctly. [6]

(d) Suppose that REF goes high for a time a in the first half of the cycle and b in the second half as shown in *Figure 4.1*. [9]

(i) Express V_B in terms of a, V_{REF} and T where $T = 20\text{ ms}$ is the pulse duration of ZERO and IN.

(ii) Show that $V_{IN} = V_{REF}\dfrac{a-b}{T+a}$.

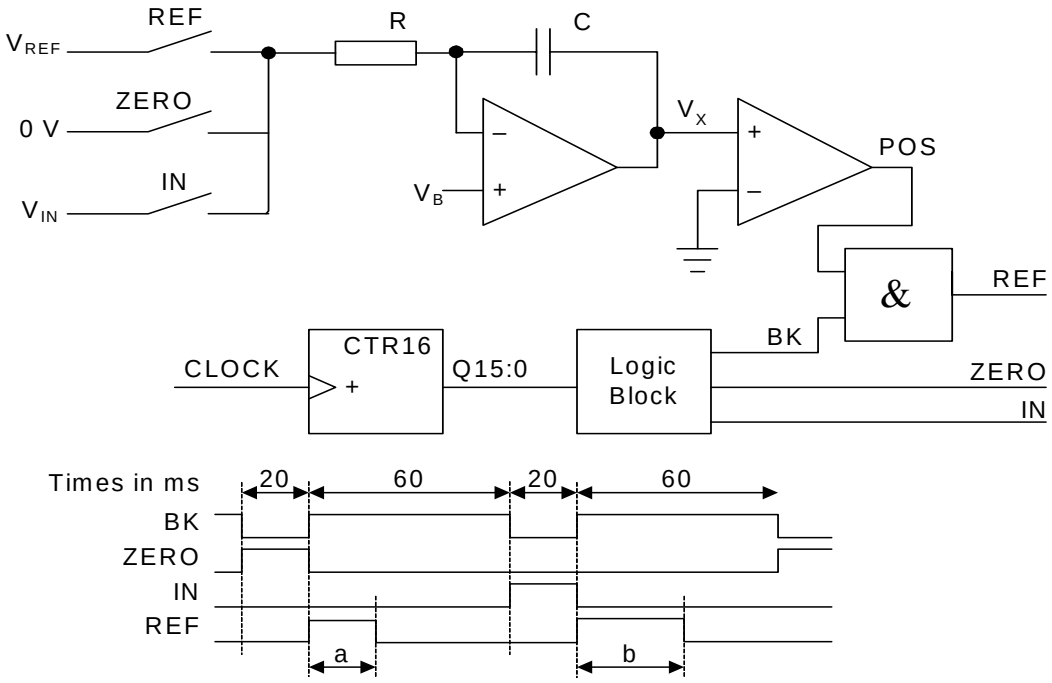


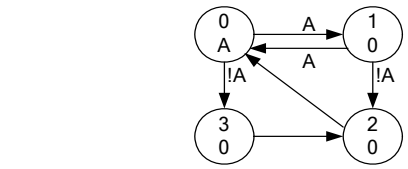
Figure 4.1

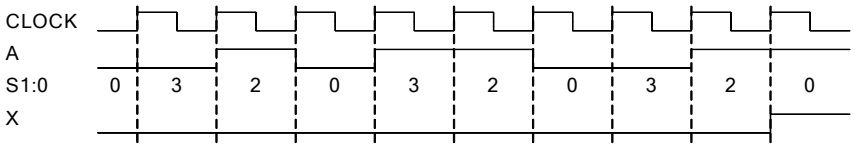
2006 E2.1/ISE2.2 Solutions

Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

. (a) We have $D1 = S1 \cdot S0 + \overline{S1} \cdot \overline{A}$, $D0 = \overline{S1} \cdot \overline{S0}$ and $X = \overline{S1} \cdot \overline{S0} \cdot A$. Hence:

	D1:0/X	A=0	A=1
S1:0	00	11/0	01/1
	01	10/0	00/0
	10	00/0	00/0
	11	10/0	10/0





[8A]

(b) The setup equation is:

$$½T + t_g + t_p + t_g + t_s < T \quad \Rightarrow \quad 25 + 8 + 25 + 5 < ½T \quad \Rightarrow \quad T > 126$$

The hold time equation is:

$$t_h < ½T + t_g + t_p + t_g \quad \Rightarrow \quad 2 < ½T + 15 + 8 + 15 \quad \Rightarrow \quad T > -72$$

Hence $T > 126$ ns $\Rightarrow$ $f < 7.94$ MHz

[8C]

(c) (i) Applying Kirchoff's current law to node Y gives: $\big((V0 - Y)G0 + (V1 - Y)G1 - Y \times G2 + (5 - Y)G3\big) = 0$. Rearranging this gives the requested expression.

(ii) When $x = 0$, we get $G3 = 0.190 \times 0.2$ mS $= 0.038$ mS

When $x = 1$, we get $G0 = 1.543 \times 0.2$ mS $-$ G3 $= 0.271$ mS

When $x = 2$, we get $G1 = 3.457 \times 0.2$ mS $-$ G3 $= 0.653$ mS

Finally $G2 = 1 - G0 - G1 - G3 = 0.038$ mS (not surprisingly equal to G3)

[8D]

(d) (i) $P0 \rightarrow C2A = 2+2+2 = 6$

$C-1 \rightarrow C2A = 2+2+2 = 6$

(ii) In an adder stage, if $Pn \oplus Qn = 1$, then the adder stage "propagates" the carry and CO=CI. We only get SEL=1 if all three stages are propagating their carry and so in this case C2A = C–1. Thus, since the multiplexer selects C2B = C-1, we will have C2B = C2A. [8AB]

If SEL=0, then the multiplexer selects C2B = C2A directly.

(iii) $P0 \rightarrow C2B = \max(2+2+2+2\ ,\ 2+1+3) = 8$

$C_{-1} \rightarrow C2B = 2$

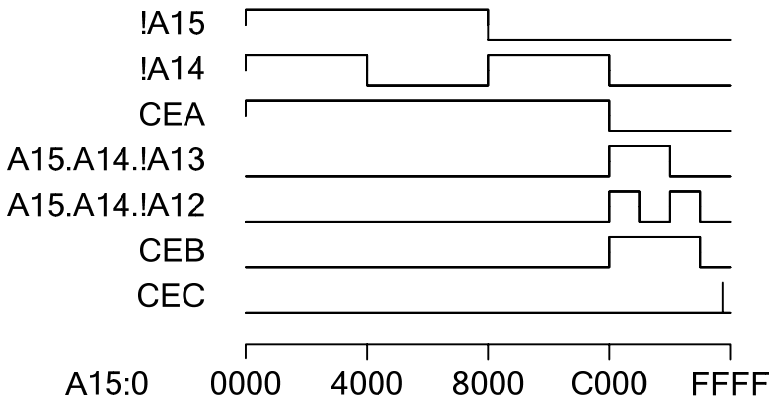
Note that although there is an apparent path $C_{-1} \rightarrow C0 \rightarrow C1 \rightarrow C2A \rightarrow C2B = 8$ this never actually arises; it is never true that a change in C-1 will cause this chain of cause and effect because it would require all the full-adders to be propagating the carry (to enable $C_{-1} \rightarrow C0 \rightarrow C1 \rightarrow C2A$) and also SEL=0 (to enable the final step $C2A \rightarrow C2B$). The entire point of the carry-skip circuit is that we prevent this from happening. Normally when analysing a circuit for the worst-case propagation delay, we assume that any path that is present in the circuit will be enabled for some set of input conditions; the carry-skip circuit is one of the rare cases when this assumption is untrue..

(e) $CEA = \overline{A15} + \overline{A14} = \overline{A15 \cdot A14}$ [8D]

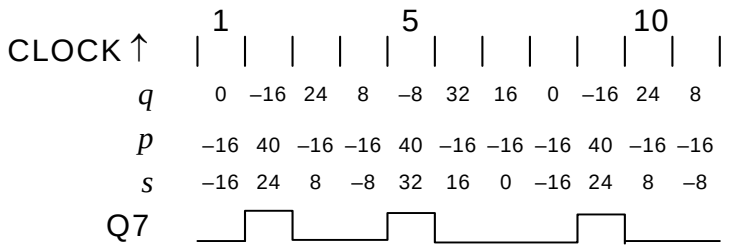
$CEB = A15 \cdot A14 \cdot \left(\overline{A13} + \overline{A12}\right) = A15 \cdot A14 \cdot \overline{\left(A13 \cdot A12\right)}$

$CEC = A15 \cdot A14 \cdot A13 \cdot A12 \cdot A11 \cdot A10 \cdot A9 \cdot A8 \cdot \overline{A7} \cdot \overline{A6} \cdot \overline{A5} \cdot \overline{A4} \cdot \overline{A3}$

Some of the terms in the expressions above are plotted below as functions of A15:0. Thus, for example, $\overline{A14}$ is true for addresses that fall in either of the ranges 0000 to 3FFF and 8000 to BFFF.



2. (a)



[10A]

(b) The circuit is a synchronous state machine with constant inputs and so it must be periodic. The maximum possible period is equal to the number of possible states which is 256. [2A]

(c) (i) The average value of p is $\alpha n + (1-\alpha)k$ since p equals n or k according to whether Q7 is high or low. [3A]

(ii) Since the initial value of q is zero, the proposition is initially true. Thereafter: [6A]

If $q \geq 0$, then $p = k \Rightarrow q' = q + k \geq k \Rightarrow k \leq q' < q$

If $q \leq -1$, then $p = n \Rightarrow q' = q + n \leq n - 1 \Rightarrow q < q' \leq n - 1$

$Q7 = 1 \quad \Rightarrow \quad p = n \quad \Rightarrow \quad q' = q + n \geq k + n > 0$ since $n > -k \quad \Rightarrow \quad Q7' = 0$

(iii) If the average value of p over a cycle of Q7 were a non zero value, x, then q would be incremented by x for every cycle of Q7 and would eventually fall outside the range $k \leq q \leq n-1$. [3A]

(iv) The average pulse frequency of Q7 is α MHz. We have $\alpha n + (1-\alpha)k = 0 \Rightarrow \alpha = \dfrac{k}{k-n} = \dfrac{1}{1+n/(-k)}$. For the example of part (a) this gives a frequency of $\dfrac{2}{7}$ MHz. [3A]

(d) We have $t_{reg} + t_{mux} + t_{add} + t_{setup} < T \Rightarrow T > 4 + 5 + 20 + 2 = 31 \text{ ns} \Rightarrow f < 32.3 \text{ MHz}$ [3C]

3. (a) SH=1 for $q \bmod 16 = 7 \Rightarrow q = 7,23,39,55,71,87,103,119$

A=1 for $q \geq 4 = 0000100_2$ [4A]

B=1 for $q \geq 120 = 1111000_2$

(b.i) [18A]

0: $R = \overline{D} \cdot (\overline{A} + B)$ goes low since D has gone high. q remains at 0 but the counter is now released.

4: q reaches 4 and so A goes high

120: q reaches 120 so B goes high which in turn takes R high

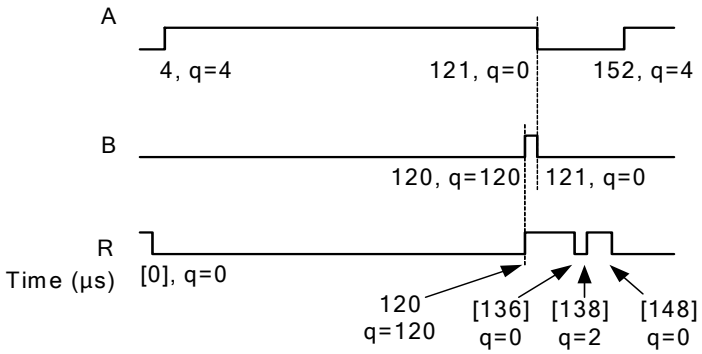
121: q resets to 0 because R is high, this causes both A and B to go low. R stays high because A is now low.

136: R goes low because D has gone high. q remains at 0.

138: q goes to 2 which is not large enough to make A high. Therefore R goes high again and q will reset to 0 at t=139.

148: R goes low because D has gone high. q remains at 0.

152: A goes high as q reaches 4



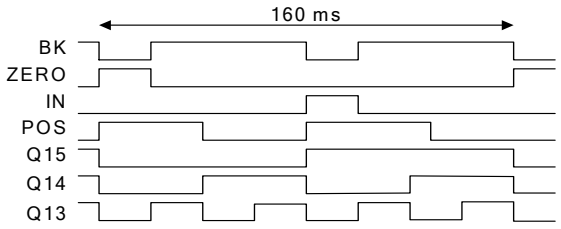
Times in brackets were given in question:

(b.ii) Data is shifted into the shift register in the centre of each bit cell. The data bits shifted in are, in sequence, 1, 0, 0, 0, 1, 0, 0, 0. Since the LSB is first, we have $V7:0 = 17 = 2x + 1$ where $x = 8$ is the transmitted value. [4A]

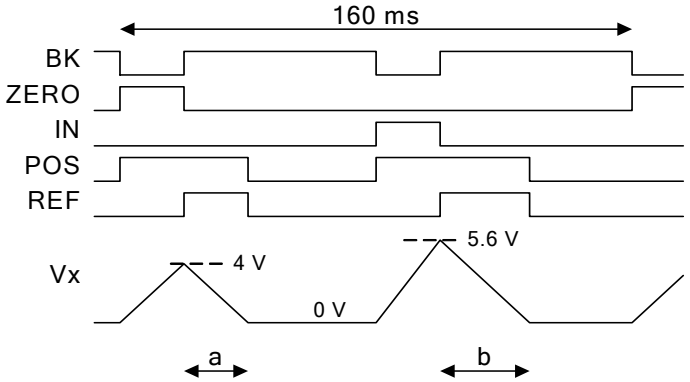
(c) The max CLOCK frequency is limited by the danger that the receiver might sample the last data bit instead of the STOP bit. If the received signal is unsynchronized, q might go to 1, immediately after the rising edge of the START bit. The STOP bit is sampled as q reaches 120. Therefore the CLOCK period, P, must obey $119P > 7 \times 16\ \mu s = 112\ \mu s$ giving a frequency of 1.063 MHz = 1/941µs. [4A]

4. (a) The input CLOCK frequency is $65536/160 = 409.6$ kHz.

$\text{BK} = \text{Q14} + \text{Q13}$, $\text{ZERO} = \overline{\text{Q15}} \cdot \overline{\text{Q14}} \cdot \overline{\text{Q13}}$, $\text{IN} = \text{Q15} \cdot \overline{\text{Q14}} \cdot \overline{\text{Q13}}$ [5A]



(b) The gradient of V_x is $\dfrac{V_B - V}{RC} = 40(5 - V)$ Volts/s where V is the input voltage. Thus we get gradients of 200, 280 and –200 V/s for ZERO, IN and REF respectively. This means that $a = 20$ ms and $b = 28$ ms and that the peak values of V_x are 4 V and 5.6 V respectively.



[10A]

(c) If $V_{IN} > 5$ then the initial integration will make V_x go negative rather than positive and the circuit will not work.

If the initial integration takes V_x to 11, then $0.8(5 - V_{IN}) = 11 \Rightarrow V_{IN} = -8.75$. [6A]

Therefore the maximum range is $-8.75 < V_{IN} < 5$.

(d) (i) The gradient of V_x is $(V_B - V)/RC$ V/s. During the first pair of integrations we have $(V_B - 0) \times T/RC = -a \times (V_B - V_{REF})/RC \Rightarrow V_B = V_{REF} \dfrac{a}{a+T}$ [9A]

(ii) During the second pair of integrations we have

$$(V_B - V_{IN}) \times T/RC = -b \times (V_B - V_{REF})/RC \Rightarrow V_{REF} = V_{IN} \frac{T}{b+T} + V_{REF} \frac{b}{b+T}$$

Equating this with the result of (i) gives

$$V_{IN} \frac{T}{b+T} = V_{REF} \left(\frac{a}{a+T} - \frac{b}{b+T} \right) = V_{REF} \left(\frac{(a-b)T}{(a+T)(b+T)} \right)$$

From which we get: $V_{IN} = V_{REF} \dfrac{a-b}{a+T}$