Paper Number(s): **E2.1**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2008

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Monday, 2 June 2:00 pm

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Time allowed: 2:00 hours

Examiners responsible:

First Marker(s): D.M. Brookes D.M. Brookes

Second Marker(s): T.J.W. Clarke T.J.W. Clarke

Information for Candidates:

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0. Signed binary numbers use 2's complement notation.*

1. (a) *Figure 1.1* shows the state table for a state machine which has a single input A and a state that is represented by the value of the unsigned 2-bit number S1:0. The table entries are of the form D1,D0 / X,Y where D1:0 denotes the next state and X and Y are the output signals during the current state. State transitions occur on the rising edges of CLOCK which, for convenience, have been shown as numbered dashed lines in *Figure 1.2*.

(i) Draw the state diagram for the circuit [5]

(ii) Complete the timing diagram shown in *Figure 1.2* by showing the state of the circuit during each clock cycle as a decimal number and the waveforms of X and Y. The state machine is initially in state 0 as shown. [3]

S1,S0	A=0	A=1
00	01/00	10/00
01	01/11	11/11
10	01/10	11/00
11	00/01	11/01

Figure 1.1

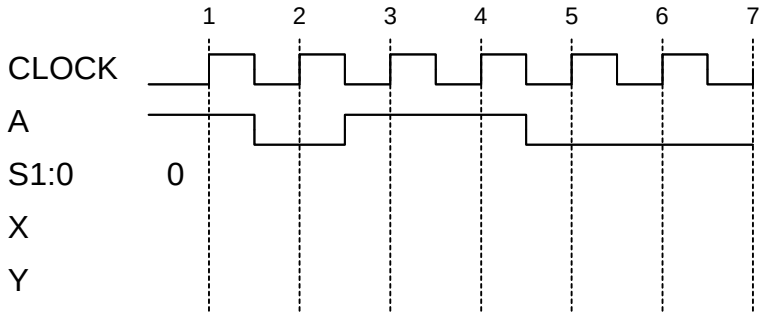


Figure 1.2

(b) In the circuit of *Figure 1.3* the propagation delays of the leftmost flipflop and the logic block are are t_p and t_d respectively. The rightmost flipflop has setup and hold times of t_s and t_h. The clock signal C is symmetrical with period T.

(i) Write the setup and hold inequalities that apply to the rightmost flip-flop. [5]

(ii) Find the maximum clock frequency for the circuit if the timing parameters (in ns) are: $t_p = 2, t_s = 11, t_h = 5$ and $7 \le t_d \le 23$ [3]

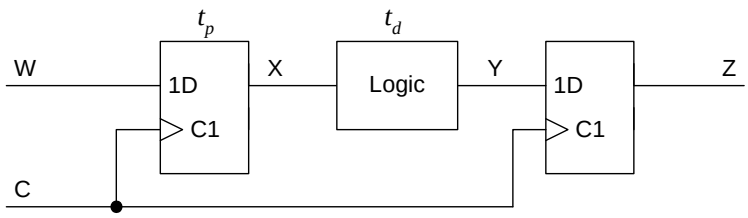


Figure 1.3

(c) *Figure 1.4* shows a digital-to-analogue converter whose input is a 3-bit unsigned binary number X2:0. Each of the three switches is labelled with the input bit that controls it and all switches are shown in the position corresponding to an input value of 0. The input voltage is $V_R = 1$ volt as shown.

(i) Determine the value of I_2 and explain why it is the same for both positions of the switch X2. [4]

(ii) Calculate the value of V_{OUT} when the input number X2:0 has the value 6. [4]

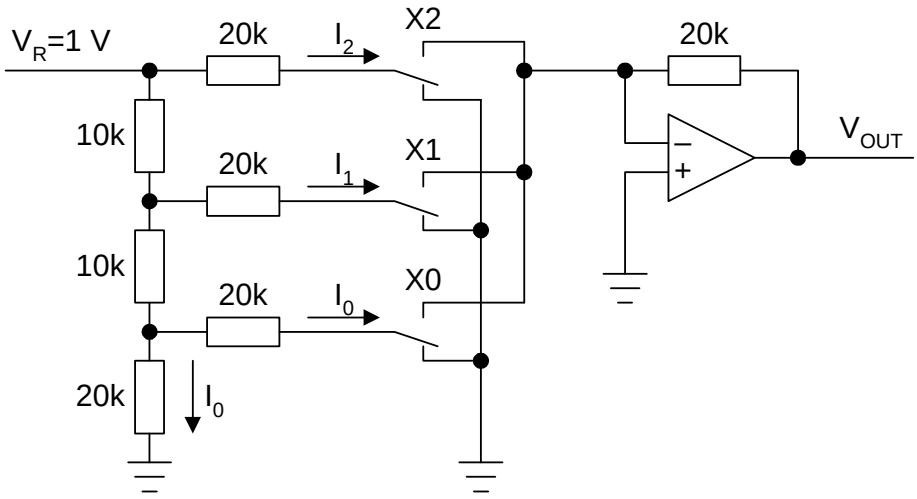


Figure 1.4

(d) A carry-lookahead adder is used to add together two 4-bit binary numbers X3:0 and Y3:0. The carry out of adder stage 1 is generated using either of the following equivalent expressions:

$$\begin{aligned} C1 &= G1 + P1 \cdot G0 + P1 \cdot P0 \cdot CI \\ &= G1 + P1 \cdot (G0 + P0 \cdot CI) \end{aligned}$$

where CI is the carry into the least significant adder stage and G*n* and P*n* are defined by $Gn = Xn \cdot Yn$ and $Pn = Xn + Yn$.

(i) Determine the maximum propagation delay from any X or Y input to C1 separately for each of the two expressions given above. Assume that AND and OR gates each have a delay of 1 unit. [4]

(ii) Give a similar expression for C2, the carry out of stage 2, and determine the propagation delay from any X or Y input when it is implemented from an unfactorized expression. [4]

(e) X7:0 is an 8-bit unsigned number in the range 0 to 255. Determine the decimal number range or ranges of values of X7:0 for which the following expressions are true:

(i) $X7 \cdot \overline{X6} \cdot X5$ [4]

(ii) $X6 \oplus X5$ [4]

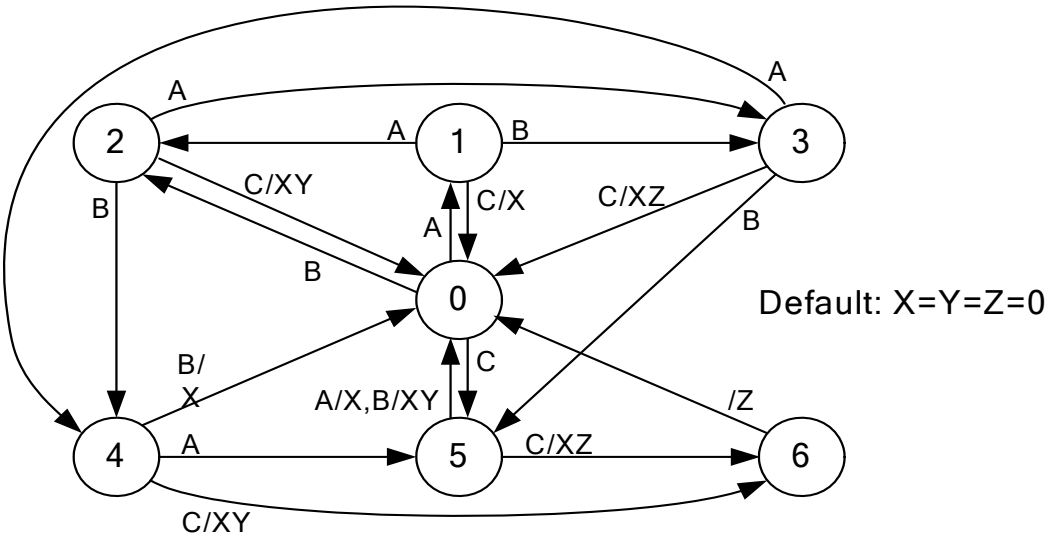
2. A state machine that controls a vending machine has three input signals A, B and C which go high for one clock cycle following the insertion of 10p, 20p and 50p coins respectively. At most one of A, B and C is ever high at a time and their transitions occur shortly after the CLOCK rising edge. The state machine has three outputs, X, Y and Z which respectively dispense a chocolate bar and give 10p and 20p coins as change. *Figure 2.1* shows the state diagram for the vending machine; the outputs are all low except where indicated on transition arrows.

(a) Complete the timing diagram shown in *Figure 2.1* showing the sequence of states, S2:0, as a decimal number and the waveforms of X, Y and Z. [7]

(b) Deduce the cost of a chocolate bar. [3]

(c) Give simplified Boolean expressions for X, Y and Z. [12]

(d) Draw a revised state diagram for a state machine having the same input and output signals as before but with a chocolate bar price of 40p. The outputs Y and Z must never be high simultaneously. [8]



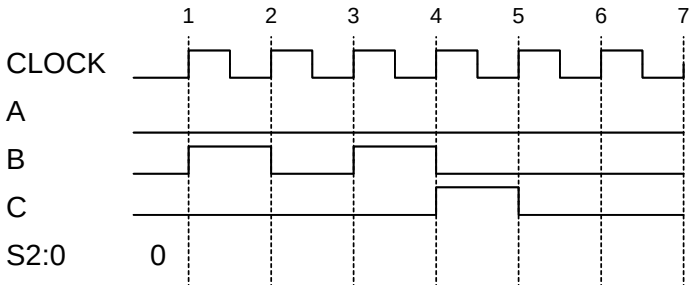


Figure 2.1

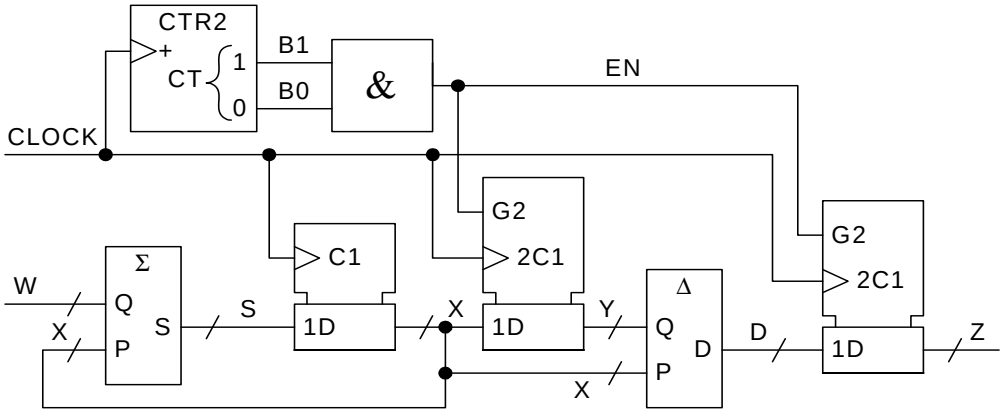
3. The circuit of *Figure 3.1* consists of an adder (Σ), a subtractor (Δ), a 2-bit counter (CTR2), an AND gate and three registers. The two registers that include a clock enable input ignore CLOCK edges whenever EN=0. The output of the subtractor is given by D=P–Q. The signals S, D, W, X, Y, Z represent multi-bit signed binary numbers whose decimal values during clock cycle n are denoted by $s(n), d(n), \cdots, z(n)$ respectively. All signal transitions occur shortly after the rising edge of CLOCK.

(a) Complete the timing diagram of *Figure 3.1* by giving the value of B1:0 in each clock cycle, the waveform of EN and the values of x, y and z in each clock cycle. The vertical dashed lines denote CLOCK rising edges and the clock cycles are numbers 1 to 13 for convenience. The initial values of B1:0, x, y and z are zero as shown. You may assume that the adder and subtractor never overflow. [14]

(b) The registers and counter have a propagation delay of 10 ns and setup/hold times of 5 ns and 2 ns respectively. The AND gate has a propagation delay of 3 ns and the adder/subtractor circuits have a propagation delay of 18 ns. Determine the maximum clock frequency. [4]

(c) Show that $x(k) = \sum_{n=1}^{k-1} w(n)$ and that $y(4m) = x(4m-4)$ where k and m are positive integers. [6]

(d) Derive an expression for $z(4m)$ in terms of $w(n)$ and, for $m = 3$, compare your solution with the answer given in part (a). [6]



n	1	2	3	4	5	6	7	8	9	10	11	12	13
w	6	–1	7	6	–2	6	7	5	–1	–4	–3	–1	0
B1:0	0												
EN													
x	0												
y	0												
z	0												

Figure 3.1

4. *Figure 4.1* shows a 4-bit analogue-to-digital converter (ADC). The circuit consists of a 2-bit flash ADC (labelled ADC1) whose output is used to select the reference voltages of a second, 3-bit, flash ADC consisting of a resistor chain, five comparators and a logic block. The unsigned values of R1:0 and P2:0 are r and p respectively. The logic block outputs are: $P2 = B \cdot C \cdot D$, $P1 = A \cdot B \cdot \overline{D} + \overline{B} \cdot D \cdot E$ and $P0 = A \oplus B \oplus C \oplus D \oplus E$. The output of the first ADC, r, and the resultant voltages at Y and Z are given by:

Input Voltage X (Volts)	X<–4	–4≤X<0	0≤X<+4	+4≤X
ADC1 Output, *r*	1	2	3	0
Voltages Y and Z (Volts)	–8, –4	0, –4	0, +4	+8, +4

(a) Complete a truth table giving the decimal value of p for the each of the following ten combinations of A, B, C, D, E: 00000, 10000, 11000, 11100, 11110, 11111, 01111, 00111, 00011, 00001. [12]

(b) If the switches are fixed in the position shown (i.e. Y=0 and Z=–4 volts) determine which of the combinations of A, B, C, D, E from part (a) might occur and the range of X voltages that will result in each. Hence show that, for –5≤X<1, the value of P2:0 is given by $p = 5 + \text{floor}(X)$ where floor(•) denotes rounding down to the next lowest integer (e.g. $\text{floor}(-1.5) = -2$). [6]

(c) Find a similar expression for p if the switches are instead in the position corresponding to $r = 3$ (i.e. Y=0 and Z=+4 volts). [6]

(d) The final output of the ADC is given by the four least significant bits of the sum $s = p + 4r + 3$. Show how s may be generated from R1:0 and P2:0 using a single 4-bit adder. [6]

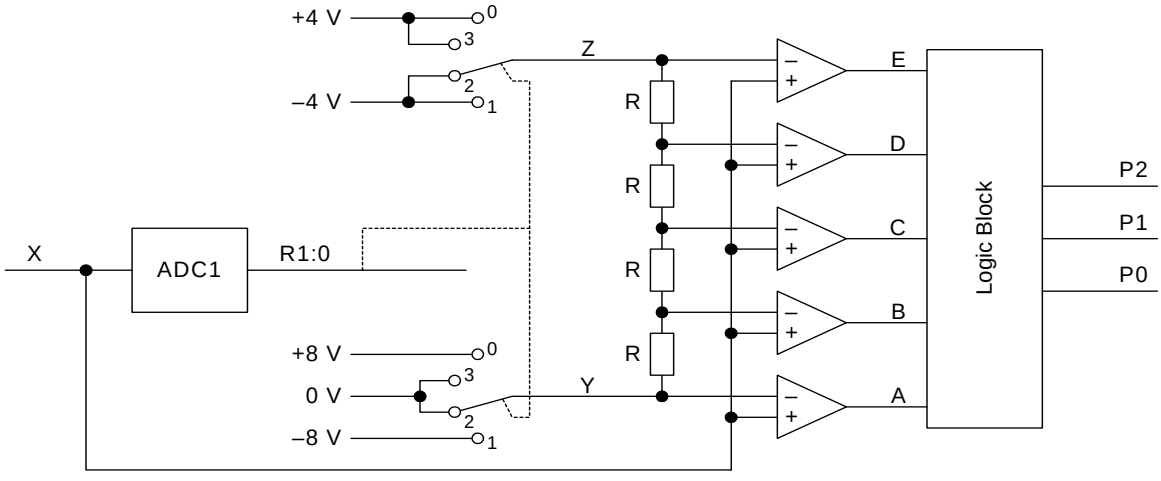
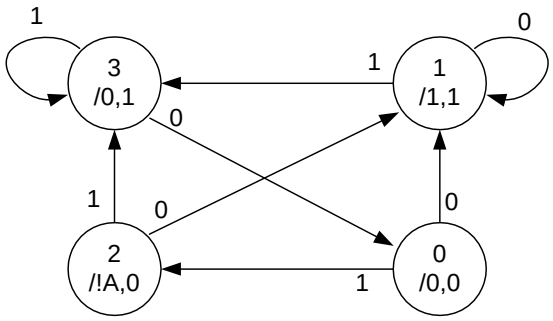


Figure 4.1

2008 E2.1/ISE2.2 Solutions

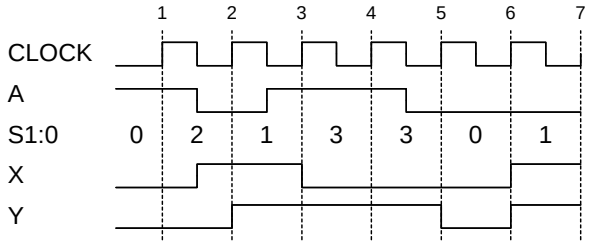
Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1. (a)



I/O Signals: A/X,Y

[5A]



[3A]

(b) The setup equation is:

$$t_p + t_d + t_s < T \quad \Rightarrow \quad 2 + 23 + 11 < T \quad \Rightarrow \quad T > 36$$

The hold time equation is:

$$t_h < t_p + t_d \quad \Rightarrow \quad 5 < 2 + 7 \quad \Rightarrow \quad 5 < 9 \text{ [OK]}$$

[5C]

Hence $T > 36$ ns $\Rightarrow$ $f < 27.8$ MHz [3C]

(c) (i) $I_2 = 1/20k = 50\,\mu$A. It is independent of the switch position because both sides of the switch are at ground potential: a true ground in one case and a virtual earth in the other. [4A]

(ii) The current into the op-amp summing junction is 75 µA. Thus $V_{OUT} = -75\times10^{-6}\times20\times10^{3} = -1.5$ V [4A]

(d) (i) The unfactorized expression has a propagation delay of 3 gates: one to generate G*n* and P*n*, one to form the AND product terms and one to OR them together. The factorized expression has a delay of 5 gates since P0, $P0 \cdot CI$, $G0 + P0 \cdot CI$, $P1 \cdot (G0 + P0 \cdot CI)$ and C1 must be formed in sequence. [4A]

(ii) The expression is [4B]

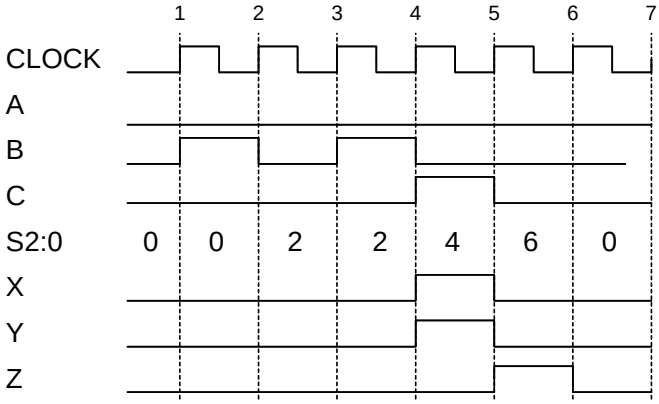
$$C2 = G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot CI$$

and the propagation delay in this form remains 3 gates.

(e) (i) The smallest value is when X4:0 = 0 which gives 160. The largest value is when X4:0 = 1 which is 160+31=191. Thus the range is 160 to 191. [8A]

(ii) There are two ranges according to whether X7 = 0 or 1. If X7 = 0, the smallest value is 00100000 = 32 and the largest is 01011111 = 95. If X7 = 1, we just add 128 to these values. Thus the ranges are 32 to 95 and 160 to 223.

2. (a) The timing diagram is:



[7A]

[3A]

(b) You insert 90p but receive 30p in change: 10p from state 4 and 20p from state 6.

Hence the cost of a chocolate bar is 60p.

(c) Expressions for the output signals (where digits represent states) are:

$$X = C \cdot (1+2+3+4+5) + B \cdot (4+5) + A \cdot 5$$
$$= C \cdot ((S2 \oplus S1) + S0) + S2 \cdot (A \cdot S0 + B \cdot \overline{S1})$$
$$= C \cdot \overline{S2} \cdot (S1+S0) + S2 \cdot \overline{S1} \cdot (A \cdot S0 + B + C)$$

[5D]

$$Y = C \cdot (2+4) + B \cdot 5$$
$$= C \cdot \overline{S0} \cdot (S2 \oplus S1) + B \cdot S2 \cdot S0$$

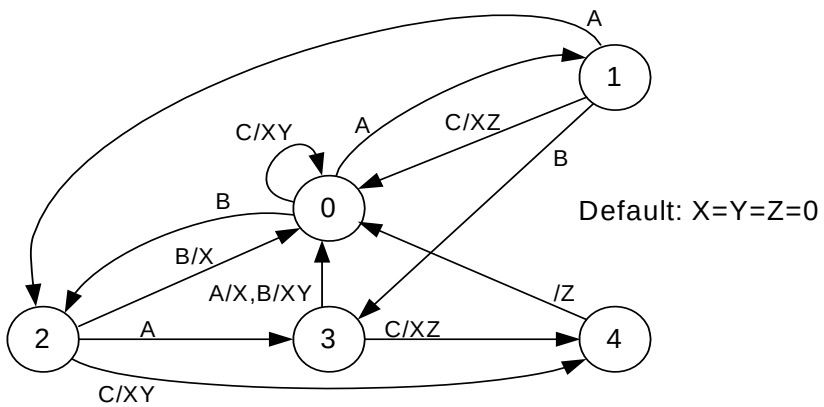
[4D]

$$Z = C \cdot (3+5) + 6$$
$$= C \cdot S0 \cdot (S2 + S1) + S2 \cdot S1$$

[3D]

These expressions assume that state 7 never arises.

(d) The easiest way to modify the state diagram is to just assume an initial credit of 20p and leave everything else the same. Thus all branches that used to go to state 0 now go to state 2. We then subtract 2 from each state number to give the following: [8D]



3. (a) In the timing digram, EN goes high whenever $q = 3$ (i.e. when n is a multiple of 4). The values of y and z change on the next CLOCK rising edge.

n	1	2	3	4	5	6	7	8	9	10	11	12	13
w	6	–1	7	6	–2	6	7	5	–1	–4	–3	–1	0
Q1:0	0	1	2	3	0	1	2	3	0	1	2	3	0
EN				‾‾‾				‾‾‾				‾‾‾	
x	0	6	5	12	18	16	22	29	34	33	29	26	25
y	0	0	0	0	12	12	12	12	29	29	29	29	26
z	0	0	0	0	12	12	12	12	17	17	17	17	–3

[14A]

(b) The worst case delay path is Y to D to Z.
This gives $10 + 18 + 5 \le T \quad \Rightarrow \quad T \ge 33 \quad \Rightarrow \quad f \le 30.3\,\text{MHz}$ [4A]

(c) We can show the $x(k)$ expression by induction since $x(k) = x(k-1) + w(k-1)$ and the proposition is true for $k = 1$ since the sum is empty. A less formal but logical argument will also be accepted.

From part (a), we see that $y(4m)$ was stored at the end of cycle $4m-4$ (which was the last time EN was high). Thus $y(4m) = x(4m-4)$ which is the required result. [6A]

(d) From the timing diagram, we see that:

$$z(4m) = x(4m-4) - y(4m-4) = x(4m-4) - x(4m-8)$$
$$= \sum_{n=4m-8}^{4m-5} w(n) = \sum_{r=1}^{4} w(4m-4-r) = \sum_{k=1}^{4} w(4m-9+k)\,.$$

[6A]

For $m = 3$, $z(12) = w(4) + w(5) + w(6) + w(7) = 6 - 2 + 6 + 7 = 17$. This agrees with the answer in part (a).

4. (a) p counts the number of high inputs and the truth table is given by:

ABCDE	p	ABCDE	p
00000	000=0	11111	101=5
10000	001=1	01111	100=4
11000	010=2	00111	011=3
11100	011=3	00011	010=2
11110	100=4	00001	001=1

[12A]

(b) Since Z<Y, the upper comparator outputs will go high in preference and so only the rightmost column in the above table is possible together with the case 00000. This gives the following table:

X	X<–4	–4<X<–3	–3<X<–2	–2<X<–1	–1<X<0	X>0
p	0	1	2	3	4	5
fl(X)	<–4	–4	–3	–2	–1	0

[6A]

From the table we see that $p = 5 + \text{floor}(X)$ is valid for –5≤X<1,

(c) Since Y<Z, only the leftmost column in the above table is possible together with the case 11111. This gives the following table:

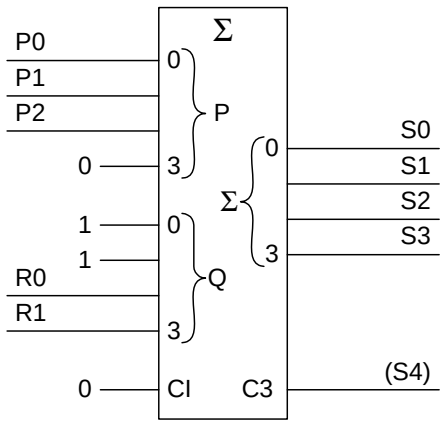
X	X<0	0<X<1	1<X<2	2<X<3	3<X<4	X>4
p	0	1	2	3	4	5
fl(X)	<0	0	1	2	3	4

[6A]

From the table we see that $p = 1 + \text{floor}(X)$ is valid for –1≤X<5,

(d) We may generate $4r + 3$ by shifting r left by two bits and setting the two LSBs to 1. This gives the circuit below and we can use C3 as the fifth output bit, S4:

[6D]



s can range from 3 to 20, so we need 5 bits to represent it as an unsigned number. Although this was not part of the question, the converter output is taken as S3:0 interpreted as a signed 4-bit number which has the value $s - 16$ when $r \geq 1$ and s when $r = 0$ for $-8 < X < +8$.