IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2009

EEE/ISE PART II: MEng, BEng and ACGI

DIGITAL ELECTRONICS 2

Thursday, 28 May 2:00 pm

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Time allowed: 2:00 hours

Examiners responsible:

  First Marker(s):   D.M. Brookes D.M. Brookes

  Second Marker(s):   T.J.W. Clarke T.J.W. Clarke

Information for Candidates:

Notation: *Unless explicitly indicated otherwise, digital circuits throughout this paper are drawn with their inputs on the left and their outputs on the right. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0. Signed binary numbers use 2's complement notation.*

1. (a) *Figure 1.1* shows the state diagram for a state machine which has a single input, A, a single output, X, and a state that is represented by the value of the unsigned 2-bit number S1:0. State transitions occur on the rising edges of CLOCK which, for convenience, have been shown as numbered dashed lines in the timing diagram of *Figure 1.1*.

   (i) Draw the state table for the circuit. [3]

   (ii) Complete the timing diagram shown in *Figure 1.1* by showing the state of the circuit during each clock cycle as a decimal number and the waveform of X. The state machine is initially in state 0 as shown. [5]
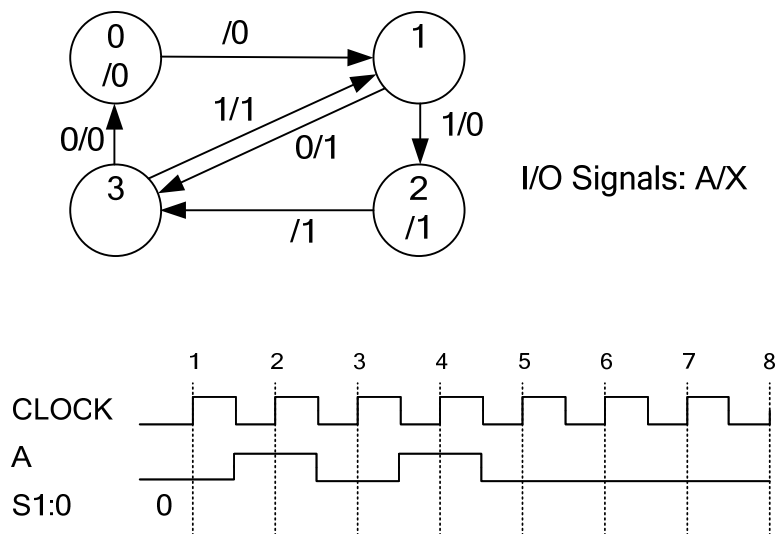

Figure 1.1

   (b) In the circuit of *Figure 1.2* the propagation delays of the leftmost flipflop and the logic block are t_p and t_d respectively. The rightmost flipflop has setup and hold times of t_s and t_h. The clock signal C is symmetrical with period T.

   (i) Write the setup and hold inequalities that apply to the rightmost flip-flop. [5]

   (ii) Find the maximum clock frequency for the circuit if the timing parameters (in ns) are: $t_p = 6, t_s = 5, t_h = 2$ and $15 \le t_d \le 27$. [3]
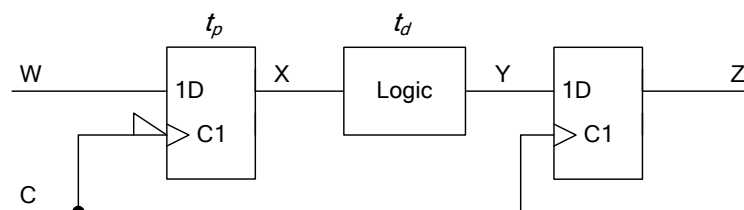

Figure 1.2

(c) *Figure 1.3* shows a successive-approximation analogue-to-digital converter preceded by a sample/hold circuit formed from an op-amp, an electronic switch and a capacitor. The converter has 14 bits precision and a full scale input range of $\pm 5\,\text{V}$.

If the A/D input current lies in the range $\pm 20\,\text{nA}$, calculate the minimum value of C to ensure that V_C does not vary by more than $\frac{1}{2}\,\text{LSB}$ during the $2\,\mu\text{s}$ conversion time. [8]
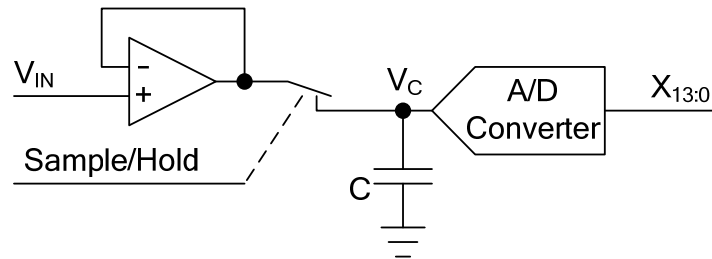

Figure 1.3

(d) *Figure 1.4* shows a circuit containing a 4-bit full adder. X3:0 and Y6:0 are unsigned binary numbers whose values are x and y respectively.

(i) Show that $y = 5x$. [2]

(ii) Determine the maximum possible value of y. [2]

(iii) If X3:0 is now a signed two's complement binary number whose value is x, give the maximum and minimum values of $y = 5x$. [2]

(iv) Show how the circuit must be modified to calculate $y = 5x$ correctly when X3:0 is a signed number as in part (iii). [2]
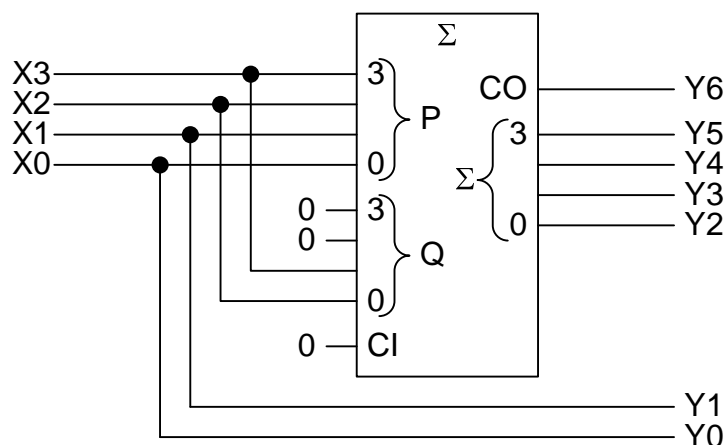

Figure 1.4

(e) X7:0 is an 8-bit signed number in the range –128 to +127. Determine the decimal number range or ranges of values of X7:0 for which the following expressions are true:

(i) $\overline{X7}\cdot\overline{X6}\cdot X5\cdot X4$ [4]

(ii) $\left(\overline{X7}\oplus X6\right)\cdot\left(\overline{X7}\oplus X5\right)$ [4]

2. The synchronous state machine shown in Figure 2.1 has a single input signal, B, and two output signals S and D. The signal T is the most significant output bit of the 10-bit counter, labelled CTR10. On the rising edge of the 1 kHz CLOCK, the counter increments if R and T are both low and resets to zero if R is high. The input, B, goes high whenever a button is pressed and the purpose of the state machine is to detect and distinguish between single and double clicks of the button. The state machine has six states and its state diagram is shown in Figure 2.1.

(a) By considering the action of the counter, explain why its T output will go high approximately 0.5 s after R goes low and why it will then remain high until one cycle after R goes high. [8]

(b) Complete the timing diagram in Figure 2.1 by showing the sequence of states taken, the waveforms of R and T and the times when output pulses occur on the S and D outputs. The initial state is 0 as shown. Do not attempt to show time delays of 1 or 2 ms on your diagram. [12]

(c) Giving your reasons fully, determine the start time to the nearest millisecond of the output pulse that results from the rising edge of B at time $t = 0.5$ s. All transitions in B occur just after the rising edge of CLOCK. [5]

(d) The state machine is to be modified to include a third output L. The outputs D and S should generate pulses for double and short single clicks as before, and the new output, L, should generate a pulse for a long single click where the button is held down for more than about 0.5s. Show what changes are necessary to the state diagram to achieve this. [5]
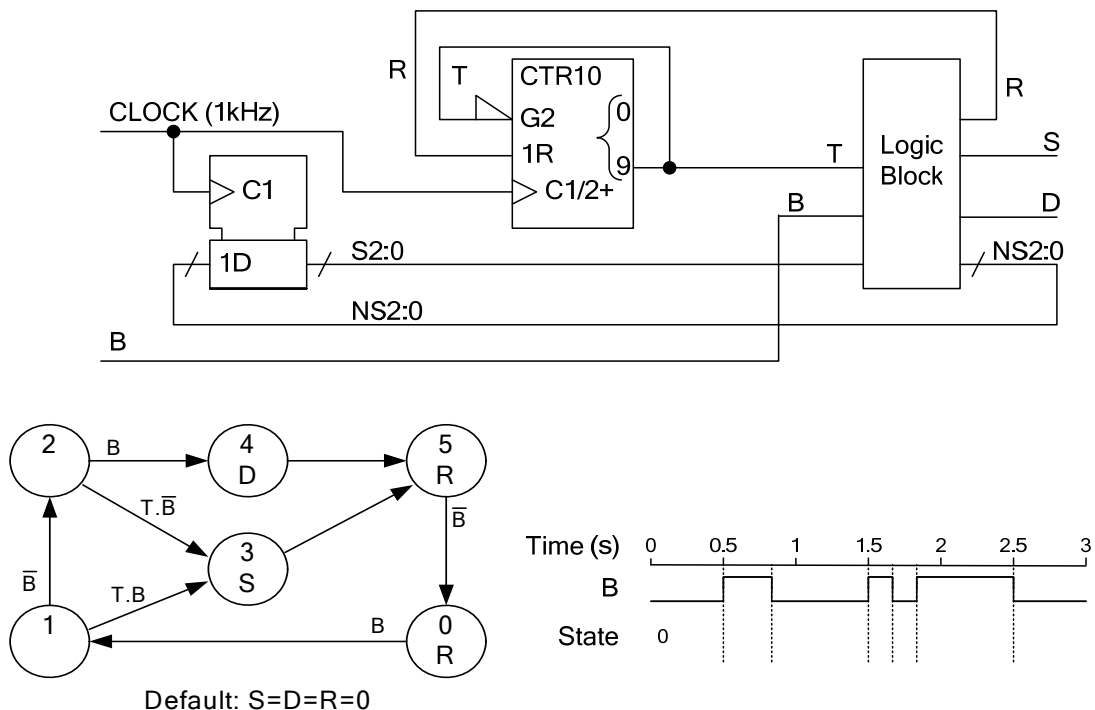

Figure 2.1

3. The circuit of *Figure 3.1* forms part of a bit-serial data transmission system. The input D is synchronized to the CLOCK and represents the sequence of bits to be transmitted. The outputs POS and NEG cause positive and negative pulses to be transmitted respectively. The 2-bit counter labelled CTR2 increments on each rising edge of CLOCK unless D is high in which case it resets to zero. The counter outputs and register outputs are all initially zero as shown in the timing diagram.

(a) Explain why the counter does not increment to 1 until cycle 4 of the diagram and show its value in the remaining clock cycles. [6]

(b) Explain the circumstances under which L changes state and complete its waveform for the remaining clock cycles. [7]

(c) Draw the waveform of G and hence draw the waveforms of POS and NEG for all the remaining clock cycles. [12]

(d) Explain why there will be at least one pulse on either POS or NEG every four clock cycles. [5]
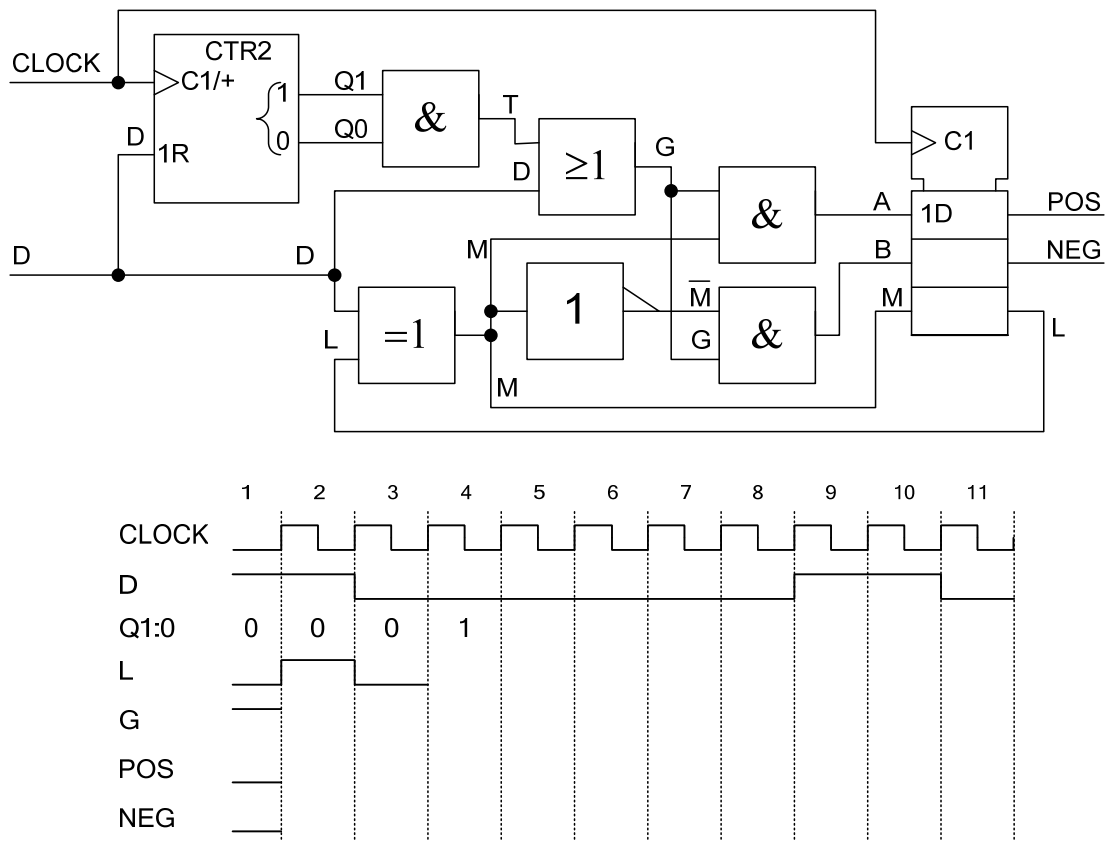

Figure 3.1

4. (a) Show that the two circuits in *Figure 4.1* calculate the same Boolean expression for Y and explain what is meant by saying that the circled pair of signals in the rightmost circuit form an "AND bundle" representation for $\overline{X}$. [4]

(b) The circuit of *Figure 4.2* includes a multiplexer whose input and output signals are "AND bundles" as shown. Show that the multiplexer can be implemented using only NAND gates and inverters with propagation delays of 2 gate delays from the SEL input and 1 gate delay from the other inputs. [8]

(c) *Figure 4.2* shows the circuit of a "carry-skip" adder which includes an n-bit full adder whose propagation delays (in gate delay units) are as follows:

Propagation delays	Output	
	C_{n-1}	S
Input C_{-1}	n	$n+3$
P	$n+1$	$n+3$

If $SEL = \overline{(P_0 \oplus Q_0) \cdot (P_1 \oplus Q_1) \cdots (P_{n-1} \oplus Q_{n-1})}$, show that $CC_{n-1} = C_{n-1}$ for any input values and construct a table of delays as above with $\overline{CC}_{n-1}$ instead of C_{n-1}. Assume that an XOR gate has a propagation delay of 2 units and that NAND gates and inverters have a delay of 1 unit. [10]

(d) Calculate the worst case delay to any S output for each of the 64-bit adder implementations given below. [8]

(i) A single 64-bit full adder whose delays are as given in part (c).

(ii) Eight copies of the circuit of *Figure 4.2* (with $n = 8$) connected as indicated in *Figure 4.3*. You may assume that the propagation delays of *Figure 4.2* are unaffected by the carry inversions required on alternate stages.
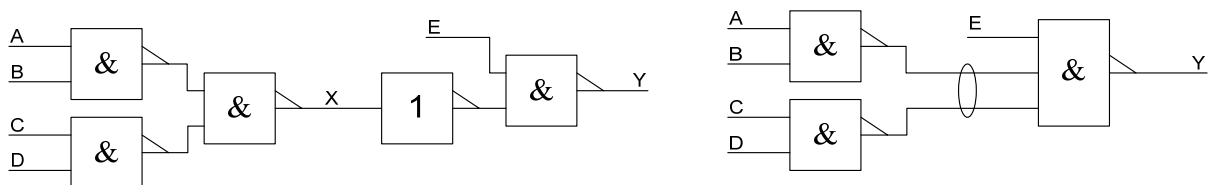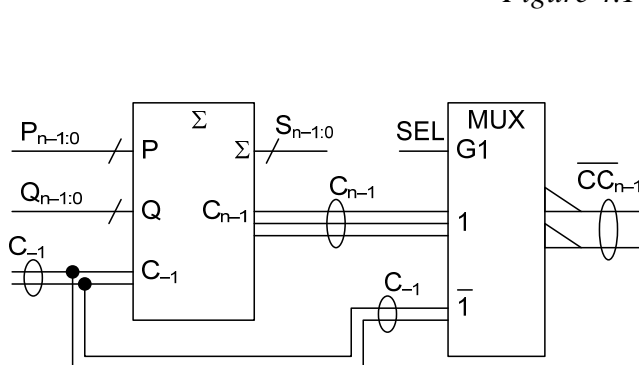

Figure 4.1
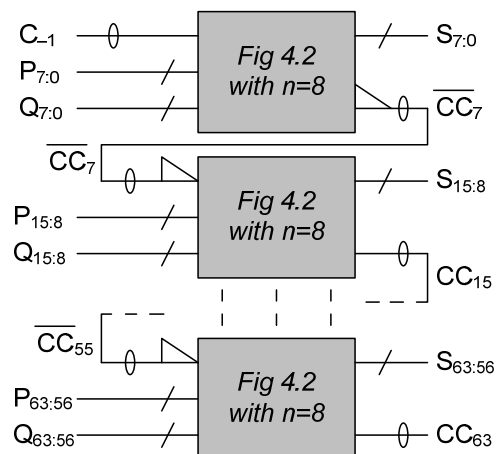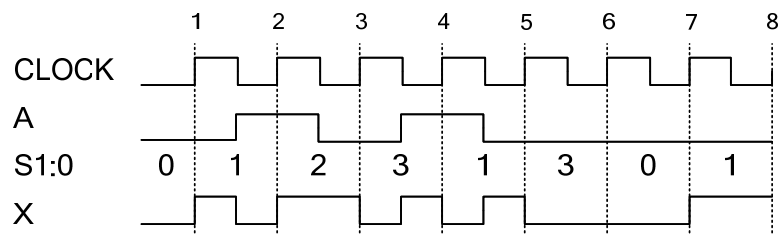

Figure 4.2

Figure 4.3

2009 E2.1/ISE2.2 Solutions

Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1.   (a)   (i)

Next State/X		A=0	A=1
State	0	1/0	1/0
	1	3/1	2/0
	2	3/1	3/1
	3	0/0	1/1

[3A]

[5A]

(b)   Taking a falling edge as the time reference, the setup equation is:

$$t_p + t_d + t_s < \tfrac{1}{2}T \quad \Rightarrow \quad 6 + 27 + 5 < \tfrac{1}{2}T \quad \Rightarrow \quad T > 76$$

The hold time equation is:

$$t_h < t_p + t_d + \tfrac{1}{2}T \quad \Rightarrow \quad 2 - 6 - 15 < \tfrac{1}{2}T \quad \Rightarrow \quad T > -38$$

[5A]

Hence $T > 76\,\text{ns} \quad \Rightarrow \quad f < 13.16\,\text{MHz}$

[3C]

(c) $\dfrac{dV}{dt} = \dfrac{I}{C} \quad \Rightarrow \quad C = \dfrac{Idt}{dV} = \dfrac{20\text{n} \times 2\mu}{10 \times \frac{1}{2} \times 2^{-14}} = \dfrac{40\text{f}}{305\mu} = 131\,\text{pF}$

[8A]

(d) (i) To multiply by 5, we calculate $x+4x$ and obtain the multiplication by 4 by shifting left by two bits: [2A]

$$\begin{array}{cccccc} X3 & X2 & X1 & X0 & 0 & 0 \\ + & & X3 & X2 & X1 & X0 \\ \hline \end{array}$$

The two LSBs of this sum do not require any logic and so we can use a 4-bit adder for the rest of the bits. Because the addition is unsigned, we can use CO as a fifth output bit.

(ii) The maximum possible value of x is 15, so the maximum value of y is $15 \times 5 = 75$ (1001011 in binary) which requires 7 bits. [2A]

(iii) The range of x is now -8 to $+7$, so the range of y is -40 to $+35$. [2A]

(iv) We need to sign-extend the Q input instead of zero-padding it. If P and Q were independent inputs, we would also need to use a full 5-bit adder. However, in this case, P and Q always have the same sign and so the CO gives the correct value for Y6. [No penalty for using a full 5-bit adder]. In fact, Y6 always equals X3 also. [2D]
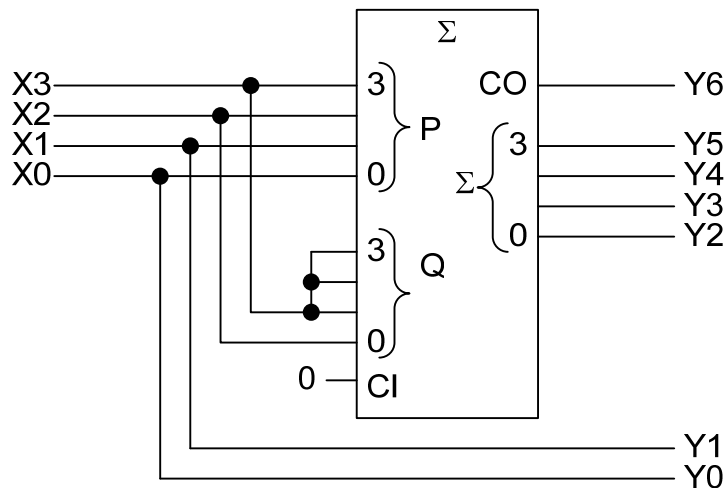

Figure 1.4

(e) (i) This expression is true for the binary range 00110000 to 00111111 which, in decimal, is 48 to 63. [4C]

(ii) The first term is true when X7=X6 and the second when X7=X5. This both terms are true iff X7=X6=X5. This is true for the binary number range 11100000 to 00011111 which, in decimal, is –32 to +31. [4C]

2. (a) When R is high, the counter will remain reset. When R goes low, the counter will start counting and when it reaches 512, Q9 (=T) will go high; this will be 0.512 seconds after R went low. Since T now is high, the count enable input (labelled G2) will be low and the counter will remain at 512 until it is reset on the clock cycle after R goes high. The counter is now held at zero until R goes low when the whole process starts again. [8A]

(b) After the first pulse the state machine remains in state 2 until T goes high 0.514 s after the start of the pulse. At this point, T goes high and the state machine goes to state 3 and emits an S pulse. In the second sequence, however, B goes high before the 0.513 s has elapsed and so the state machine goes into state 4 and emits a D pulse.

[12A]
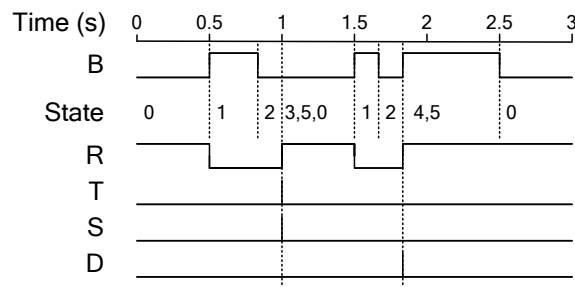
(c) If B goes high on CLOCK rising edge 0 at $t = 0.5$ s, R will go low just after edge 1 and so the counter will count to 1 after edge 2 and to 512 after edge 513. Therefore T will go high just after edge 513. The state machine will therefore enter state 3 at edge 514 causing S to go high. This therefore happens at $t = 1.014$ s. [5A]

[5D]

(d) To detect a long press, we introduce an extra state and branch to it if T goes high while we are in state 1. [Other solutions in cluding a Mealy machine are possible].


Default: S=D=R=0
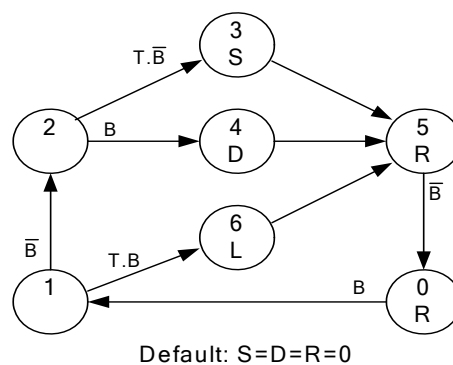
3. (a) The counter is held reset as long as D remains high. D goes low just after the CLOCK rising edge and so the counter cannot increment to 1 until the following rising edge. [6A]

(b) Since $M = L \oplus D$, L will change state at the end of any clock cycle in which D is high, i.e. at the end of cycles 1, 2, 9 and 10. [7A]

(c) G is true whenever D is true and also whenever Q1:0=3. Whenever G is high, either A or B will also be high depending on whether M is high or low. Therefore there will be a pulse on either POS or NEG during the following cycle. Since M also determines the value of L in the following cycle, L will be high during a POS pulse and low during a NEG pulse. [12A]

(d) When D is low, the counter runs and G will go high every fourth clock cycle when the counter equals 3. When D is high, then G is also forced high. Thus G can never be low for more than three consecutive clock cycles. Whenever G is high, there is a POS or NEG pulse during the next clock cycle. It follows that there can never be more than 3 consecutive clock cycles without a POS or NEG pulse. [5A]
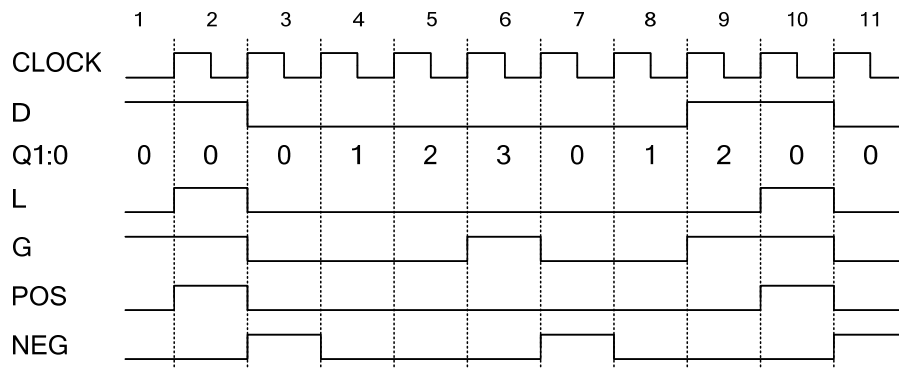
4   (a)   The central NAND gate and inverter can be merged to form an AND gate. We then have an AND gate feeding an NAND gate which is equivalent to a single 3-input NAND gate as in the rightmost circuit. Also easily shown using Boolean algebra.

           [4A]

We know, from the first circuit, that the NAND of the two circled signals is X, and so their AND is $\overline{X}$. An "AND bundle" is a group of signals whose AND represents a signal in the circuit that is significant but that is never explicitly formed.

(b)   The left circuit shows a conventional multiplexer formed from NAND gates. We can omit the final NAND gate to give an AND bundle output of $\overline{CC}_{n-1}$ and the bundled inputs just increase the number of inputs required for the other NAND gates. The delay is clearly 2 gates from the SEL input and 1 gate from the others.

           [8D]
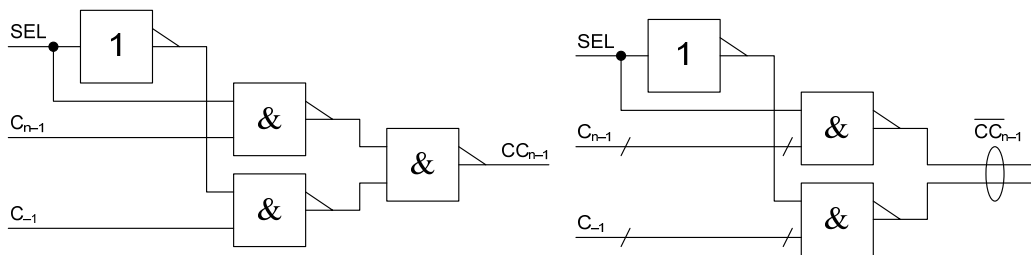
(c)   If SEL=1, then the multiplexer selects C_{n-1} as its input and so $CC_{n-1} = C_{n-1}$. SEL-0 only occurs when each of the XOR terms in the expression for SEL is true, i.e. when each column of the addition is propagating the carry. Under these circumstances, $C_{n-1} = C_{-1}$ and so $CC_{n-1} = C_{n-1}$ .is true for this case as well. The delays are now as given below:

           [10A]

Gate delays		Output	
		$\overline{CC}_{n-1}$	S
Input	C_{-1}	1	$n+3$
	P	$\max(5, n+2)$	$n+3$

The delays to S are unaffected by the addition of the multiplexer. The delay from C_{-1} to $\overline{CC}_{n-1}$ is only 1 gate, while the delay from P now has two paths: one via SEL with a delay of $2+1+2 = 5$ and one via C_{n-1} which now has an additional 1-gate delay introduced by the multiplexer.

(d)   We can calculate the delays to the S outputs by adding appropriate values from the table calculated in part (c).

(i)   From the table given in the question: delay is $64 + 3 = 67$.

           [3C]

(ii)   Worst case is P0→C7→C15→…→C55→S63 = $10 + 6\times1 + 11 = 27$

           [5C]