Paper Number(s): **E2.1**

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
EXAMINATIONS 2010

EEE/ISE PART II: MEng, BEng and ACGI

**DIGITAL ELECTRONICS 2**

Wednesday, 26 May 2:00 pm

There are FOUR questions on this paper.

Q1 is compulsory.
Answer Q1 and any two of questions 2-4.
Q1 carries 40% of the marks. Questions 2 to 4 carry equal marks (30% each).

Time allowed: 2:00 hours

**Examiners responsible:**

First Marker(s): D.M. Brookes D.M. Brookes

Second Marker(s): T.J.W. Clarke T.J.W. Clarke

**Information for Candidates:**

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) *Figure 1.1* shows the state diagram for a state machine with one input, A, and one output X. The state is represented by a 2-bit binary number in the range 0 to 3. The state changes only on the clock rising edges which are indicated by vertical dashed lines in the timing diagram.

(i) Draw the state table for the state machine. [4]

(ii) Complete the timing diagram showing the sequence of states taken and the waveform of the output X. [4]

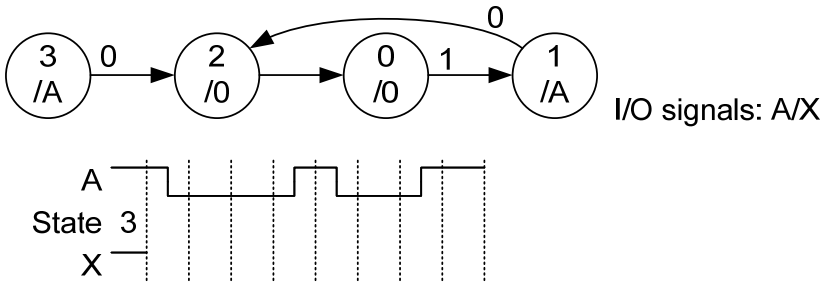



*Figure 1.1*

(b) In the circuit of *Figure 1.2*, the gates have a propagation delay $t_G$ and the flipflops have a propagation delay $t_P$ and setup/hold times of $t_S$ and $t_H$ respectively. The clock, CK, is a symmetric square wave with period $T$.

(i) Write down the setup and hold inequalities that apply to the rightmost flipflop. [4]

(ii) Calculate the maximum clock frequency for reliable circuit operation if $t_S = 3$ , $t_H = 1$ , $5 < t_P < 10$ and $2 < t_G < 4$ where all times are in nanoseconds. [4]

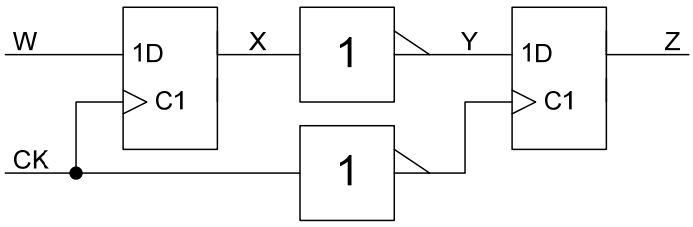
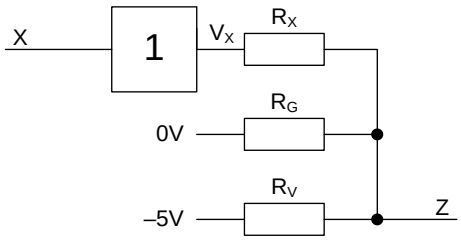



*Figure 1.2*

(c) The gate output voltage, $V_X$, in *Figure 1.3* takes the values 0 and +5 V for logic zero and logic one respectively. Select the resistor values, $R_X, R_G$ and $R_V$ so that $Z$ takes the values shown in the table and that the parallel combination of the three resistors equals 100 Ω. [8]




| X | Z |
|---|---|
| 1 | 0.5 volts |
| 0 | -0.5 volts |

*Figure 1.3*

(d) The circuit of *Figure 1.4* adds together two 3-bit unsigned numbers P2:0 and Q2:0 to give a 4-bit unsigned answer S3:0. The decimal values of P2:0, Q2:0 and S3:0 are denoted $p$, $q$ and $s$ respectively.

The propagation delays of the full adders to their S and C outputs are respectively 3 gate delays and 2 gate delays from any of their inputs.

Determine the longest propagation delay to any bit of S3:0 for each of the following cases:

(i) Initially $p = 1$ and $q = 4$; then $p$ changes to 2. [2]

(ii) Initially $p = 1$ and $q = 7$; then $p$ changes to 0. [3]

(iii) Initially $p = 1$ and $q = 6$; then $p$ changes to 2. [3]

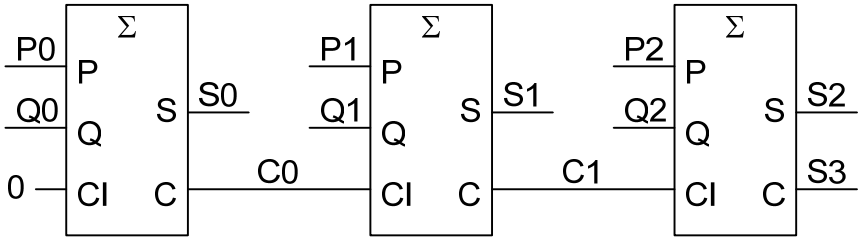



*Figure 1.4*

(e) X7:0 is an 8-bit signed number in the range –128 to +127. Give the range or ranges of values for which each of the following Boolean expressions is true:

(i) $\overline{X7} \cdot X6 \cdot X5$ [2]

(ii) $\overline{X7 \oplus X6}$ [3]

(iii) $X7 + X6$ [3]

2. The circuit of *Figure 2.1* shows a state machine together with a shift register, 3-bit binary counter and multiplexer. The purpose of the circuit is to encode a sequence of input bits at X as a sequence of 4-bit words at D3:0 with the following meanings:

| D3 | D2 | D1 | D0 | Meaning |
|---|---|---|---|---|
| 0 | a | b | c | Represents the three bits a, b, c |
| 1 | m2 | m1 | m0 | Repeat the previous bit *m* times where *m* is the 3-bit number m2:0 |

Thus an input bit sequence at X of 101 11111 010 would be encoded at D3:0 as the three words 0101, 1101 and 0010.

The state diagram is shown in *Figure 2.2*; the output V goes high for one clock cycle when a valid output word is available at D3:0. All transitions in X occur slightly after the rising edge of CK which provides the clock input for the state machine, shift register and counter.

(a) In the timing diagram shown in *Figure 2.3*, the rising edges of CK are shown by vertical dashed lines and the clock cycles have been numbered for convenience. Complete the timing diagram showing the state occupied during each cycle, the waveform of D3 and the decimal value of Q2:0 in each cycle. [18]

(b) Give the sequence of output words generated by the circuit and verify that they correctly represent the input sequence at X. [6]

(c) Explain why the circuit would not work correctly if X were high instead of low during clock cycles 11 to 15. Modify the circuit and/or the state diagram transitions so that the circuit works correctly for all input sequences. [6]

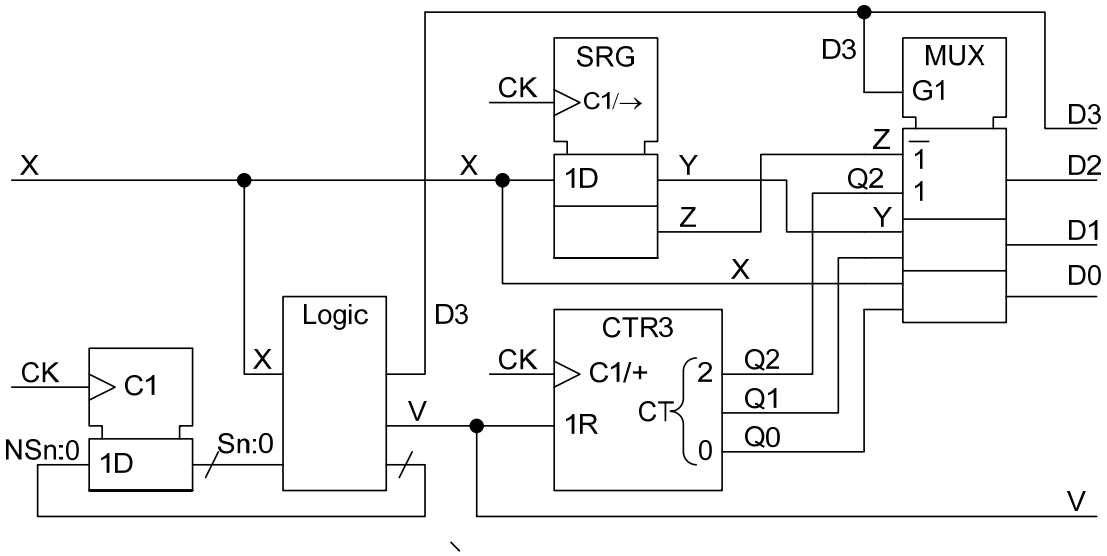



*Figure 2.1*

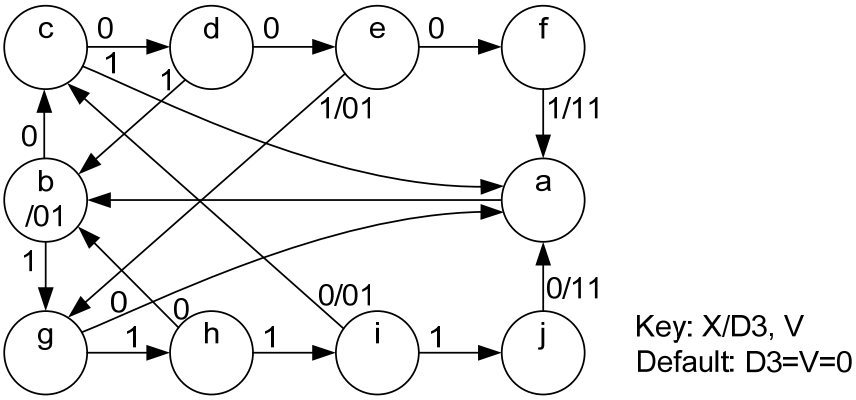



*Figure 2.2*

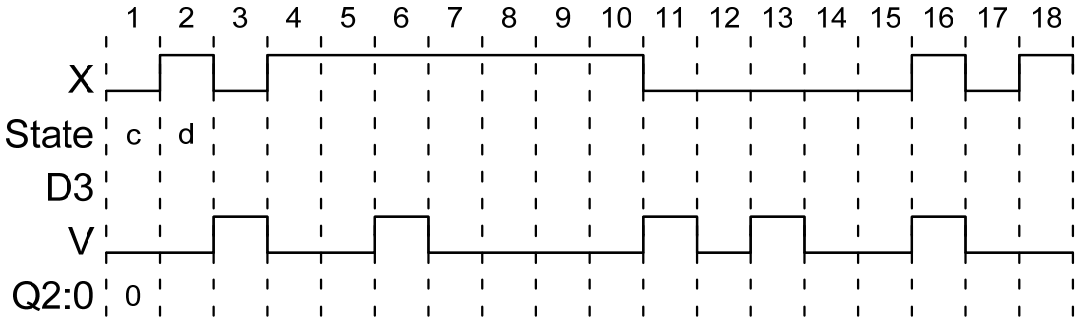



*Figure 2.3*

3. *Figure 3.1* shows part of the memory interface of a microprocessor (µP) which includes both RAM and ROM memories although the ROM is not shown on the diagram. The circuit includes a delay element whose propagation delay is $t_D$ as shown.

(a) The block marked "Decode Logic" generates chip enable signals for the RAM and ROM memory. Give Boolean expressions for RAMEN and ROMEN that are true for the hexadecimal address ranges 0000 – 9FFF and A000 – EFFF, respectively and false otherwise. [8]

(b) *Figure 3.2* shows the timing specifications of the microprocessor during a memory read cycle. Draw a timing diagram showing the signals CK, W, X, Y and OE during a read cycle. If all gates have a propagation delay of $t_G$, calculate the times of the rising and falling edges of OE relative to the rising edge of CK. Assume $t_D + t_G < t_A < ½T$. [12]

(c) *Figure 3.3* shows the timing specifications of the RAM during a read cycle. Determine the maximum and minimum values of $t_D$ that will ensure $t_S > 20$ and $20 < t_H < 40$ with the following timing values: [10]

$$T = 100 \qquad t_A = 38 \qquad t_P = 20 \qquad t_E = 10 \qquad 2 < t_F < 10 \qquad t_G = 2.$$

The solution to this question does not necessarily involve all of these values.

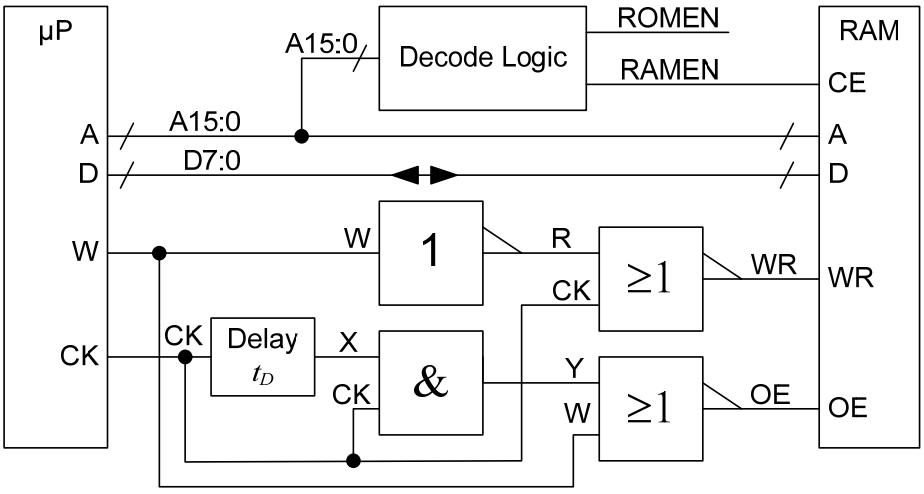



*Figure 3.1*

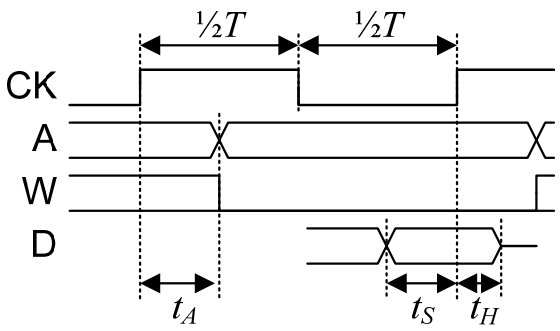



*Figure 3.2*

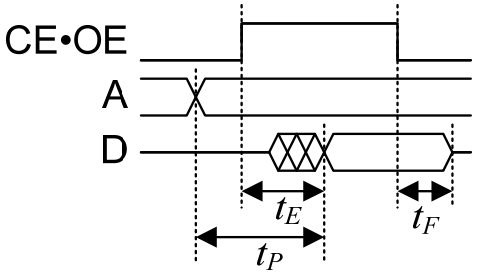



*Figure 3.3*

4. The circuit of *Figure 4.1* shows an analogue-to-digital converter (ADC) followed by a digital-to-analogue converter (DAC). The ADC input is $w = x + d$ where $x$ is the input signal and $d$ an added dither signal. The value of a least significant bit (LSB) is 1 mV and the voltage $y$ is equal to the voltage $w$ rounded to the nearest whole number of millivolts. The conversion error is defined as $e = y - x$.

   All voltages in this question are given in mV.

   (a) Suppose that $d = 0$ and $x$ is a DC value in the range $-7.5 < x < -6.5$. Show that the conversion error is given by $e = -7 - x$. [5]

   (b) Now suppose that $x$ is a DC value in the range $0 < x < 0.5$ and that $d$ is a random value in the range $-0.5 \leq d < 0.5$ with a uniform probability density function as shown in *Figure 4.2*. List the possible values that $y$ can take and give the probability of each as a function of $x$. [10]

   Calculate the mean and variance of $y$ as functions of $x$ where

$$E(y) = \sum_i i \times pr(y = i), \quad Var(y) = -\big(E(y)\big)^2 + \sum_i i^2 \times pr(y = i)$$

   (c) Now suppose that $x$ is a DC value in the range $0 < x < 0.5$ and that $d$ is a random value in the range $-1 \leq d < 1$ with a triangular probability density function as shown in *Figure 4.3*.

   (i) Show that $pr(y = -1) = \frac{1}{2}(x - 0.5)^2$ and $pr(y = +1) = \frac{1}{2}(x + 0.5)^2$. [4]

   (ii) Calculate the mean and variance of $y$ as functions of $x$. [6]

   (d) Briefly explain why dither is added to a signal before it is quantized and why the triangular dither of part (c) is preferred to the uniform dither of part (b). [5]

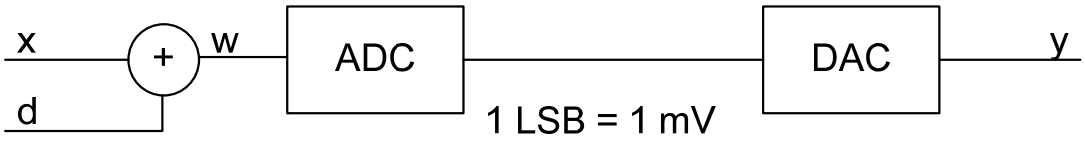



*Figure 4.1*

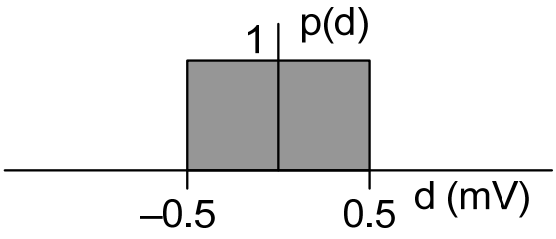



*Figure 4.2*

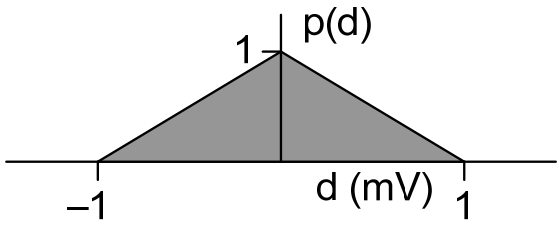



*Figure 4.3*

# 2010 Paper E2.1/ISE2.2: Digital Electronics II- Solutions

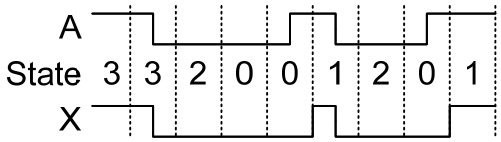
Key to letters on mark scheme: B=Bookwork, C=New computed example, A=Analysis of new circuit, D=design of new circuit

1. (a) (i) The state table is: [4A]

| | NS1:0/X | A=0 | A=1 |
|---|---|---|---|
| S1:0 | 00 | 00/0 | 01/0 |
| | 01 | 10/0 | 01/1 |
| | 11 | 10/0 | 11/1 |
| | 10 | 00/0 | 00/0 |

*Mostly well done. The commonest mistake was to put /A in the state table instead of /0 or /1.*

(ii) The timing diagram is: [4A]




*The commonest mistake was to extend the X pulses to the next rising edge of the clock whereas, in fact it respons immediately to a change in A.*

(b) (i) Setup: $t_P + t_{G1} + t_S < \frac{1}{2}T + t_{G2}$

Hold: $\frac{1}{2}T + t_{G2} + t_H < T + t_P + t_{G1}$ [4A]

*Note that the $t_G$ delays cannot be cancelled because they correspond to different gates. Also, because of the inverter in the CLOCK signal to the second flipflop, the equations both involve $\frac{1}{2}T$. These were the two commonest errors. Several people omitted the delay in the clock path, $t_{G2}$.*

(ii) Setup: $\frac{1}{2}T > t_P + t_{G1} + t_S - t_{G2} = 10 + 4 + 3 - 2 = 15$ ns

Hold: $\frac{1}{2}T > t_{G2} + t_H - t_P - t_{G1} = 4 + 1 - 5 - 2 = -2$ ns

Hence $T > 30$ ns $\Rightarrow$ $f_{CK} < 33$ MHz [4A]

*Several people failed to verify that the hold inequality was satisfied. Several people made algebraic errors: most commonly getting signs wrong.*

(c) Applying Kirchoff's current law at node Z gives: [3A]

$$Z = \frac{V_X R_X^{-1} \ - 5R_V^{-1}}{R_X^{-1} + R_G^{-1} + R_V^{-1}}$$

However, we know that the parallel combination of the resistors is 100 Ω, so the denominator equals 10 mS. Substituting for the given values of Z gives:

$$5R_X^{-1} - 5R_V^{-1} = 5 \text{ m}$$

$$-5R_V^{-1} = -5 \text{ m}$$

$$R_X^{-1} + R_G^{-1} + R_V^{-1} = 10 \text{ m}$$

From which we get $R_V = 1$ kΩ, $R_X = 500$ Ω and $R_G = 143$ Ω. [5D]

*This question (like any involving parallel impedances) is much easy to solve using conductances as above. Several people used resistances directly and got lost in complicated algebra. Several took $V_X = 1$ instead of $V_X = 5$ when $X = 1$ which makes a solution impossible. There were quite a lot of sign errors made in the algebra. Several people weirdly assumed that the three currents exiting node Z were all equal (rather than that they sum to zero as KCL says). Several others half remembered a KCL-like formula wrongly. Generally far more algebra than was actually needed. A very few wisely used the simultaneous equation function on the calculator.*

(d) (i) *s* changes from 5 to 6 (0101 to 0110). All the carry signals remain at 0 throughout, so the delay is just 3 gate delays. [2A]

(ii) *s* changes from 8 to 7 (1000 to 0111). The longest delay path is P0-C0-C1-S2 which has a total delay of 7 gate delays. [3A]

(iii) *s* changes from 7 to 8 (0111 to 1000). The longest delay path is P1-C1-S2 which has a total delay of 5 gate delays. [3A]

*Several people didn't understand that propagation delay is the time delay from when p changes to when S3: 0 becomes stable. So the "initial conditions" are necessary to give the starting situation: they don't themselves have a propagation delay. The longest delay in parts (ii) and (iii) is to S2 rather than to S3. The propagation delay applies just as much when the carry changes from 1 to 0 (as in part (ii)) as when it changes from 0 to 1.*

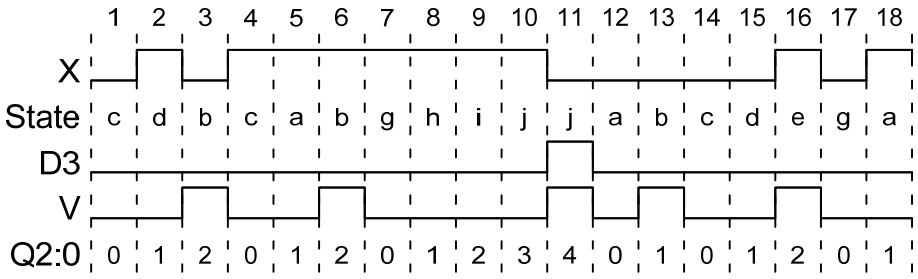
(e) (i) 96 to 127 [2A]

(ii) –64 to +63 [3A]

(iii) –128 to –1 and also 64 to 127 [3A]

*Several treated the expression in part (ii) as an XOR rather than an XNOR.*

2. (a) The completed timing diagram is: [18A]

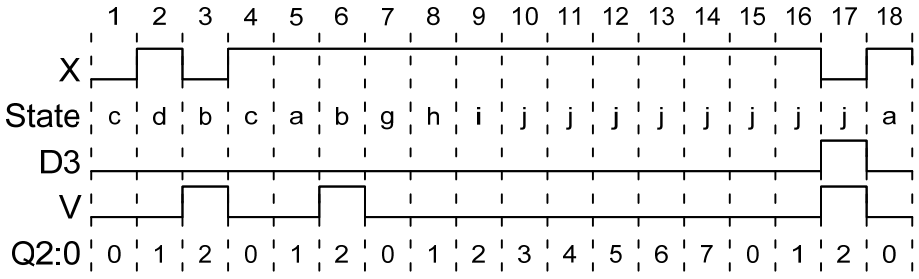



*Most people got this correct. A strangely common error was to set Q2:0=0 instead of 4 in cycle 11. Several did not recognise that it was a synchronous reset and so set Q2:0=0 in the same cycle as V=1 rather than in the following one. Some did not realise that "1R" means the counter reset is synchronous. A few people though V was a count enable rather than a reset. Another strange error was to make D3 the same as X or else always the inverse of V.*

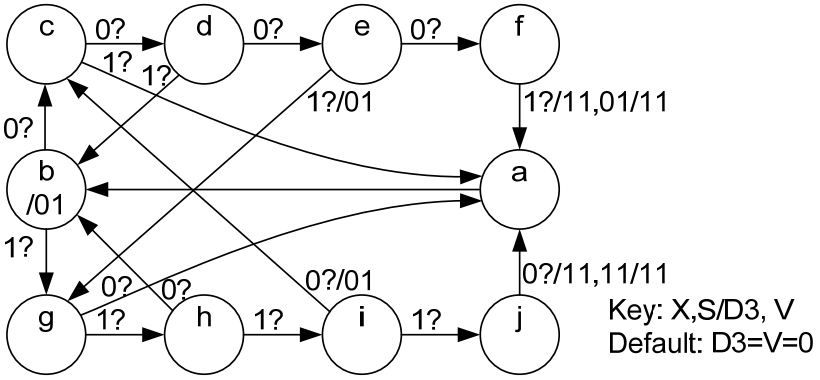
(b) Output words are generated when V=1 in cycles 3, 6, 11, 13 and 16. When D3=0 the mux selects the shift register ouputs and so D2:0 equals the last three bits of X (with D0 equal to the current value of X). When D3=1 (only in cycle 11) D2:0=Q2:0 which is 4 in this case. The output words are therefore 0010 0111 1100 0000 0001. These correctly correspond to the bit sequences 010 111 1111 000 001 (where spaces delimit the bits corresponding to each word). [6A]

*Several people got completely the wrong output words (e.g. 0101 as the first word, perhaps from the example given in the question). Quite a few people didn't realise that the output words are generated only when V=1.*

(c) If X remains high, the circuit will remain in state j and the counter will wrap around. This means that the repetition count will be 8 too low. [3A]

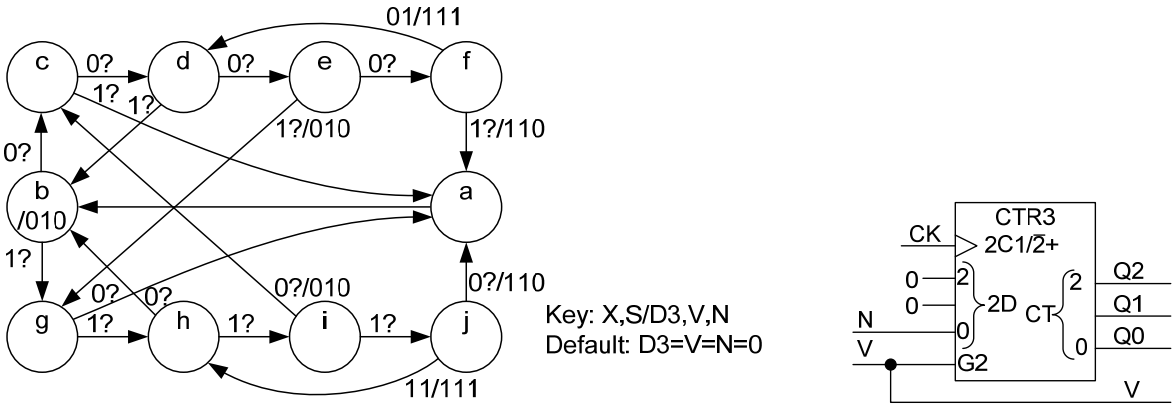



To avoid this, we need to detect when the counter equals 7 in states f or j and force an output word. We therefore define an additional state machine input $S = Q2 \cdot Q1 \cdot Q0$ and modify the state diagram as follows: [3D]

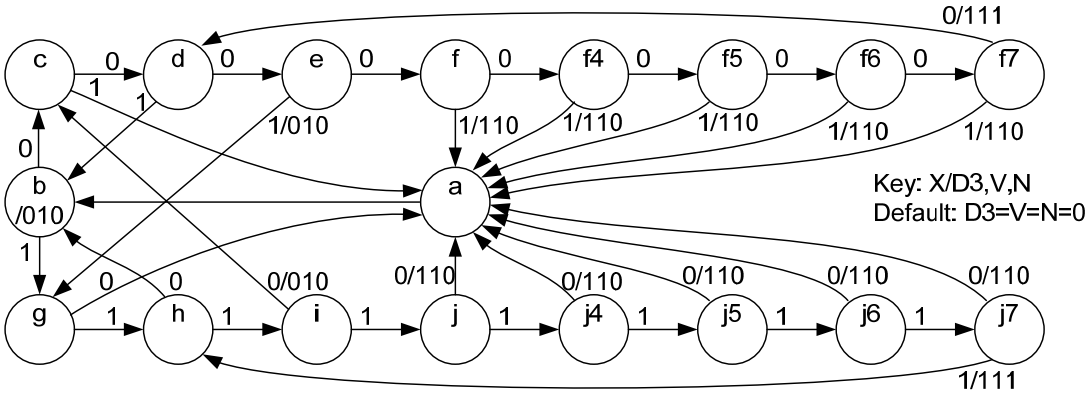


This is rather wasteful because a long run of 1's will result in 0111 1111 0111 etc.

If we want to make the encoding more efficient, we either have to define 1000 as meaning "repeat the previous bit 8 times" or else output 1111 every seven cycles within a long run of 1's. To make the counter divide by 7, we must either reset it when it reaches 6 (but force D2:0=7 in the next cycle) or else reset it to 1 instead of 0.




Instead of detecting Q2:0=7 externally, another possibility is to use extra states to count how many consecutive 1's or 0's we have had.




[Note that the lowest possible repetition count is 3 so we can improve the transmission efficiency if the receiver treats count of 0,1,2 as 8,9,10. In this case we would need a 4-bit counter and would need to detect counts of 10 instead of 7 in states f and j.]

3. (a) There are many possible equivalent expressions:

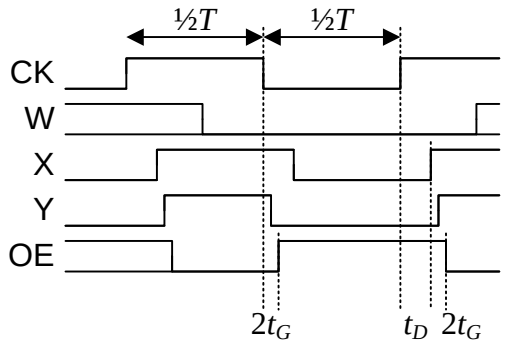
$$RAMEN = \overline{A15} + \overline{A14} \cdot \overline{A13} = \overline{A15 \cdot (A14 + A13)} = \overline{A15 \cdot A14} \cdot \overline{A15 \cdot A13}$$

$$ROMEN = A15 \cdot \big((A14 \oplus \mathrm{A13}) + A14 \cdot \overline{A12}\big) = A15 \cdot \big((A14 \oplus \mathrm{A13}) + A13 \cdot \overline{A12}\big)$$

$$= A15 \cdot (\overline{A14} \cdot A13 + A14 \cdot \overline{A13 \cdot A12})$$ [8D]

*Surprisingly badly done. Many people just encoded the two ends of the range without ensuring that the expressions were valid in between. The most reliable method by far was to use a K-map with the four most significant address bits as the inputs.*

(b) X is the same as CK but delayed by $t_D$. The effect of the delay element and the following AND gate is that Y goes low one gate delay after the CK goes low but takes an extra $t_D$ to go high when the CK goes high again. [12A]




Thus OE goes high at $\frac{1}{2}T + 2t_G$ and goes low at $[T] + t_D + 2t_G$.

*An easy question that was mostly well done. Several people lost marks because they did not give expressions for the rise and fall times of OE as requested. Others lost marks because their timing diagram stopped before the second CK rising edge and did not show the full cycle.*

(c) As seen in the previous part, the delay element only affects the falling edge of OE. Therefore it will only be involved in the $t_H$ requirement of the microprocessor. [10A]

$$20 < t_H < 40 \Leftrightarrow 20 < t_D + 2t_G + t_F < 40 \Leftrightarrow 14 < \mathrm{t_D} < 26$$

The setup equations constrain $T$ but do not involve $t_D$ and are:

$$t_A + t_P + t_S < T \Rightarrow T > 78$$

$$, \quad \tfrac{1}{2}T + 2t_G + t_E + t_S < T \Rightarrow T > 76$$

*On the whole, this part was done very poorly. Several people tried wrongly to combine these two constraints into something involving $t_P - t_E$ which is completely wrong. Like many memory circuits, there is a maximum hold time as well as the more usual minimum hold time; thus $20 < t_H < 40$ means that $t_H > 20$ and $t_H < 40$ are two separate requirements. Quite a number of people thought that data was clocked into the microprocessor on the falling edge of OE.*

*The original question did not make it clear that D must go tristate after $t_H$.*

4. (a) If $d = 0$, then for $-7.5 < x < -6.5$ $y$ will always equal $-7$ since $y = \mathrm{rnd}(w) = \mathrm{rnd}(x) = -7$.

Hence $e = y - x = -7 - x$. [5A]

*An easy question that almost everyone got right.*

(b) Since $0 < x < 0.5$, we know that $-0.5 < w < 1$ and so $y = 0$ or 1.

We can see that $pr(d < q) = q + 0.5$ for $-0.5 \leq q \leq 0.5$.

We can calculate the probabilities as:

$pr(y = 0) = pr(w < 0.5) = pr(d + x < 0.5) = pr(d < 0.5 - x) = 1 - x.$

Also $pr(y = 1) = 1 - pr(y = 0) = x$. [4C]

*Many people wrongly said $-0.5 \leq w < 1$ although even then $pr(w = 0.5) = 0$. Quite badly done: often the probabilities did not even sum to 1.*

Hence: $E(y) = 0 \times pr(y = 0) + 1 \times pr(y = 1) = x$

and $Var(y) = -x^2 + 1 \times pr(y = 1) = \text{x} - \text{x\^2}$ [6C]

(c) Since $0 < x < 0.5$, we know that $-1 < w < 1.5$ and so $y = -1, 0$ or $+1$. $y$ can only equal $-1$ if $d < -0.5 - x < 0$. Similarly $y$ can only equal $+1$ if $d > 0.5 - x > 0$.

For $-1 < q < 0$, we have $pr(d < q) = \frac{1}{2}(q + 1)^2$ and for $0 < q < 1$, we have $pr(d > q) = \frac{1}{2}(q - 1)^2$ . These are the integrals of little triangular regions of the dither pdf.

So, $pr(y = -1) = pr(d < -0.5 - x) = \frac{1}{2}(0.5 - x)^2 = \frac{1}{2}(x - 0.5)^2$.

Also, $pr(y = 1) = pr(d > 0.5 - x) = \frac{1}{2}(-0.5 - x)^2 = \frac{1}{2}(x + 0.5)^2$ [4C]

Hence $pr(y = 0) = 1 - \frac{1}{2}(x - 0.5)^2 - \frac{1}{2}(x + 0.5)^2 = 0.75 - x^2$

Hence $E(y) = pr(y = 1) - pr(y = -1) = \frac{1}{2}(x + 0.5)^2 - \frac{1}{2}(x - 0.5)^2 = x$

and $Var(y) = -x^2 + pr(y = 1) + pr(y = -1) = 1 - x^2 - pr(y = 0) = 0.25$ [6C]

(d) Quantizing a low amplitude signal results in a quantization error that is strongly correlated with the signal as seen in part (a). By adding dither, we can ensure that the average quantization error is zero (i.e. $E(y) = x$ as in parts (b) and (c)) and is uncorrelated with the signal. With rectangular dither, however the variance of the quantization error is signal dependent as in part (b) but with triangular dither the variance too is independent of $x$. [5B]

*Several people interpreted the first part of this to mean "why is dither added before quantization rather that afterwards" instead of "why is dither added before quantization rather that not adding it at all".*