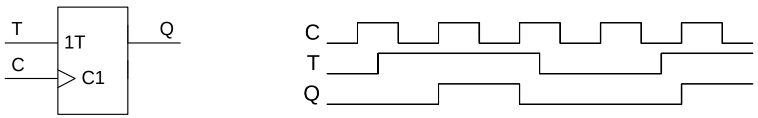
E2.11/ISE2.22 – Digital Electronics II

Problem Sheet 2

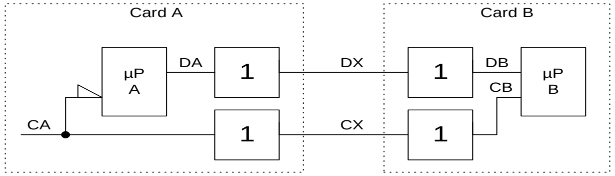
(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. A toggle flipflop (T-flipflop) changes state whenever its T input is high on the CLOCK ↑ edge as shown in the timing diagram.

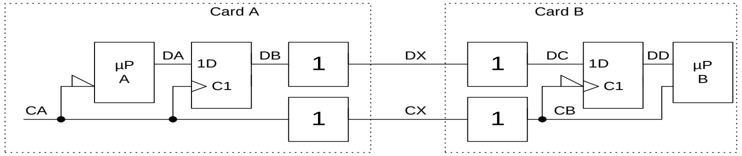


Show how a T-flipflop can be made by combining an XOR gate with a D-flipflop.

2C. A multi-processor system contains two microprocessors which are mounted on separate printed circuit cards. The clock and data signals pass through a line driver when they leave one card and a line receiver when they pass onto the next. The combined delay of the driver+receiver may vary between 13 ns and 22 ns. New data values appear at DA on the falling edge of CA with a propagation delay of 5 to 50 ns. Data is clocked into µP B on the rising edge of CB with a setup time of 12 ns and a hold time of 27 ns. If the clock, CA, is a symmetrical squarewave, calculate its maximum frequency.

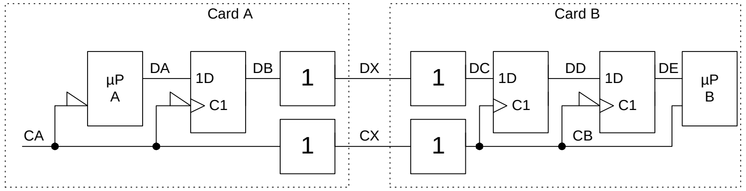


3C. We can speed up the circuit from the previous question by using high-speed flipflops with shorter propagation delays and setup times. The flipflops in the revised circuit have setup and hold times of 5 ns and 3 ns and propagation delays in the range 2 to 10 ns. Note that the second flipflop has an inverted clock. Calculate the new maximum clock frequency by considering its minimum period for each of µPA→flipflop, flipflop→flipflop and flipflop→µPB.



4C. By considering the Hold requirements, explain why the circuit in question 3 would not work if the two flipflops were interchanged.

5D. If we add a third flipflop, we can improve the speed further. Calculate the maximum clock frequency for the following circuit and explain in words how it has achieved the performance increase when compared with the original circuit of question 2.



6A. Explain why most memory integrated circuits have “tri-state” data output pins.

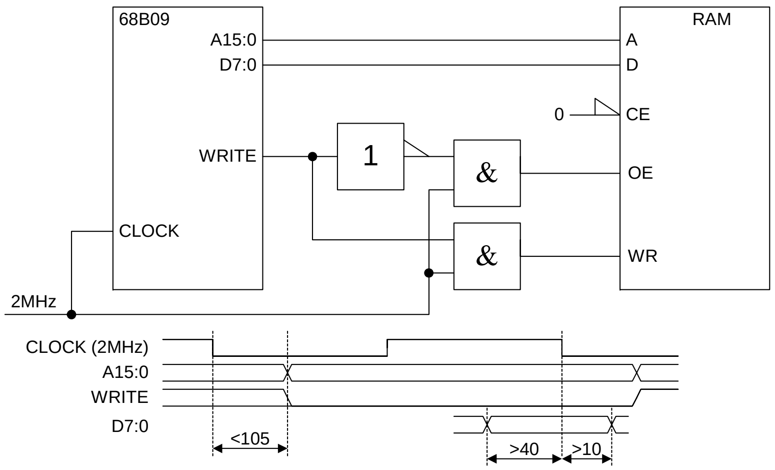
7B. In an 8-bit microprocessor system, addresses 0000 to 9FFF are occupied by RAM and addresses A000 to DFFF are occupied by ROM. The system also contains two peripheral devices: a serial port occupying addresses E100 to E107 and a parallel port occupying addresses E200 to E201. You have a supply of 8k×8 RAM integrated circuits and a supply of 16k×8 ROM integrated circuits.

a) State how many input address pins you would expect to find on each of the RAM integrated circuits, ecah of the ROM integrated circuits and on each of the peripheral device integrated circuits.

b) Derive Boolean expressions for the CE inputs of each memory and peripheral integrated circuit.

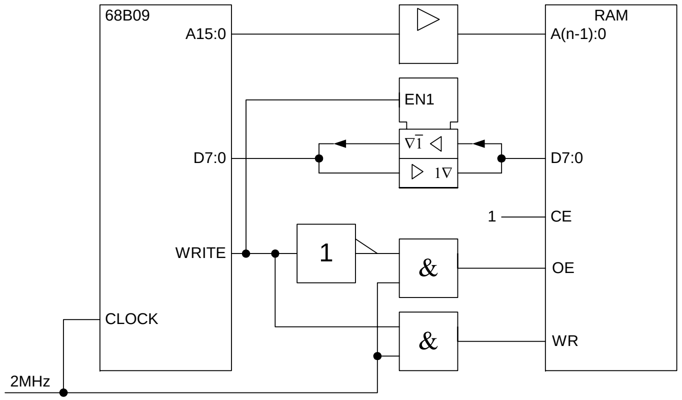
c) Say what is unusual about the byte ordering within the ROM.

8B. The diagram shows a Motorola 68B09 microprocessor connected to a memory circuit together with the timing diagram for a microprocessor read cycle..



Each logic gate has a propagation delay that may vary independently in the range 5 to 10 ns. Calculate the maximum permissible access times of the memory from (a) its address inputs, and (b) its OE input.

9C. The circuit of question 8 is altered by the introduction of buffers in the address lines and bi-directional buffers in the data lines.



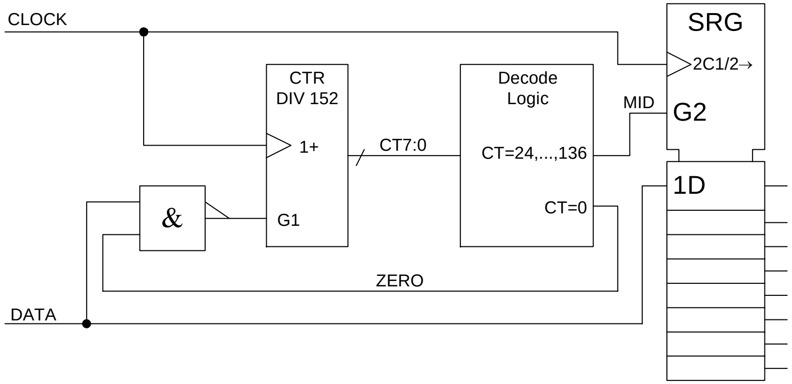
The address line buffers have a propagation delay of <18 ns while the data line buffers have a propagation delay of <12 ns, an enable time of <40 ns and a disable time of <25ns. The enable time applies when an output changes from a high impedance state to a driven state, the disable time applies when an output changes from a driven state to a high impedance state.

Calculate the new values of the maximum permissible access times of the memory from (a) its address inputs, and (b) its OE input.

10A. Explain why a bi-directional buffer is normally designed to have a longer enable time than disable time.

11D. Buffers for address and data lines can be made faster if they have inverted outputs. Say how the operation of a microprocessor is affected if the address and data lines pass through inverting buffers between the microprocessor and (a) read-write RAM memory and (b) read-only ROM memory.

12B. Asynchronous bit serial data consisting of a start bit (logical 0), 8 data bits and a stop bit (logical 1) is received by the circuit below. The CLOCK frequency is 16× the transmission bit rate. Give a Boolean expression for the signal MID; simplify it where possible.



13C. In question 12, the CLOCK frequency is changed to 4× the transmission bit rate. Determine the appropriate counter division ratio and the counter values for which MID should now be high. Determine the clock accuracy required by the transmitter and receiver to ensure that the data is received correctly.

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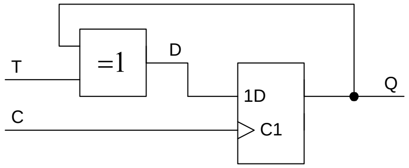
Solution Sheet 2

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. As seen in problem sheet 1, an XOR gate can be used to invert a signal or pass it through unchanged according to whether a control input is high or low.



2C. We define $t=0$ as the falling edge of CA.

Setup requirement: $\max(DB\uparrow\downarrow)+12 < \min(CB\uparrow)$
$50+22+12 <(13 + \frac{1}{2}T)$
$\frac{1}{2}T > 71 \Rightarrow f < 7$ MHz

Hold requirement: $\max(CB\uparrow) + 27 > \min(T + DB\uparrow\downarrow)$
$\frac{1}{2}T+22 + 27 > T + 5+13$
$\frac{1}{2}T > 31$ (less severe restriction than above)

Note the extra T term in the hold requirement: this is because we want the *second* transition of DB to occur >27 ns after CB↑. The Hold requirement is so easily satisfied that it wouldn't normally be necessary to calculate it exactly.

3C.

µPA →	Setup:	$\max(DA\uparrow\downarrow) +5 < \min(CA\uparrow)$	Hold:	$\max(CA\uparrow)+3< \min(T+DA\uparrow\downarrow)$
flipflop		$50+5 < \frac{1}{2}T$		$\frac{1}{2}T+3< T + 5$
CA↓=0		$\frac{1}{2}T > 55 \Rightarrow$ **$f < 9$ MHz**		$\frac{1}{2}T > -2$ ☑
flipflop →	Setup:	$\max(DB\uparrow\downarrow)+5 < \min(CB\downarrow)$	Hold:	$\max(CB\downarrow)+3< \min(T+DB\uparrow\downarrow)$
flipflop		$10+22+5 < \frac{1}{2}T+13$		$\frac{1}{2}T+22+3< T +2+13$
CA↑=0		$\frac{1}{2}T > 24 \Rightarrow f < 21$ MHz		$\frac{1}{2}T > 10 \Rightarrow f < 50$ MHz
flipflop →	Setup:	$\max(FB\uparrow\downarrow)+12<\min(CB\uparrow)$	Hold:	$\max(CB\uparrow)+27<\min(T+FB\uparrow\downarrow)$
µPB		$10+12<\frac{1}{2}T$		$\frac{1}{2}T+27<T + 2$
CB↓=0		$\frac{1}{2}T > 22 \Rightarrow f < 23$ MHz		$\frac{1}{2}T > 25 \Rightarrow f < 20$ MHz

It can be seen that the critical figure is the setup time for the first flipflop: this is because the microprocessor takes such a long time (up to 50 ns) to output its data. Question 4 (which doesn't work) and question 5 (which does) show how to relax this constraint. In the third row of the previous table, I have cancelled out the delay of the clock line driver/receiver from the two sides of the inequality. This is only valid if we can assume that the propagation delays for rising and falling edges are the same (not generally true).

4C. The first flipflop now responds to a falling clock edge: this means that µPA now has a full clock cycle to output its data rather than only a half cycle. We have therefore doubled maximum clock frequency of the circuit. (Note that the middle row of this table is unchanged from the previous question).

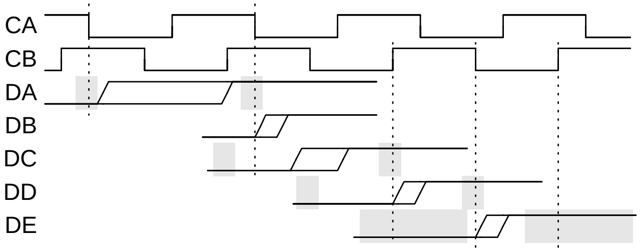
The problem is that the output from the second flipflop now changes on the rising clock edge and therefore fails to meet the hold time of µPB.

µPA → flipflop	Setup:	$\max(DA\uparrow\downarrow)+5<\min(T+CA\downarrow)$	Hold:	$\max(CA\downarrow)+3<\min(DA\uparrow\downarrow)$
CA↓=0		$50+5<T$		$0+3<5$ ☑
		$T > 55 \Rightarrow$ **$f < 18$ MHz**		
flipflop →	Setup:	$\max(DC\uparrow\downarrow)+5<\min(CB\uparrow)$	Hold:	$\max(CB\uparrow)+3<\min(T+DC\uparrow\downarrow)$
flipflop		$10+22+5 < \frac{1}{2}T+13$		$\frac{1}{2}T+22+3<T + 2+13$
CA↓=0		$\frac{1}{2}T > 24 \Rightarrow f < 21$ MHz		$\frac{1}{2}T > 10 \Rightarrow f < 50$ MHz
flipflop → µPB	Setup:	$\max(DD\uparrow\downarrow)+12<\min(T+CB\uparrow)$	Hold:	$\max(CB\uparrow)+27<\min(DD\uparrow\downarrow)$
CB↑=0		$10+12<T$		**$2 > 27$** ☒
		$T > 22 \Rightarrow f < 46$ MHz		

5D. We can fix the hold problem by adding a third flipflop. The last row of the previous table is now replaced by the two rows below and the maximum frequency is now 18 MHz.

flipflop →	Setup:	$\max(DD\uparrow\downarrow)+5<\min(CB\downarrow)$	Hold:	$\max(CB\downarrow)+3<\min(T+DD\uparrow\downarrow)$
flipflop		$10+5<\frac{1}{2}T$		$\frac{1}{2}T+3<T + 2$
CB↑=0		$\frac{1}{2}T > 15 \Rightarrow f < 33$ MHz		$\frac{1}{2}T > 1 \Rightarrow f < 500$ MHz
flipflop → µPB	Setup:	$\max(DE\uparrow\downarrow)+12<\min(CB\uparrow)$	Hold:	$\max(CB\uparrow)+27<\min(T+DE\uparrow\downarrow)$
CB↓=0		$10+12<\frac{1}{2}T$		$\frac{1}{2}T+27<T + 2$
		$\frac{1}{2}T > 22 \Rightarrow f < 23$ MHz		$\frac{1}{2}T > 25 \Rightarrow f < 20$ MHz

The timing of this circuit with a clock period of about 60 ns (16.7 MHz) is shown below with setup/hold windows shaded:



6A. Two reasons. Firstly many memories, though not all, use the same pins for data input as for data output: the outputs must therefore be turned off (or “tristated”) to allow new data to be written into a memory location. Secondly, a large memory system contains several memory integrated circuits which are enabled one at a time according to the address range selected (as in question 7 below). The use of tri-state outputs allows all memory data lines to be connected together without the need for an external multiplexer to switch between them.

7B. a) RAM has 13 address inputs, ROM has 14, Serial Port has 3 and Parallel Port has 1.

b) We need 5 RAM chips and one ROM, serial and parallel chips. The CE inputs are given in the following table:

Chip	**Address Range**	**CE**
RAM	0000 – 1FFF	$\overline{A15}\cdot\overline{A14}\cdot\overline{A13}$
	2000 – 3FFF	$\overline{A15}\cdot\overline{A14}\cdot A13$
	4000 – 5FFF	$\overline{A15}\cdot A14\cdot\overline{A13}$
	6000 – 7FFF	$\overline{A15}\cdot A14\cdot A13$
	8000 – 9FFF	$A15\cdot\overline{A14}\cdot\overline{A13}$
ROM	A000 – DFFF	$A15\cdot\left(\overline{A14}\cdot A13+A14\cdot\overline{A13}\right)$
Serial	E100 – E107	$A15\cdot A14\cdot A13\cdot A8$
Parallel	E200 – E201	$A15\cdot A14\cdot A13\cdot A9$

Note that I have not included all the address lines needed to fully decode the Serial and Parallel port adress ranges. The microprocessor should never access the undefined memory locations in the range E000 to FFFF so it does not matter if the peripheral ports respond to several of them. As defined above, the following addresses will all refer to the serial port’s lowest location: E100, E108, E110, E118, …, FFF8. Of the 16 address lines, 3 are direct inputs to the serial port, 4 are used in forming its CE and 9 are unused. The 9 unused lines can take on 512 possible values and so the serial port will appear 512 times in the memory map. If a PAL is being used to generate the CE signals, then the number of PAL inputs required may be reduced by not decoding peripheral address ranges fully.

c) The bytes are in the wrong order in the ROM. The ROM has 14 address inputs, namely A13:0. Addresses A000 to BFFF have A13=1 and will therefore be mapped to the second half of the ROM; addresses C000 to DFFF have A13=0 and will be mapped to the first half of the ROM. This situation could be corrected by inverting A13 before connecting it to the ROM but this would add delay: a neater solution is to use A14 as the most significant address bit rather than A13.

8B. Note that only the setup time matters for this question. Let A be the access time (or propagation delay) from the address inputs and E be the access time from the OE input. The clock period is 500 ns. P is the propagation delay of a gate (i.e. 5 to 10 ns)

max(105+A)+40<500 ⇒ **A < 355 ns**
max(P+E)+40<250 ⇒ **E < 200 ns** (taking P=10, its maximum value)

9C. We now have three possible paths to consider:

A15:0→Mem→D7:0	max(105+18+A+12)+40<500 ⇒ **A < 325 ns**
CLOCK↑→Mem:OE→D7:0	max(P+E+12)+40<250 ⇒ **E < 188 ns**
WRITE→Buff:EN1→D7:0	max(105+40)+40<500 ⇒ **185>500** ☑

Note that in the symbol for the bidirectional buffer: the ∇ denotes tristate outputs: the output marked with a 1 is enabled when EN1 is high while the output marked with a $\overline{1}$ is enabled when EN1 is low. The ∇ always goes immediately next to the output pin. The symbol ▹ denotes a buffer: a gate with a higher than normal output current capability. Any signals that flow right to left instead of the more normal left to right must be marked with a 🡐.

10A. If the same wire is driven high by the output of one device and low by that of another, a high current will flow which will waste power and which may even damage the integrated circuits involved. To reduce the possibility of two devices trying to drive the same wire simultaneously, tristate outputs are almost always designed to turn off more quickly than they turn on.

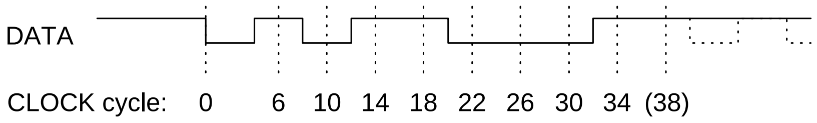
11D. The effect of inverting the address lines is to subtract them from FFFF. Thus what were memory locations 0000, 0001 and 0002 now become FFFF, FFFE and FFFD. Providing the chip enables are generated correctly, this reversal does not matter at all for a RAM: as long as each distinct address refers to a unique memory location the microprocessor does not care where it is inside the chip. For a ROM, the contents must be preprogrammed in the correct locations: thus the program would need to be stored backwards.

12B. The counter counts up from 0 to 151.

MID=CT3•!CT2•!CT1•!CT0 will get all odd multiples of 8, i.e. 8, 24, …, 136.

To eliminate the first of these we make MID=(CT7+CT6+CT5+CT4)•CT3•!CT2•!CT1•!CT0

13C. The counter should now divide by 38:



The eighth bit will now be clocked in at the end of the clock cycle in which CT5:0 equals 34. This is at time 34P+t from the beginning of the START bit where 0<t<P and P is the receiver clock period. This time must be in the range 8T to 9T where T is the duration of a bit cell. Thus

$$8T<34P+0 \Rightarrow T/P<4.25$$
$$9T>34P+P \Rightarrow T/P>3.89$$

If we assume that T and P have nominal values of T_0 and P_0 with a fractional tolerance of $\pm x$, we have

$$T_0\,(1-x) < T < T_0\,(1+x) \quad \text{and} \quad P_0\,(1-x) < P < P_0\,(1+x)$$

By considering the maximum and minimum possible values of the ratio T/P, we get:

$$\frac{T_0(1+x)}{P_0(1-x)} = 4.25 \quad \text{and} \quad \frac{T_0(1-x)}{P_0(1+x)} = 3.89$$

From which

$$\frac{(1+x)^2}{(1-x)^2} = \frac{4.25}{3.89} \quad \Rightarrow \quad (1+x) = 1.045(1-x) \quad \Rightarrow \quad x = \frac{0.045}{2.045} = 2.2\%$$

Substituting this value for x into the original equations gives $T_0/P_0 = 4.07$

Hence both the transmit and receive clocks must have a ratio of 4.07 and a tolerance of ±2.2%.This requirement is slightly more stringent than for the more usual 16× clock.