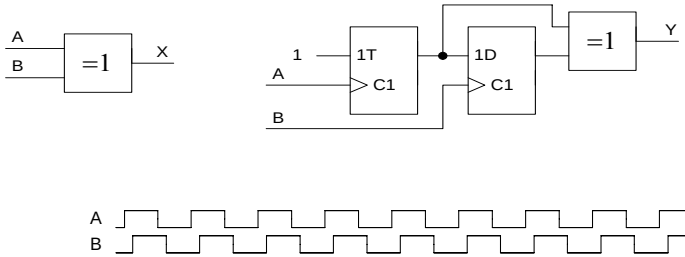
E2.11/ISE2.22 – Digital Electronics II

Problem Sheet 3

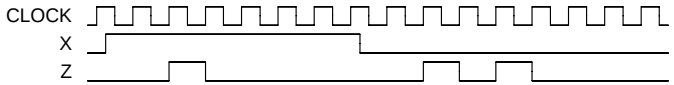
(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Q2:0 is the output of a 3-bit binary counter whose input is a constant frequency squarewave, CLOCK. Give a Boolean expression for Z in terms of Q2:0 such that Z is high whenever Q2:0 has the value 6. Draw a timing diagram showing the waveforms of CLOCK and Z and the value of Q2:0 during each clock cycle. Indicate on your diagram where glitches might occur in Z.

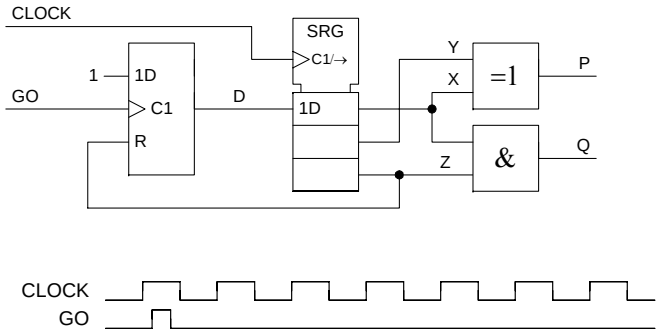
2C. The diagram shows two *phase-detector* circuits. Inputs A and B are symmetrical squarewaves with the same frequency but differing phases. Complete the timing diagram by showing the waveforms of X and Y for the case when B lags A by 45°. If logical 0 and 1 correspond to 0 V and 5 V respectively, sketch graphs showing how the DC components (i.e. average values) of X and Y vary with the phase difference.



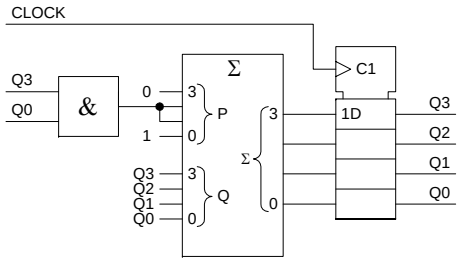
3B. The signal X forms the input to a shift register that is clocked by CLOCK↑. As shown in the timing diagram, the signal Z gives one pulse when X goes high and two pulses when it returns low. If the successive outputs from the shift register are A, B, C, … derive a Boolean expression for Z.



4B. Complete the timing diagram by drawing the waveform of P and Q. Explain why only one of these signals is certain to be glitch-free. If the GO pulse occurs at a random time with respect to the CLOCK, determine the average time delay in CLOCK periods between the GO↑ edge and the Q↑ edge.

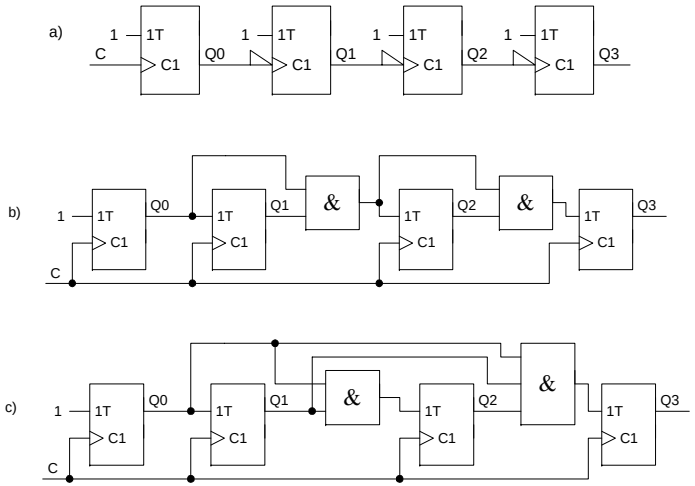


5C. The diagram shows an AND gate, a 4-bit register and an adder connected together to form a counter. List the values taken by the P input of the adder for all possible values of Q3:0. Draw a state diagram showing the sequence of values taken by Q3:0 on successive CLOCK pulses.



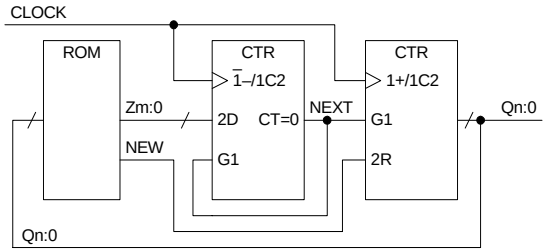
6C. Modify the above circuit so that it follows the count sequence 1, 2, 3, …, 9, 10, 1, 2, 3, …. Draw a state diagram for your revised circuit.

7C. In the following counter circuits, the propagation delays of gates and flipflops are 5 and 10 ns respectively and the setup time for the flipflops is 2 ns. In addition, a flipflop clock input must stay high for at least 5 ns and low for at least 2 ns. For each circuit, calculate the maximum clock frequency and the maximum propagation delay from the C input to any of the Qn outputs. Say what your answers would be for 32-bit counters designed in the same manner. Note that for design (c), each successive AND gate has one additional input.



8D. The diagram shows the circuit for a programmable pulse generator consisting of a read-only memory (ROM) and two counters of length m+1 and n+1 bits respectively. On the CLOCK↑ the leftmost counter is loaded with the value Z if NEXT=1 and counts down if NEXT=0 while the rightmost counter counts up if NEW=0 and is reset to zero if NEW=1. When the contents of the leftmost counter equal zero, its CT=0 output goes high. Determine the waveform of Q0 if the ROM contents are:

Q1:0	Z2:0	NEW
0	5	0
1	0	0
2	3	0
3	2	1



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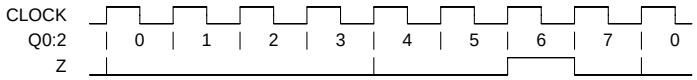
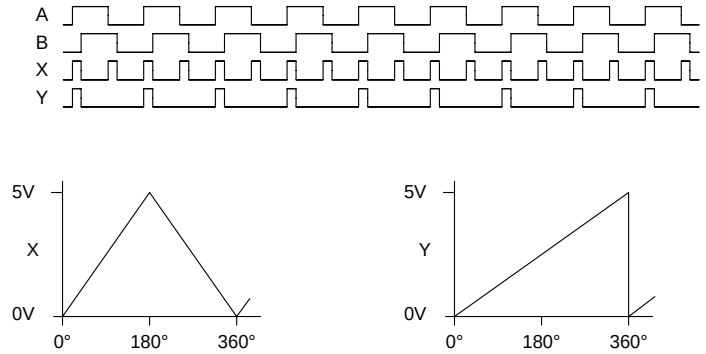
Solution Sheet 3

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Z = Q2•Q1•!Q0. Note that (a) Q2 is always the MSB and (b) we must include the !Q0 term. Glitches in Z are possible for the transitions 3→4 and 7→0.



2C. The XOR gate goes high twice per cycle whereas the more complicated circuit only goes high once per cycle. The advantage of the complicated circuit is that it covers a full 360° monotonically.

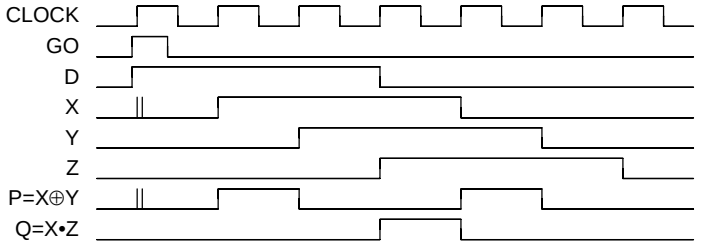


3B. Z = B ⊕ C + !D • E

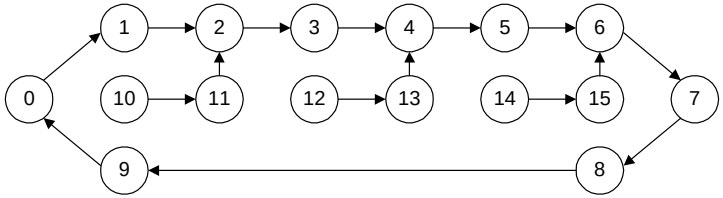
Note that since this expression does not involve A, it will be glitch-free.

4C. The output of the first shift-register stage can go metastable if D↑ occurs just before the CLOCK↑ edge. This will only affect the P output because Z will be low at the time which will force Q low regardless of X.

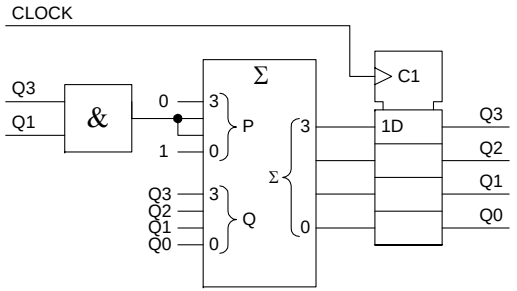
The average time delay between GO↑ and Q↑ will be 2½ clock periods.

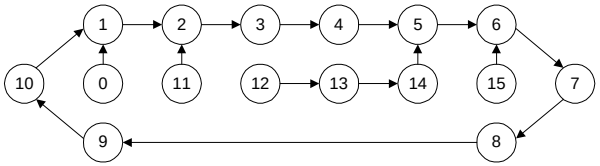


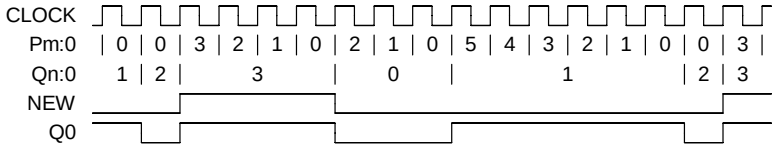
5C. The P input of the adder equals 7 when Q is 9, 11, 13 or 15. For all other values of Q it equals 1. Bearing in mind that the adder result is modulo 16 (i.e. 10+7=1), this results in the following state diagram:



6C. We want to make 10 the maximum count rather than 9, so we need to detect when Q3 and Q1 are high. We will now add 7 onto Q in states 10, 11, 14 and 15.







7C. For the 4-bit counters shown:

(a) Frequency limited only by the CLOCK constraints: 1/7ns =143 MHz (or 100 Hz if it must be symmetrical). The worst-case propagation delay is the change from 1111 to 0000 which takes 40 ns.

(b) $T - (10+5+5) > 2 \Rightarrow T > 22 \Rightarrow f < 45$ MHz. Delay = 10 ns.

(c) $T - (10+5) > 2 \Rightarrow T > 17 \Rightarrow f < 59$ MHz. Delay = 10 ns.

For a 32-bit counter:

(a) Worst-case delay increases to 320 ns

(b) We now have $T > 12 + 30 \times 5 = 162 \Rightarrow f < 6$ MHz.

(c) Unchanged.

The ripple counter (a) has the highest clock speed but the longest propagation delay. As the counter length increases, the propagation delay of design (a) increases while the maximum clock frequency of design (b) decreases. Design (c) maintains its high performance regardless of counter length but requires some very large gates.

8D. The Q0 output goes alternately high and low for a length of time determined by the leftmost counter. Thus the ROM output Zm:0 that is associated with each value of Qn:0 is one less than the length of the next count sequence. When NEW is high, the whole sequence starts again from Q=0. For the ROM contents given in the question, we get a total cycle length of 14 clock cycles.

In the timing diagram, Pm:0 is the contents of the leftmost counter.