E2.11/ISE2.22 – Digital Electronics II

Problem Sheet 5

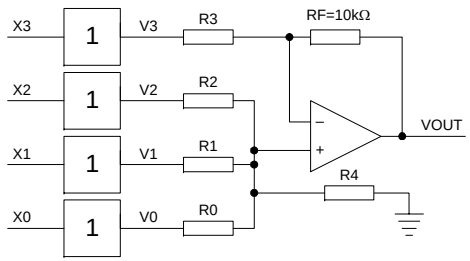
(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. A 3½ digit Digital Voltmeter has a display range of ±1999 and an accuracy of ±2 on the display. How many bits would a binary A/D converter need to have for its ±0.5 LSB accuracy to be as good as that of the DVM?

2B. A 12-bit converter has a resolution of 1 mV (i.e. 1 LSB = 1 mV) and input voltages in the range ±0.5 mV are converted to the value 0. What range of input voltages will be converted to –2047 ?

3B. A 10-bit converter converts an input voltage x to the value floor(x / 10mV). If 1 V < x < 8 V, what range of output values will be obtained ?

4C. X3:0 is a 4-bit signed number whose value, X, lies in the range –8 to +7. If the logic levels of V3:0 are 0 V and +5 V, choose values for R0 to R4 so that VOUT is equal to X/8 volts.



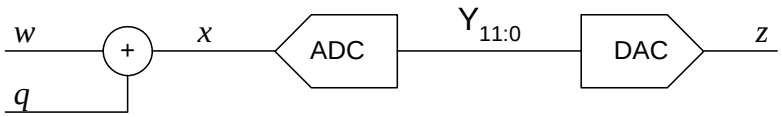
5C. The composite video signal to drive a monochrome TV monitor takes one of three different voltages according to the values of two digital signals DATA and SYNC:

DATA	SYNC	V_{OUT}
0	0	0.0
1	0	0.7
0	1	–0.3
1	1	Don't Care

Design a circuit to generate VOUT having a 50 Ω output impedance. You may assume that output logic levels are 0 and 5 V and that +5 V and –5 V power supplies are available should you need them. You do not need any op-amps although you will need at least one logic gate.

6B. Signals on a compact disc are stored as sequences of 16-bit numbers. Determine the maximum undistorted signal-to-noise ratio obtainable for a music signal whose peak amplitude is 10 times as great as its RMS value.

7B. Traingular pdf dither, q, of amplitude ±1 mV is added to an input signal, w, before conversion to a 12 bit number Y11:0. This is then sent to a DAC to generate an output voltage z. If all voltages are measured in mV then $z = \text{round}(w+q)$ and the pdf of q is equal to $p(q) = 1 - |q|$ for $|q| < 1$.



(a) Assuming that $|w| < 0.5$, show that the probability that $z = -1$ is given by $pr(z=-1) = 0.125 \times (2w-1)^2$.

(b) Derive similar expressions for $pr(z=0)$ and $pr(z=+1)$ for $|w| < 0.5$.

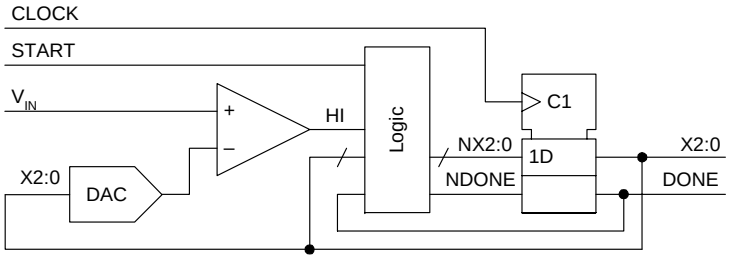
(c) Determine the mean and variance of z in terms of w.

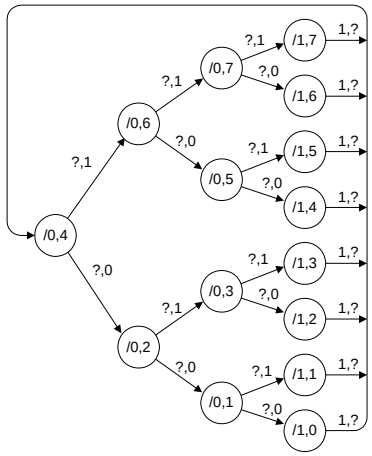
8C. A sample-hold circuit is used to store the input voltage of a 12-bit A/D converter during each conversion. The sample-hold circuit has an aperture uncertainty of 5 ns and a leakage current of ±1 nA. The A/D converter has an input voltage range of ±10 V.

If the input voltage is a sine wave of amplitude 10 V, calculate the input frequency at which the aperture uncertainty will result in an error of ±0.5 LSB [surprisingly low].

If the sample-hold uses a storage capacitor of 200 pF calculate how long the input voltage can be held before it changes by 0.5 LSB due to the leakage current.

9D. The circuit and state diagrams for a successive approximation converter are shown below. The output signals X2:0 and DONE are also used as the state bits. Derive Boolean equations for NX2:0 and NDONE. You should ensure that your circuit can never get stuck.





I/O Signals: START,HI/DONE,X0:2

10B. In the questions below, u represents a 4-bit unsigned binary number in the range 0 to 15 and x represents a signed 4-bit binary number in the range –8 to +7. Determine the range of possible values that each expression can take and give a Boolean expression for each bit of the corresponding binary number (signed or unsigned as appropriate). The function floor(x) denotes the largest integer less than x.

(a) $15 - u$	(b) floor(u/8)	(c) $u - 8$
(d) floor(u/2)	(e) $-(x+1)$	(f) floor(x/2)
(g) –floor(x/8)	(h) x – 8×floor(x/8)	(i) $x - 16\times$floor(x/8)
(j) floor(u/2) – 4×floor(u/8)	(k) $2u - 15\times$floor(u/8)	(l) $u - 16\times$floor(u/8)

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Solution Sheet 5

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. Full-scale range = 3998 so the accuracy is 2/3998 of full-scale range. For an N-bit binary A/D converter, the full-scale range is (2^N–1) LSB giving an accuracy of 0.5/(2^N–1).

Hence $\frac{0.5}{2^N - 1} \le \frac{2}{3998} \quad \Rightarrow \quad 2^N \ge 1000.5 \quad \Rightarrow \quad N \ge 9.96 \quad \Rightarrow \quad N = 10$

2B. –2047 mV ±0.5 mV, i.e. –2047.5 mV to –2046.5 mV.

3B. 1 V and 8 V correspond to output values of 100 and 800 respectively, so if 1 V < x < 8 V, the output will be in the range 100 to 799.

4C. A change of 5 V in V3 must give a change of –1 V in VOUT, a gain of –0.2. Hence RF/R3 = 0.2 ⇒ R3 = 50 kΩ.

When V3=0, the op-amp may be viewed an a non-inverting amplifier with a gain of (1 + RF/R3) = 1.2. The voltage at VOUT due to V2:0 is therefore given by:

$$V_{OUT} = 1.2 \times \frac{G_2 V_2 + G_1 V_1 + G_0 V_0}{G_4 + G_2 + G_1 + G_0}$$

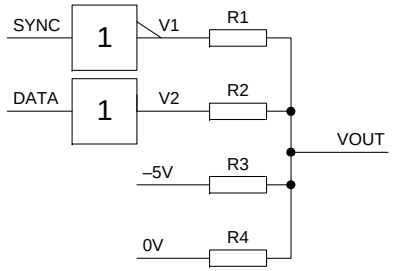
where G4:0 are the reciprocals of R4:0.

To minimize the effect of op-amp bias currents, we should make the Thévenin impedances at the input terminals equal. This means that G4+G2+G1+G0 = G3+GF = 120 µS.

The gains from V2, V1 and V0 to VOUT must be 0.1, 0.05 and 0.025 respectively. Thus we have G2 = 120 µS × 0.1/1.2 = 10 µS ⇒ R2 = 100 kΩ. Similarly, R1 = 200 kΩ and R0 = 400 kΩ.

Finally G4 = 120 µS – G2 – G1 – G0 = 102.5 µS ⇒ R4 = 9.8 kΩ.

5C. The SYNC signal needs inverting because SYNC going high must cause the output to decrease. We will need a negative bias voltage in order to obtain –0.3 V. Our circuit is therefore:



Taking Gn = 1/Rn we must have G1+G2+G3+G4 = 1/50Ω = 20 mS.

Then VOUT = ($V_1G_1 + V_2G_2 – 5G_3$) / 20 mS.

From the truth table, we see that changes of 5 V in V1 and V2 must give changes in VOUT of 0.3 and 0.7 volts respectively; this means we need gains of 0.06 and 0.14. Hence:

G1 = 0.06 × 20 mS = 1.2 mS ⇒ R1 = 833Ω.
G2 = 0.14 × 20 mS = 2.8 mS ⇒ R2 = 357Ω.
To generate the –0.3 V offset: 5G3 = 0.3 × 20 mS = 6 mS ⇒ R3 = 833Ω.
G4 = 20 mS – G1 – G2 – G3 = 14.8 mS ⇒ R4 = 67.6Ω.

Note it is possible to take R4 to +5 V instead in which case R3 and R4 are 116Ω and 135Ω.

This circuit is very fast since it has no op-amps.

6B. The range of a 16-bit signed number is ±32767 and so to avoid distortion, the RMS value must be no higher than 3276.7. From the notes, the RMS value of quantisation noise is 0.289 LSB which gives a signal-to-noise ratio of 11338 which equals 81 dB

7B. (a) z will equal -1 when $x < -0.5$, so

$$\begin{aligned} pr(z=-1) &= pr(x<-0.5) = pr(q<-0.5-w) \\ &= \int_{q=-1}^{-0.5-w} p(q)dq = \int_{q=-1}^{-0.5-w} 1-|q|\,dq = \int_{q=-1}^{-0.5-w} 1+q\,dq \\ &= \left[q+0.5q^2\right]_{q=-1}^{-0.5-w} = 0.125\times(2w-1)^2 \end{aligned}$$

Note that because $|w|<0.5$ is given in the question, both integration limits are always negative and so we can replace $|q| \to -q$ in the integrand. You can also get this answer graphically (and more easily) by drawing the pdf and finding the area of the triangle representing $pr(q<-0.5-w)$.

(b) $pr(z=+1) = 0.125\times(2w+1)^2$

$$pr(z=0) = 1 - pr(z=-1) - pr(z=+1) = 0.75 - w^2$$

(c) We have

$$\begin{aligned} E(z) &= 1\times pr(z=+1) - 1\times pr(z=-1) \\ &= 0.125\times\left((2w+1)^2 - (2w-1)^2\right) = w \end{aligned}$$

$$\begin{aligned} Var(z) &= E(z^2) - E(z)^2 = E(z^2) - w^2 \\ &= 1\times pr(z=+1) + 1\times pr(z=-1) - w^2 \\ &= 0.125\times\left((2w+1)^2 + (2w-1)^2\right) - w^2 \\ &= w^2 + 0.25 - w^2 = 0.25 \end{aligned}$$

8C. Full-scale range of 20 V equals 4096 LSB so 0.5 LSB = 0.5 × 20/4096 = 2.44 mV.

The peak rate of change of a 10 V sinewave is $20\pi f$ volts per second. The voltage change in 5 ns is therefore $\pi f \times 10^{-7}$. These are equal when f = $2.44 \times 10^{-3} \times 10^{7} / \pi$ = 7.77 kHz.

For the second part I = C dV/dt from which $\Delta t = C\times\Delta V/I = 2\times10^{-10}\times2.44\times10^{-3}/10^{-9}$ = 488 μs.

9D. We send the all zero state to the initial state of a conversion.

$$\begin{aligned} NDONE &= DONE\cdot\overline{START} + \overline{DONE}\cdot X0 \\ NX2 &= DONE\cdot(X2+START) + \overline{DONE}\cdot X2\cdot(X0+X1+HI) + \overline{DONE}\cdot\overline{X2}\cdot\overline{X1}\cdot\overline{X0} \\ NX1 &= DONE\cdot X1\cdot\overline{START} + \overline{DONE}\cdot X1\cdot(X0+HI) + \overline{DONE}\cdot X2\cdot\overline{X1}\cdot\overline{X0} \\ NX0 &= DONE\cdot X0\cdot\overline{START} + \overline{DONE}\cdot X0.HI + \overline{DONE}\cdot X1\cdot\overline{X0} \end{aligned}$$

10B. We call the answer w or z according to whether it is unsigned or signed:

(a) 0<=w<=15, W_i=!U_i

(b) 0<=w<=1, W_0=U_3

(c) –8<=z<=7, Z_3=!U_3, Z_i=U_i for i=0,1,2

(d) 0<=w<=7, W_i=U_{i+1}

(e) –8<=z<=7, Z_i=!X_i

(f) –4<=z<=3, Z_i=X_{i+1}

(g) 0<=w<=1, W_0=X_3

(h) 0<=w<=7, W_i=X_i for i=0,1,2

(i) 0<=w<=15, W_i=X_i

(j) 0<=w<=3, W_i=U_{i+1} for i=0,1

(k) 0<=w<=15, W_0=U_3, W_i=U_{i-1} for i=1,2,3

(l) –8<=z<=7, Z_i=U_i