E2.11/ISE2.22 – Digital Electronics II

Tutorial Problems

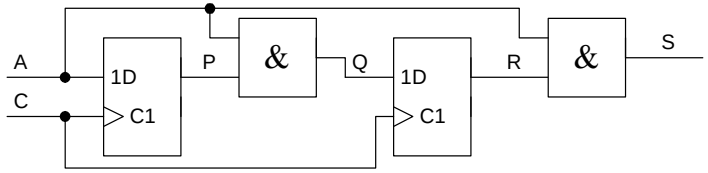
These three questions are intended for discussion at tutorials. Each student should bring a worked solution to his or her tutorial in the weeks specified for each question.

1. **For discussion in the tutorial in weeks 4 or 5 (26 Oct to 6 Nov).**

   In the circuit below the propagation delay of the flipflops may vary between 4 and 7 ns while the propagation delay of the gates may vary between 2 and 6 ns.

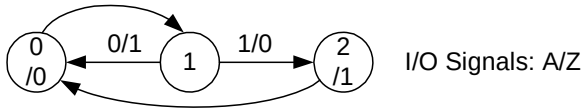
   Calculate the minimum and the maximum propagation delays from each of A and C to each of P, Q and R and S.

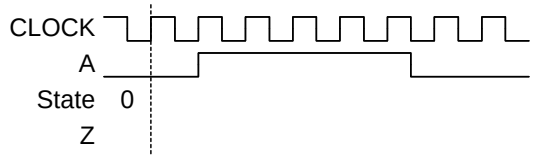
   If the flipflops have a setup time of 5 ns, what is the maximum frequency of C?



2. **For discussion in the tutorial in weeks 6 or 7 (9 Nov to 20 Nov).**

   The state diagram for a state machine is shown below. All state transitions occur on the rising edge of CLOCK. Complete the timing diagram be showing the sequence of states and the value of the output signal Z. Transitions in A occur slightly after the CLOCK edges.

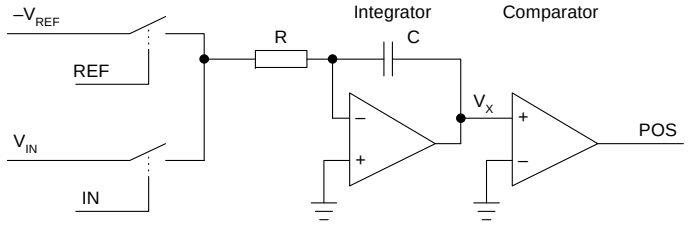




3. **For discussion in the tutorial in weeks 8 or 9 (23 Nov to 4 Dec).**

   In the dual-ramp converter shown, V_{REF} = 5 V, V_{IN} lies in the range 0 to +10 V and the signal integration time is 20 ms. Calculate the values of R and C so that the maximum current through C is 50 µA and V_X always lies within the range ±10 V.

   Sketch the waveforms of IN, REF, POS, V_R and V_X when converting an input of V_{IN} = 8 V. Mark all important times and voltages on the waveforms.



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Solution to Tutorial Problems

1. See pages 1.3,1.4,2.3 and 2.4 of the notes.

The propagation delay of a circuit is the time delay between an input transition and a consequential output transition. This is a slightly trick question because there is no propagation delay between A and of P or R since a transition in A does not directly cause these signals to change. It is an important property of a flipflop that its output changes only in response to rising CLOCK edges. The min and max delays from A to S or Q are 2 and 6 ns. Of course if P (or R) happen to be low, there is no propagation delay between A and Q (or S) either.

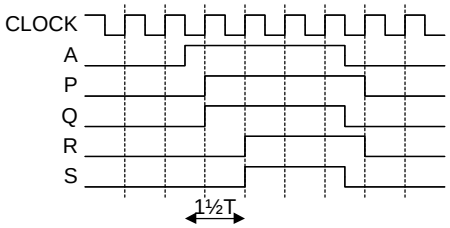
The min and max delays from C to P, Q, R and S are 4 and 7, 6 and 13, 4 and 7, and 6 and 13 ns respectively. The important point to realise is that since a transition at Q does not directly cause R to change, it follows that there is no delay path through both flipflops. The expression for a propagation delay **never** involves more than one flipflop delay.

The minimum clock period is the sum of the setup time and the maximum delay from the clock to the data input of the second flipflop, Q. This equals 5 + 13 = 18 ns giving a maximum clock frequency of 55.6 MHz.

The hold time requirement will result in a second inequality, but in a circuit like this, in which all flipflops respond to the same edge of a common clock, the inequality does not involve the clock period and is always satisfied. It is worth pointing out that you NEVER get both the setup time and the hold time in the same equation.

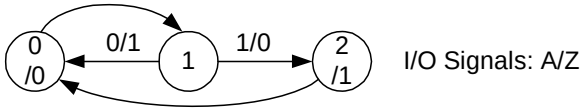
Discussion points:

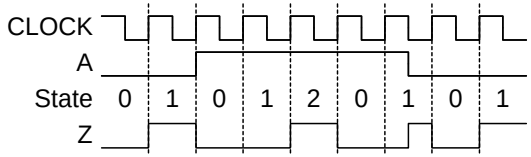
- **Action of the circuit**. The output, S, follows the input, A, with a delay that is different for rising and falling edges. For falling edges the delay is 6 ns, while for rising edges it averages 1½ clock cycles.



- **Application of the circuit:** A circuit such as this can be used to generate the WAIT signal in a microprocessor-to-memory interface. The signal A would go high to indicate a memory access request by a microprocessor. After some delay, the signal S would go high to indicate that the memory had had time to respond. At the end of the memory access cycle, A is taken low and S follows low immediately.
- **Time Delay**: The time delay between A and P may vary from around 0 to around *T*, the clock period. If we are being pedantic it can vary from $t_{propagtaion}–t_{hold}$ to $T+t_{propagtaion}+t_{setup}$.
- **Metastability**: If A changes within the setup-hold window then one or both the flipflops may become metastable for 10's of nanoseconds and the flipflop output may change one or more times during this period. In general, if a flipflop's data input is not synchronized with its CLOCK, you need to wait a relatively long time after the CLOCK rising edge before you can trust the flipflop output to be stable.

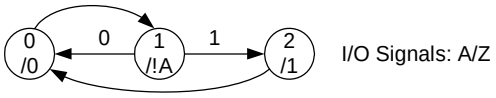
2. See page 3.9 of the notes. It is easiest to find the state sequence first and then fill in Z. We know that Z is low in state 0, high in state 2 and equal to !A in state 1.





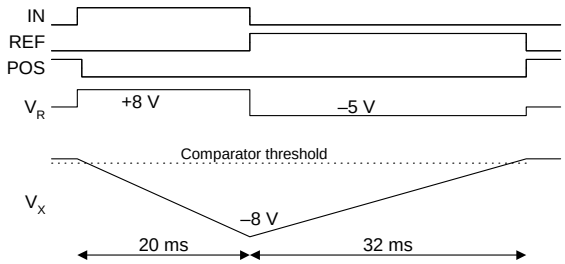
Discussion points:

- **State Transitions**: All state transitions occur on the rising edge of CLOCK. This is a defining feature of synchronous state machines. Equivalently, the circuit remains in each state for an integral number of clock cycles.
- **Timing Diagram Conventions**: A timing diagram is drawn at a scale appropriate for the purpose in hand and should not include irrelevant detail. In this case, the timing diagram illustrates the state sequence of the circuit but makes no attempt to show time delays of only a few nanoseconds. It is understood by convention that when a signal transition is shown as occurring at the same time as a CLOCK edge, it actually occurs o few nanoseconds afterwards. Thus the transitions of A would be assumed to occur just after the CLOCK edges even if the question had not states this explicitly.
- **Labels on arrows:** Labels on an arrow refer to the state emitting the arrow (not the one receiving it). Thus the labels 0/1 and 1/0 specify the value that Z takes while in state 1.
- **State sequence**: The next state is determined by the current state and the value of the input just before the rising edge of the CLOCK. It is important to realise that the circuit is not prescient and its behaviour cannot depend on what A does after the CLOCK edge. Hence the state in the third clock cycle above is 0 and not 2.
- **Boolean Output Expressions**: The labels on the arrows emitted by state 1 specify the value of Z. We can represent the same information as shown below: the choice is merely a matter of taste.



- **Moore/Mealy**: This is a Mealy machine because in at least one state, the output depends directly on the input. This is also apparent from the timing diagram above in which it can be seen that when A changes in the middle of a clock cycle, this causes an immediate change in the output Z.

3. See pages 4.20 and 4.21 of the notes. Tohe maximum voltage across R is 10 V, so to get a maximum current of 50 µA we must have R = 200 kΩ. The minimum value of VX arises when we integrate 50 µA for 20 ms. Thus C = 50 µA × 20 ms / 10 V = 100 nF.



Discussion points:

- A commercial converter will normally include (a) a unity-gain buffer on the input, (b) some extra circuitry to null out offsets in the buffer and integrator op-amp.
- **Converting Negative Inputs**: To make a bipolar converter, you need a $+V_{REF}$ reference as well. You could generate this with a unity-gain inverter but a mor accurate method is to charge up a capacitor and then use switches to reverse it polarity.