Ratiometric current-mode rational DAC

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By exploring the principle of current division, a ratiometric current-steering rational implementation of a rational digital-to-analogue converter (DAC) is proposed. In this implementation, current scaling is achieved through ratios and, as a result, achieve greater independence from actual physical parameters and their associated non-idealities, resulting in the potential for achieving higher accuracy.

Introduction: Rational digital-to-analogue converters (DACs) may be viewed as a general ratio-based quantisation scheme in which the quantisation values are derived from ratios with variable numerators as well as denominators [1]. Accordingly, linear quantisation can be viewed as an important subset of such a quantiser, where the quantisation values are derived from only variable numerators and a fixed denominator. While previous implementations have demonstrated the feasibility of the more general rational quantisation scheme, implementation of the DAC, particularly in realising the variable denominator has proved to be tricky.

The non-idealities of real transistors in the realisation of the divide operator inherent in the rational quantisation scheme, such as with the translinear divider/multiplier approach, constrained the operation range of such DACs within strict limits where assumptions such as the exponential I–V characteristic of weak-inversion MOS transistors and the independence of current flow from gate–source voltage for a MOS transistor in saturation are valid.

Ratiometric approach: This Letter concentrates on the realisation of the variable denominator, as realisations of the variable numerator have been covered extensively in the literature for linear DACs [2, 3]. In particular, the proposed approach focuses on exploiting strictly linear relationships between devices that are valid at all operating points to achieve current division.

It is useful at this point to distinguish between current division, where one current is arithmetically divided by another current, and current partitioning, in which a current is split into several smaller currents in accord with Kirchhoff's Current Law, as networks that partition currents are also frequently referred to in the literature as current dividers.

In this case, the principle of current partitioning was used to effect current division. In the simple case in which a current is split into two branches, as shown in Fig. 1, the current through R_1 would be:

$$I_1 = \frac{R_2}{R_1 + R_2} I_{in} \tag{1}$$

If R_2 is a composite resistor, whose resistance is the effective resistance of a switched network of binary weighted resistors in parallel, then:

$$R_2 = \frac{1}{\sum_{i=0} b_i/r_i} = \frac{r}{\sum_{i=0} 2^i b_i} \tag{2}$$

where $r_i = r/2^i$, and b is the bit value that is 1 when the switch is on and 0 otherwise. If $r = R_1$, the current through R_1 would then be:

$$I_1 = \frac{1}{1 + \sum_{i=0} 2^i b_i} I_{in} \tag{3}$$

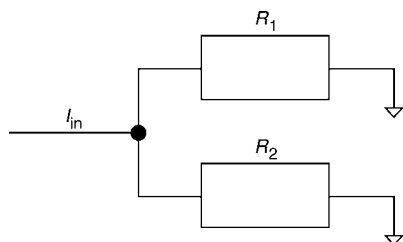which is independent of the actual resistance of the network.

Fig. 1 *Basic two-resistor current-divider network*

Hence, the ratiometric approach provides a means to tune a current in an inverse manner as required in realising a variable denominator in a rational DAC in a highly linear way that is independent of non-idealities intrinsic in real devices, as long as the devices are matched in the sense that $r = R_1$.

CMOS implementation: As a simple example, a CMOS implementation of a 2×3-bit base precision rational DAC, where the variable denominator is implemented using the ratiometric approach discussed in the previous section, is shown in Fig. 2 as an illustration of how the proposed approach might work.
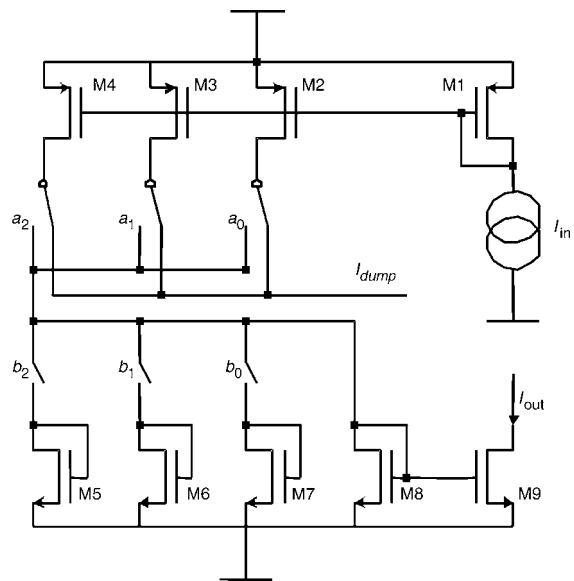

Fig. 2 *Ratiometric CMOS implementation of 2×3-bit rational DAC*

The PMOS transistors implement a straightforward standard current-scaling DAC that will generate the variable numerator values. The transistors M2–4 serve as current sources that are controlled by the input current I_{in} through M1. The geometries of M2–4 are scaled in increasing binary factors of M1's size, such that $S4 = 2S3 = 4S2 = 4S1$, where S is the parameter that modulates the width and length of the individual transistors. The currents through each source are then switched between the dump or through the NMOS transistors M5–8, where the total current through M5–8 is:

$$I^* = \sum_{j=0}^{3} 2^j a_j \tag{4}$$

where a is the bit value that determines the state of the switch, such that when a is one the switch directs currents to the left and when it is zero switches it to the right.

The transistors M5–8 implement active resistances, where M5–7 realise the switched binary scaling network of parallel resistors, whose effective resistance corresponds to R_2 in the earlier analysis, while M8 is the MOS active equivalent of R_1. The transistors implement active resistances such that $R_8 = R_7 = 2R_6 = 4R_5$.

The active resistance of any of the transistors M5–8 is given by the inverse of the small-signal transconductance. In general, the resistance can be implemented as a parallel bank of identical diode-connected transistors of the same size as M8. In this way, the current through any of the transistors and the voltage across it if its corresponding switch is on would be the same, and hence their transconductance would be matched.

Hence, the overall transfer function of the rational DAC in Fig. 2 is:

$$I_{out} = \frac{\sum_{j=0}^{3} 2^j a_j}{1 + \sum_{i=0}^{3} 2^i b_i} I_{in} \tag{5}$$

Simulation and results: A 2×8-bit precision rational DAC was simulated using the AMS 0.35 μm process models. Binary-scaled PMOS transistors were used to implement the switched current sources, while the sinks were implemented with binary scaled

NMOS transistors, where the resistances of the sinks were decreased by scaling the transistor widths.

Two types of switches were used in the design. A asymmetrical low-glitch differential pair proposed by Wu *et al.* [4] was used to implement the current steering switches in the implementation of the variable numerator as well as in achieving bipolar operation, while single transistor MOS switches were used to direct the flow of current in the current divider network within the numerator block.

Fig. 3 shows the output current of a simulation run with a 9.8 kHz normalised tone fed into the digital control block and sampled at 1.25 MHz, with a bias current of 100 nA, resulting in an output peak current of 49.7 µA.
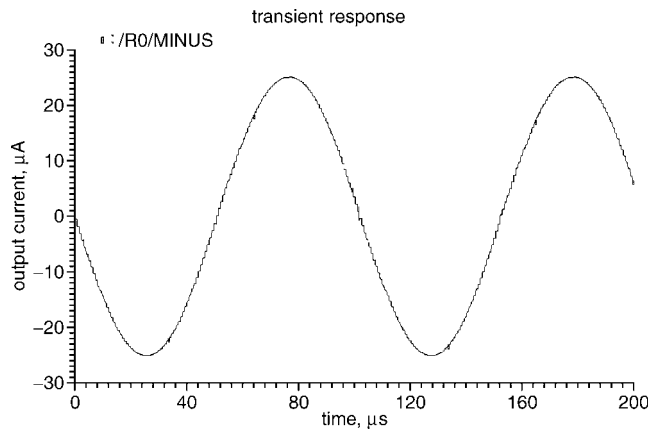

Fig. 3 *Simulated output with 9.8 kHz test tone sampled at 1.25 MHz*

Conclusion: A ratiometric implementation of a rational DAC, in which free and very linear current division of the numerator term by the denominator term is obtained as a result of Kirchhoff's current law, has been demonstrated using an elegant totally CMOS design.

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