Guest Editors' Introduction: Field Programmable Logic and Applications

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THE impact of Field Programmable Logic on the computing community has been growing for more than a decade. Field Programmable Logic devices are no longer just a prototyping vehicle for Application-Specific Integrated Circuits (ASICs), but are increasingly found in computer systems where the user configurable logic and interconnects offer unique advantages. This special section contains seven papers reporting on a number of interesting advances in the architectures, compilation techniques, and applications of configurable computer systems, all chosen from the 13th International Conference on Field Programmable Logic and Its Applications, held on 1-3 September 2003 in Lisbon, Portugal.

Two papers are selected to reflect the diversity that reconfigurable architecture can offer. The paper "The MOLEN Polymorphic Processor" by S. Vassiliadis, S. Wong, G. Gaydadjiev, K. Bertels, G. Kuzmanov, and E. Moscu Panainte presents a mixed general purpose and custom computing machine, proposing their own computing paradigm, instruction set, and compiler methodology. This paper attempts to combine both by extending a general purpose instruction set with eight special instructions to implement reconfigurable functions. This paper illustrates that the traditional barrier between the software and hardware worlds is fast diminishing. Many of the modern Field Programmable Gate Array (FPGA) architectures which include embedded processors also illustrate this new reality. The second paper, "An Asynchronous Dataflow FPGA Architecture" by J. Teifel and R. Manohar, presents an FPGA architecture able to implement high-performance asynchronous logic using the dataflow paradigm. These asynchronous circuits do not need a global clock to ensure that computation proceeds in the right sequence. Instead, all cells compute concurrently and are connected by specific communication channels which guarantee the necessary data dependencies according to a dataflow scheme. They developed a specific asynchronous FPGA device instead of utilizing conventional clocked FPGA architectures, as has been done by others in the past.

Software environments and tools for reconfigurable computers can be very different from those found in conventional computers. Three papers are selected to demonstrate such differences. The first, "Operating Systems for Reconfigurable Embedded Platforms" by C. Steiger, H. Walder, and M. Platzner, addresses some issues in the design of an operating system for a reconfigurable system, focusing on the runtime environment that guarantees proper scheduling of real-time tasks. Unlike conventional software-only scheduling, this operating system requires a strong connection between the scheduling and placement of hardware modules. The second paper, "Exploiting Program Branch Probabilities in Hardware Compilation" by H. Styles and W. Luk, addresses a very interesting topic relating to the optimization of circuits implementing behaviors with branching constructs. For many years, software compilation has taken advantage of branch probabilities to optimize the average-case performance of algorithms. This paper extends the approach to compilation for reconfigurable hardware. It is demonstrated that an approach based on queuing theory can provide insights into an appropriate trade off between circuit area and circuit performance for each component in a design. As a result, the overall design has significantly improved performance under the same area constraint, compared to common approaches that do not consider load balancing issues. The last compilation paper by K. Shayee, J. Park, and P. Diniz considers the impact of compiler loop transformations on hardware designs implemented in reconfigurable logic. It has long been accepted that loop transformations offer a useful way to formalize and automate design space exploration. However, the impact of loop transformations on circuit performance is not always well-understood due to the simplifying architectural models often employed. This paper studies the impact of loop transformations on both area and performance measures and focuses on the particularly interesting area of loop transformations within architectures containing a limited number of memory channels.

Computer systems based on Field Programmable Logic only compete favorably against conventional computer systems in specific applications. Two such applications are chosen for the last two papers. The first by C. Ebeling, C. Fisher, G. Xing, M. Shen, and H. Liu presents the design and implementation of an OFDM receiver in the RaPiD reconfigurable architecture as a case study for comparing the relative cost and performance of ASIC, programmable, FPGA, and domain-specific reconfigurable systems. The last paper, by I. Skliarova and A. Ferrari, gives a

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comprehensive account of the attempts that have been made to solve Boolean Satisfiability (SAT) problems using Reconfigurable Hardware, including a system proposed and developed by the authors. Solving SAT using software algorithms is known to be a very difficult problem. On the other hand, hardware algorithms for SAT are particularly difficult due to the sheer size of common problem instances, which can be handled well by software algorithms making use of the virtual memory hierarchy. The quest for a general purpose reconfigurable machine has SAT as a major obstacle to be overcome. This paper offers a very good introduction to this fascinating research problem.

We hope the readers will enjoy reading this special section as much as we enjoyed compiling it.

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Guest Editors

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Peter Y.K. Cheung (M'85-SM'04) received the BSc degree in electrical engineering from Imperial College in 1973. After working at Hewlett Packard for a number of years, he returned to Imperial College as a research assistant and was appointed a lecturer in 1980. He is currently a professor of digital systems and deputy head of the Electrical and Electronic Engineering Department at Imperial College, University of London. His research interests include VLSI architectures for DSP and video processing, reconfigurable computing, embedded systems, and high-level synthesis and optimization of digital systems, particularly those containing field programmable logic. He has coauthored more than 100 publications and two research monographs in these areas and has served on the technical program committee of many international conferences, including ISCAS, FPL, FPT, and DATE. He is a senior member of the IEEE.

George A. Constantinides (S'96-M'01) received the MEng degree in information systems engineering and the PhD degree in electrical and electronic engineering from Imperial College, University of London, in 1998 and 2001, respectively. He has been a lecturer in digital systems in the Electrical and Electronic Engineering Department of Imperial College since 2002. He is the author of 25 refereed conference and journal papers and the book *Synthesis and Optimization of DSP Algorithms* (Dordrecht: Kluwer, 2004). His research interests include reconfigurable computing and electronic design automation, with a particular focus on digital signal processing algorithms. He was program cochair of the International Conference on Field-Programmable Logic and Applications in 2003 and serves on the program committees of FPL, FPT, ERSA, and ARC. He was the founding chair of the UK SIGDA chapter, serving as general chair (2001) and technical chair (2002-2003) of its annual workshop. He is a member of the IEEE and the ACM.

Jose T. de Sousa received the BS and MS degrees in electrical and computer engineering from IST-Technical University of Lisbon, in 1989 and 1992, respectively, and the PhD degree from the Department of Electrical and Electronic Engineering at Imperial College, University of London, in 1998. After working for almost two years as a member of the technical staff at Bell Laboratories-Lucent Technologies, Inc, in Murray Hill, New Jersey, he returned to IST-Technical University of Lisbon in 1999 as an assistant professor in the Department of Electrical and Computer Engineering, where he is currently the head of the Software/Configware Algorithms Group. He is coauthor of *Boundary-Scan Interconnect Diagnosis* (Dordrecht: Kluwer, 2004),and coeditor of *Field Programmable Logic and Applications* (Springer Verlag, 2003). He has written more than 40 technical papers in the areas of electronic testing and reconfigurable logic. He is a steering committee and a program committee member of the International Conference on Field Programmable Logic and Applications, of which he was general chair in 2003. He has been a program committee member of the North Atlantic Test Workshop (NATW) and of the International Workshop on Applied Reconfigurable Computing (ARC) since 1999 and 2004, respectively. He is member of the IEEE and AES.