# Lecture 10: Sequential Circuits

Digital Electronics I



# Points Addressed in this Lecture

- Properties of synchronous and asynchronous sequential circuits
- Overview of flip-flops and latches



# Properties of Sequential Circuits

- So far we have seen Combinational Logic
  - the output(s) depends only on the current values of the input variables
- Here we will look at Sequential Logic circuits
  - the output(s) can depend on present and also past values of the input and the output variables
- Sequential circuits exist in one of a defined number of states at any one time
  - they move "sequentially" through a defined sequence of transitions from one state to the next
  - The output variables are used to describe the state of a sequential circuit either directly or by deriving state variables from them



# Synchronous and Asynchronous Sequential Logic

- Synchronous
  - the timing of all state transitions is controlled by a common clock
  - changes in all variables occur simultaneously
- Asynchronous
  - state transitions occur independently of any clock and normally dependent on the timing of transitions in the input variables
  - changes in more than one output do not necessarily occur simultaneously
- Clock
  - A clock signal is a square wave of fixed frequency
  - Often, transitions will occur on one of the edges of clock pulses
    - i.e. the rising edge or the falling edge

# Truth Tables

- Just as for combinational circuits, sequential circuits can be described using truth tables
- In sequential circuits, truth tables include the idea of transitions in time

| A | B | Q+ |
|---|---|---|
| 0 | 0 | Q |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | X |

- Notes
  - Q is the output before a change in inputs
  - Q+ is the output after a change in inputs
  - X is don't care
- For synchronous circuits Q+ is the value of Q at the next clock pulse



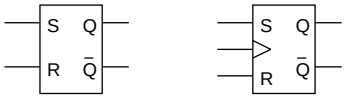
# Flip-Flops

- Flip-flops are the fundamental element of sequential circuits
  - bistable
  - (gates are the fundamental element for combinational circuits)
- Flip-flops are essentially 1-bit storage devices
  - outputs can be set to store either 0 or 1 depending on the inputs
  - even when the inputs are de-asserted, the outputs retain their prescribed value
- Flip-flops have (normally) 2 complimentary outputs
  - $Q$ and $\overline{Q}$
- Three main types of flip-flop
  - R-S J-K D-type



# R-S Flip-Flop

- Symbols



Asynchronous



Synchronous

- Operation
  - Asserting S sets $Q$ to 1 and $\overline{Q}$ to 0
  - Asserting R resets $Q$ to 0 and $\overline{Q}$ to 1
  - In the asynchronous flip-flop the outputs change immediately following the changes in the inputs
  - In the synchronous flip-flop the outputs change on the next clock pulse after the changes in the inputs

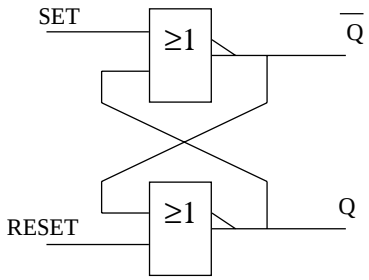


- Truth Table

| S | R | Q+ | |
|---|---|---|---|
| 0 | 0 | Q | *** |
| 0 | 1 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | X | |

- the "memory" in this device can be seen in the truth table row marked ***
  - i.e. when S=R=0, the output holds onto its value
- in a synchronous flip-flop the Q output changes on the next clock
- the input condition S=R=1 produces an undefined output X
  - this combination of inputs would normally be avoided in a design

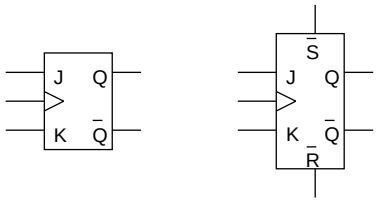
# Construction of a Bistable Circuit






# J-K Flip-Flop

- Symbol




- Operation
  - The J-K flip-flop is a synchronous device
  - Inputting J=1 and K=0 sets $Q$ to 1 and $\overline{Q}$ to 0 after the next clock pulse
  - Inputting J=0 and K=1 resets $Q$ to 0 and $\overline{Q}$ to 1 after the next clock pulse
  - Additional S and R inputs are sometimes included to permit asynchronous set and reset of the outputs respectively. These signals override the J and K inputs.



- Truth Table

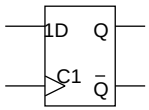
| J | K | $Q+$ |
|---|---|---|
| 0 | 0 | $Q$ |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q}$ |

- Notes
  - the first 3 lines of the truth table are the same as for R-S flip-flop
  - all input combinations have defined outputs
  - Q+ indicates the value of Q after the next clock pulse
  - inputting J=K=1 causes the output to toggle on each clock pulse
    - you might call this a Toggle flip-flop



# D Flip-Flop

- Symbol




Operation
  - The D-type flip-flop is a synchronous device
  - It has one data input and a clock.
  - On the rising edge of the clock the data on D goes to the output Q
- Truth Table

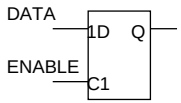
| D | Q+ |
|---|---|
| 0 | 0 |
| 1 | 1 |

- Notes
  - Probably the simplest flip-flop and very widely used

# Transparent Latch

- A latch is a device which “latches” data for use at a future time.
- The D-type flip-flop can do this - so can a transparent latch

- Symbol




- Truth Table

| ENABLE | Q+ |
|---|---|
| 0 | Q |
| 1 | DATA |

- Operation
  - When ENABLE goes to 0, Q is "latched" (held at its current value)
  - When ENABLE is 1, Q is the same a DATA



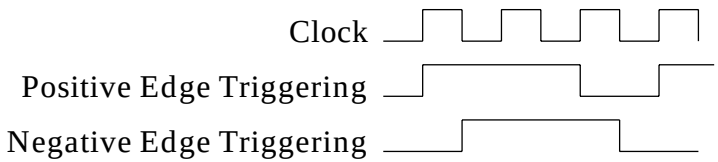
# Transparent Latch Implementation

- Tocci page 205



# Edge-Triggering

- Synchronous flip-flops change state on the edge of a clock pulse
- Positive edge triggered:
  - changes state on the 0 to 1 transition of the clock
- Negative edge triggered:
  - changes state on the 1 to 0 transition of the clock






- D-types are positive edge triggered
- J-Ks are negative edge triggered
  - need to check on the data sheet for a particular device
- For internal design of flip-flops see:
  - section 4.3 of Wilkinson and
  - (The internal design of flip-flops is non-examinable material in this course)