Lecture 10: More on Flip-flops

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Points Addressed in this Lecture

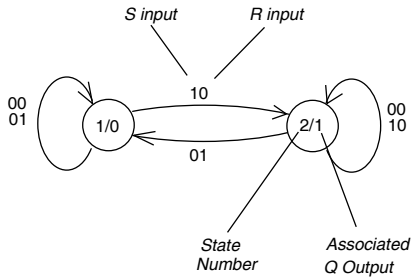
- Introduction to Moore model and Mealy model state diagrams
- State diagrams and state tables of flip-flops
- Timing parameters of flip-flops

State Diagrams

- There are two ways to draw state diagrams:
  - **Moore** model and **Mealy** model
  - we will look first at the Moore model using the Reset-Set (RS) flip-flop as an example
- A Moore model state diagram shows
  - a circle for each of the various "states" a circuit can be in
    - "states" refers to the logic levels around the circuit
  - labels in the circles to show the state number and the associated output for that state
  - an arrow for each possible transition between states
  - labels on the arrows to show the required conditions to transit between states

State Diagram of RS Flip-Flop

- The circuit must be in either state 1 or state 2.



- In state 1
  - Q output = 0
  - an input of S=1, R=0 causes a transition to state 2
  - any other input leaves the circuit in state 1
  - (an input of S=R=1 is not allowed for RS flip-flops)
- In state 2
  - Q output = 1
  - an input of S=0, R=1 causes a transition to state 1
  - any other input leaves the circuit in state 2

State Table of RS-Flip-Flop

- A state table is a tabular form of the state diagram
  - one row for each possible state
- Shows the next state which will be entered for all possible combinations of inputs
- The ordering of the inputs is same as for Karnaugh map

- Example

Present State	Next state inputs: SR			
	00	01	11	10
1	1	1	X	2
2	2	1	X	2

- The circuits is in state 2; the inputs are S=1, R=0. What is the next state?
  - state 2

Assigned State Table of RS-Flip-Flop

- Differs from a State Table by showing the associated outputs not the state numbers
- Example

Present Output	Next output inputs: SR			
	00	01	11	10
0	0	0	X	1
1	1	0	X	1

- The output of the circuits is 1; the inputs are S=1, R=0. What is the next output?
  - 1

Boolean Expression from Assigned State Table

- We continue the example of the RS flip-flop and call the "next output" Q+
- The assigned state table defines the logical relationship between the inputs (S and R) and Q+
  - a Boolean relationship
- Hence we can re-draw the assigned state table as a Karnaugh map

Q\SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

Q\SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

- The Boolean expression is then obtained by grouping terms as usual

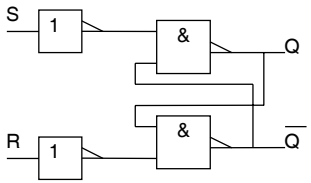
$$Q^+ = Q\overline{R} + S$$
$$\overline{Q^+} = \overline{Q}\overline{S} + R$$

- Such equations are called **characteristic equations**

Implementation from Characteristic Equations

- The flip-flop can be implemented using gates
- It is common to re-write using NAND gates only

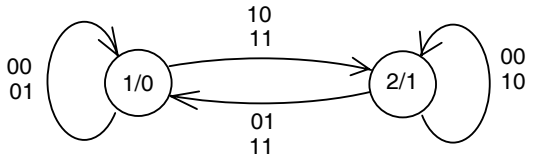
$$Q^+ = \overline{\overline{\overline{(Q\overline{R})}.\overline{S}}}$$
$$\overline{Q^+} = \overline{\overline{\overline{(\overline{Q}S)}\overline{R}}}$$



Asynchronous RS Flip-flop

JK State Implementation

- Moore Model State Diagram



- Assigned State Table

Present Output	Next output inputs: JK			
	00	01	11	10
0	0	0	1	1
1	1	0	0	1

- Characteristic Equation

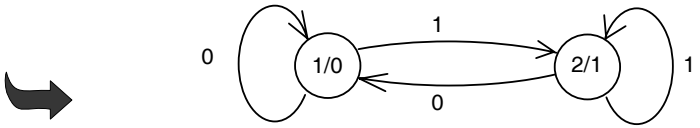
$$Q^+ = J\overline{Q} + \overline{K}Q = \overline{\overline{J\overline{Q}}.\overline{\overline{K}Q}}$$

  - when J=1, K=0 then Q+ = $\overline{Q}$+Q = 1
  - when J=0, K=1 then Q+ = 0
  - when J=1, K=1, then Q+ = $\overline{Q}$ (toggle)

  - Note that the JK is not normally implemented directly from this equation
  - A master-slave configuration is used instead

D-type Implementation

- Moore Model State Diagram



- Assigned State Table

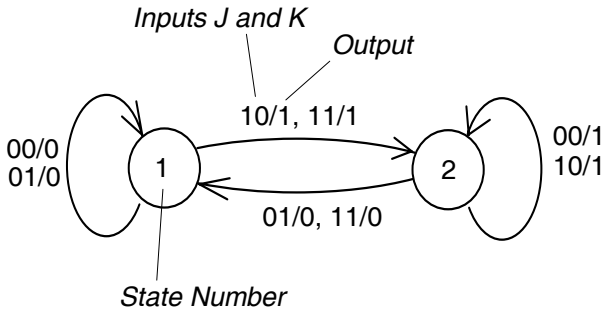
Present Output	Next output	
	0	1
0	0	1
1	0	1

Characteristic Equation

$$Q^+ = D$$

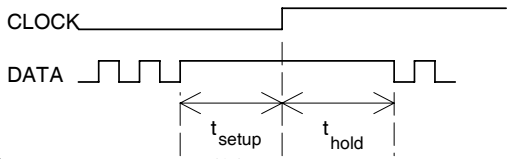
Mealy Model State Diagrams

- Similar principles to Moore model but different labelling
- State circles are labelled only with state numbers
- Outputs are written next to inputs on the arrows
- E.g. JK Flip-flop



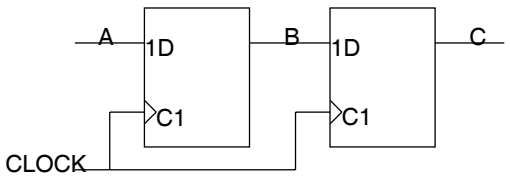
Timing Parameters of Flip-flops

- For correct operation of flip-flops
  - data inputs must not change either just before or just after clock pulses
- If data changes near the clock the flip-flop might enter a metastable state
  - neither 0 nor 1
- The amount of time before and after the clock pulse in which data transitions are not allowed are called:
  - setup and hold times
  - defined by the manufacturer



Cascaded Flip-flops

- Hold time of a flip-flop is always less than the propagation delay between CLOCK and Q
- Rising edge of CLOCK causes the data at A to go to B and data at B to go to C in example below



- What data does C end up with?
  - B doesn't change immediately because of the propagation delay
  - The input to the second flip-flop is value of B just before the CLOCK rising edge i.e. B->C; A->B
- Hence
  - This circuit shifts the data one position to the right on each clock pulse