Digital Electronics

Tutorial Sheet 11

1.* Complete the following truth tables for a JK, D and T flip-flop respectively

J	K	CL	Q+
0	0	↓	
0	1	↓	
1	0	↓	
1	1	↓	

D	CLK	Q+
0	↑	
1	↑	

T	CLK	Q+
0	↑	
1	↑	

2.** Construct a Karnaugh map for each flip-flop expressing the next value of Q in terms of the present value of Q and the inputs. Hence show how you could synthesise a T flip-flop and a JK flip-flop using D flip-flops and appropriate gates.