Digital Electronics

Tutorial Sheet 12

1.* Show that a binary down-counter can be implemented using a binary up-counter. To do this, draw the transition table for a 4-bit up-counter and for a 4-bit down counter and then consider the relationship between corresponding bits in the two tables.

2.** A 3-bit synchronous counter with a synchronous $\overline{\text{CLEAR}}$ input is connected as shown below in Figure 1. Draw a state diagram for the circuit. Draw also the modified state diagram if the $\overline{\text{CLEAR}}$ input were asynchronous? Finally, draw the modified logic symbol.

3.** The circuit below in Figure 2 uses a 4-bit synchronous binary counter with a synchronous $\overline{\text{LOAD}}$ input. The signal TC is high whenever the contents of the counter equal 15. The frequency of CLOCK is 16 kHz.

a) If N3:0 = 5, draw a state diagram for the counter.

b) If N3:0 = 5, what is the frequency of the signal OUT?

c) Derive a general formula giving the frequency of OUT in terms of the value N.

d) What is the frequency of the signal OUT if N=15?

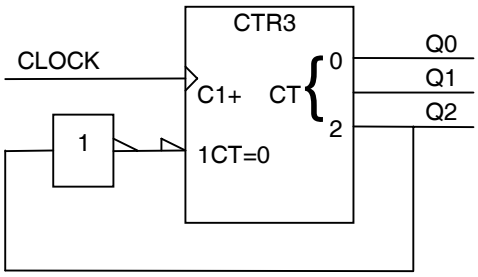

Figure 1

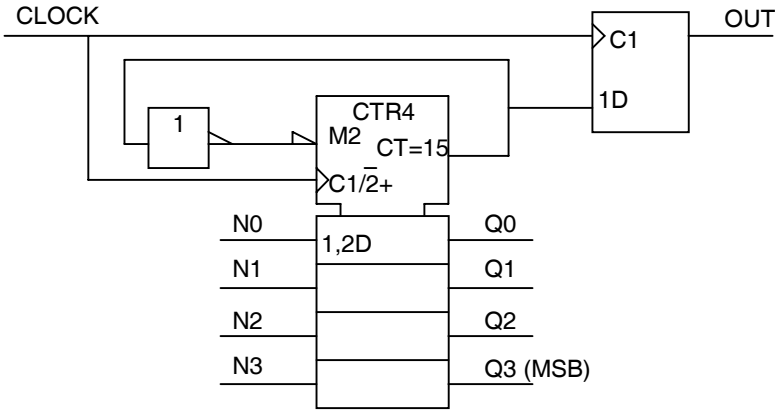

Figure 2