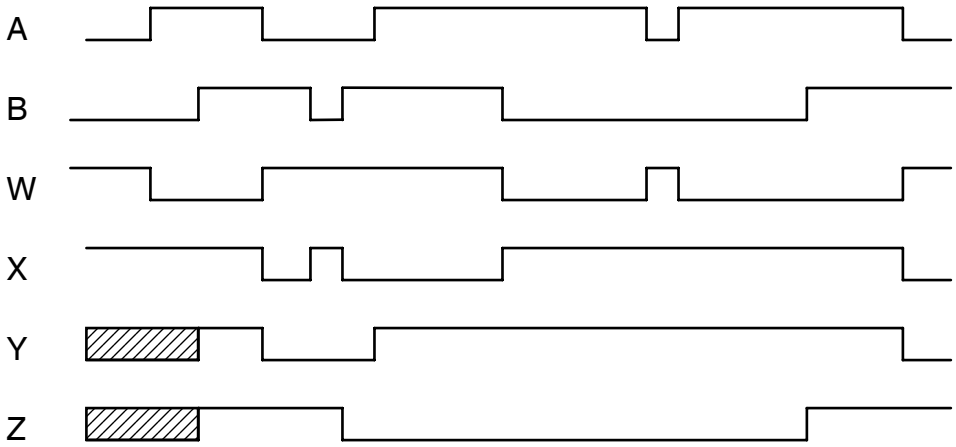
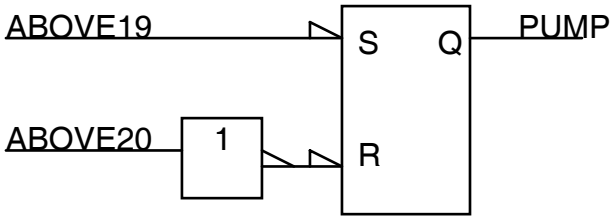
Digital Electronics

Answer Sheet 9 & 10

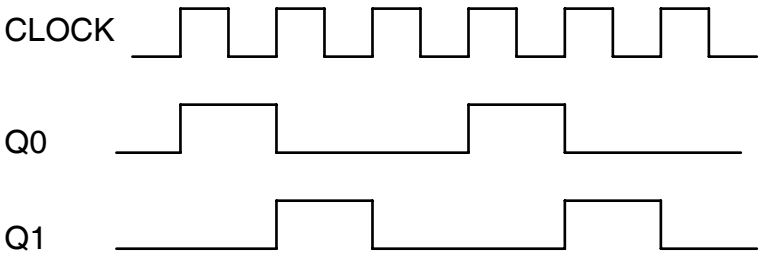
1.



2.



3.



4.

J	K	CLK	Q+
0	0	↓	Q
0	1	↓	0
1	0	↓	1
1	1	↓	$\overline{Q}$

D	CLK	Q+
0	↑	0
1	↑	1

T	CLK	Q+
0	↑	Q
1	↑	$\overline{Q}$

5. Given a D flip-flop, we have to consider what logical combination of its output and circuit inputs which, when connected to the input of the D flip-flop will cause it to operate as T or JK as appropriate. We know that D is fed to Q on the rising edge of the clock.

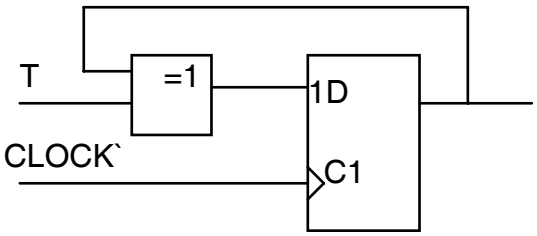
For a T flip-flop, we require

T	Q	D
0	0	0
0	1	1
1	0	1
1	1	0

Karnaugh map for D in terms of T and Q:

T\Q	0	1
0	0	1
1	1	0

Hence $D = T \oplus Q$



For a JK flip-flop, we require

J	K	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Karnaugh map for D in terms of J, K and Q:

Q\JK	00	01	11	10
0	0	0	1	1
1	1	0	0	1

Hence $D = \overline{Q}.J + Q.\overline{K}$