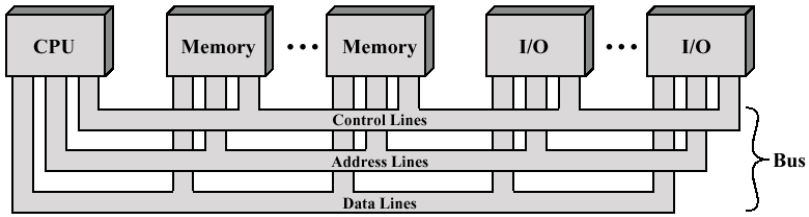
Lecture 12 - System Buses: Interfacing Processors and Peripherals

- System interconnection structures may support these transfers:
  - **Memory to processor**: the processor reads instructions and data from memory
  - **Processor to memory**: the processor writes data to memory
  - **I/O to processor**: the processor reads data from I/O device
  - **Processor to I/O**: the processor writes data to I/O device
  - **I/O to or from memory**: I/O module allowed to exchange data directly with memory without going through the processor - Direct Memory Access (DMA)

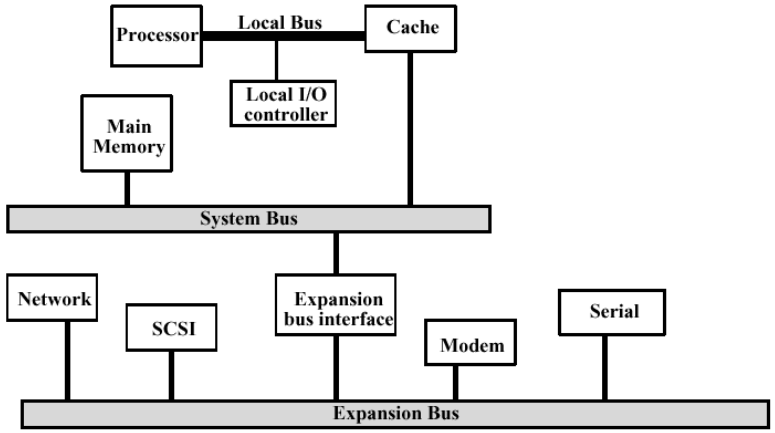


Reference: Computer Organization & Architecture (5th Ed), William Stallings

Signals found on a bus

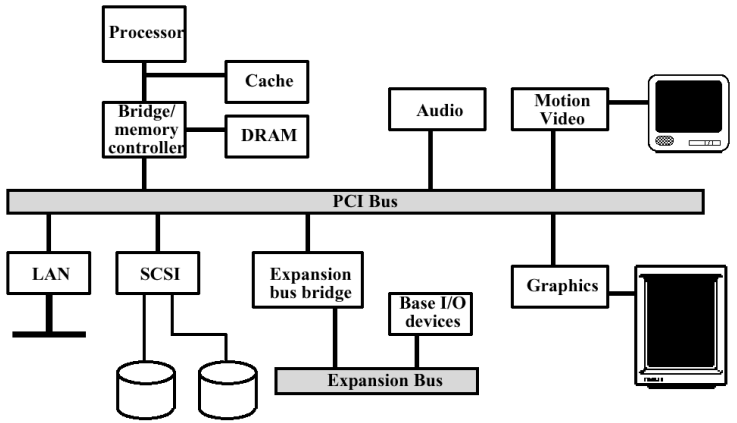
- **Address lines**
- **Data lines**
- **Control lines**:
  - **Memory write**: data on the bus written into the addressed location
  - **Memory read**: data from the addressed location placed on the bus
  - **I/O write**: data on the bus output to the addressed I/O port
  - **I/O read**: data from the addressed I/O port placed on the bus
  - **Bus REQ**: indicates a module needs to gain control of the bus
  - **Bus GRANT**: indicates that requesting module has been granted control of the bus
  - **Interrupt REQ**: indicates that an interrupt is pending
  - **Interrupt ACK**: Acknowledges that pending interrupt has been recognized
  - **Reset**: Initializes everything connected to the bus
  - **Clock**: on a synchronous bus, everything is synchronized to this signal

Traditional Bus Architecture



- Speed of expansion bus is limited.

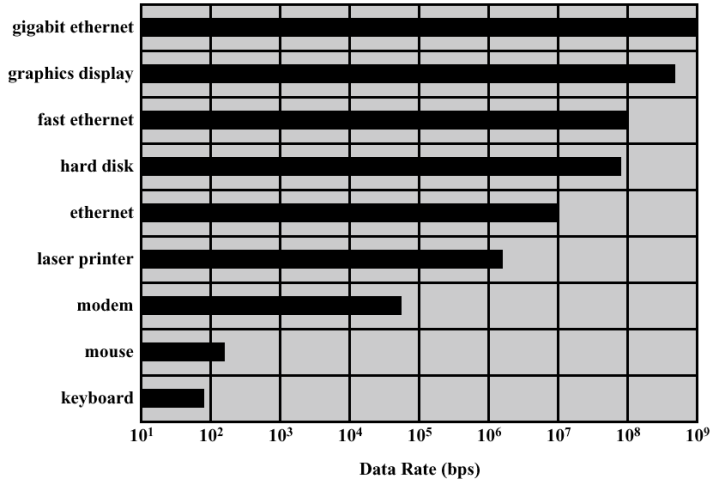
High-Performance Bus Architecture (e.g. PCI Bus)



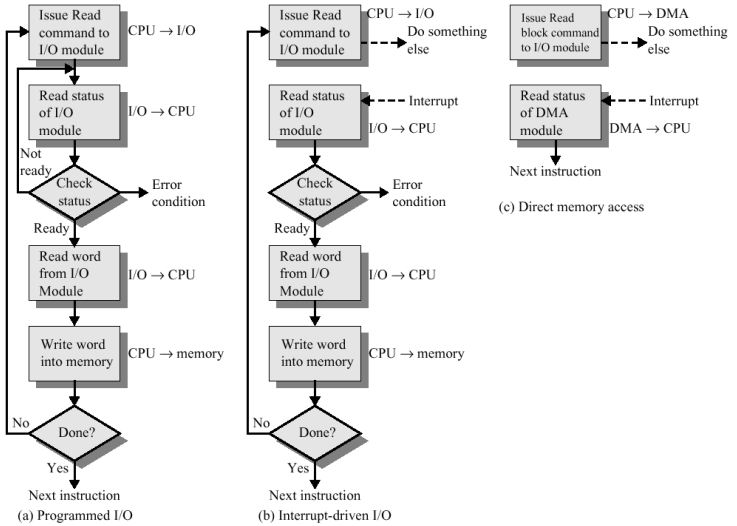
- Separate out fast local bus (PCI bus) and slower I/O expansion bus (ISA bus)

I/O Devices

- Very diverse data rate:



Techniques for Inputting a Block of Data



Polling and Interrupt

- Both are methods to notify processor that I/O device needs attention
- **Polling**
  - simple, but slow
  - processor check status of I/O device regularly to see if it needs attention
  - similar to checking a telephone without bells!
- **Interrupt**
  - fast, but more complicated
  - processor is notified by I/O device (interrupted) when device needs attention
  - similar to a telephone with bells

Direct Memory Access

- Interrupt & programmed I/O requires processor to transfer data between memory and I/O module.
- Processor is tied up in performing the transfer by executing a number of instructions - SLOW!!!
- I/O module can contain autonomous hardware to perform transfer – DMA
- DMA is stealing bus cycles from processor - a technique known as cycle stealing

Direct Memory Access (con't)

- DMA is initiated by a processor. The following information must be sent by the processor to the DMA module:
  - Tell DMA module whether a read or write is required
  - Send to the DMA module the address of the I/O device involved in the transfer
  - The starting location in memory to read from or write to - DMA module will store this locally in the address register
  - The number of word to read or write - DMA module will store this in the data count register
- Once DMA is initiated, the processor can continue with other work.
- Since processor has cache memory, it can work concurrently with transfer between I/O device and memory. (But there is extra work needed to ensure *cache coherency*)