

## ADC Architectures I: The Flash Converter

by Walt Kester

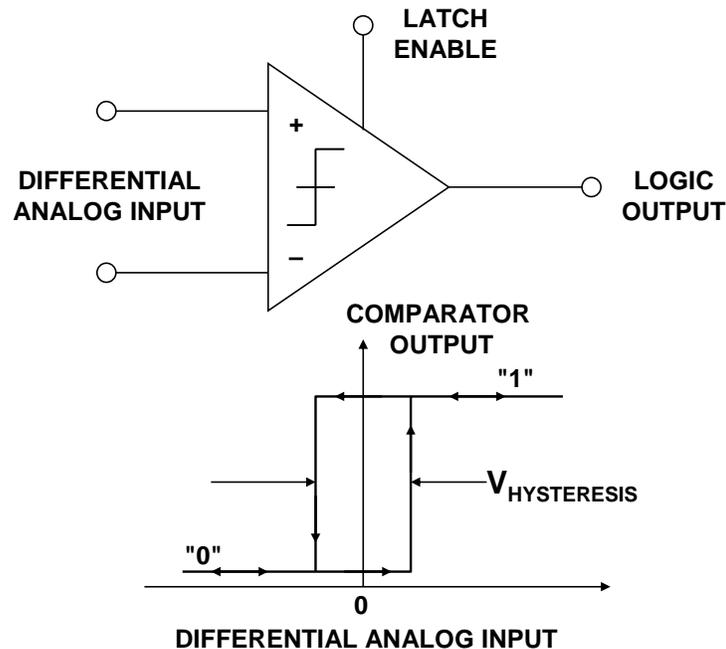
### INTRODUCTION

Commercial flash converters appeared in instruments and modules of the 1960s and 1970s and quickly migrated to integrated circuits during the 1980s. The monolithic 8-bit flash ADC became an industry standard in digital video applications of the 1980s. Today, the flash converter is primarily used as a building block within subranging "pipeline" ADCs. The lower power, lower cost pipeline architecture is capable of 8- to 10-bits of resolution at sampling rates of several hundred MHz. Therefore, higher power stand-alone flash converters are primarily used in 6- or 8-bit ADCs requiring sampling rates greater than 1 GHz. These converters are usually designed on Gallium Arsenide processes.

Because of their importance as building blocks in high resolution pipeline ADCs, it is important to understand the fundamentals of the basic flash converter. This tutorial begins with a brief discussion of the comparator which is the basic building block for flash converters.

### THE COMPARATOR: A 1-BIT ADC

As a changeover switch is a 1-bit DAC, so a comparator is a 1-bit ADC (see Figure 1). If the input is above a threshold, the output has one logic value, below it has another. Moreover, there is no ADC architecture which does not use at least one comparator of some sort.



**Figure 1: The Comparator: A 1-Bit ADC**

The most common comparator has some resemblance to an operational amplifier in that it uses a differential pair of transistors or FETs as its input stage, but unlike an op amp, it does not use external negative feedback, and its output is a logic level indicating which of the two inputs is at the higher potential. Op amps are not designed for use as comparators—they may saturate if overdriven and recover slowly.

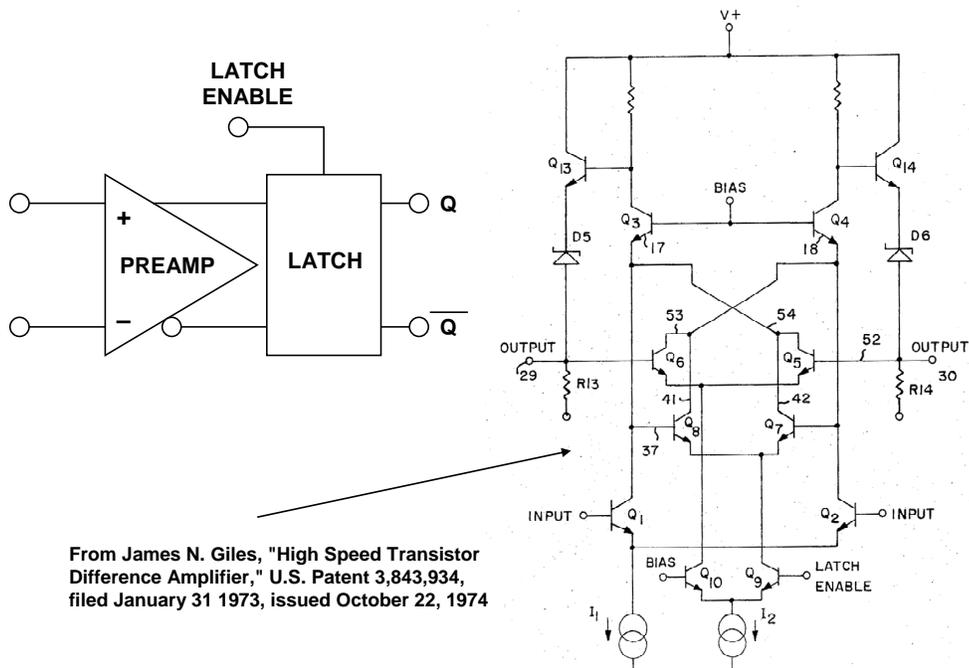
Many op amps have input stages which behave in unexpected ways when used with large differential voltages, and their outputs are rarely compatible with standard logic levels. There are cases, however, when it may be desirable to use an op amp as a comparator, and an excellent treatment of this subject can be found in Reference 1.

Comparators used as building blocks in ADCs need good resolution which implies high gain. This can lead to uncontrolled oscillation when the differential input approaches zero. In order to prevent this, "hysteresis" is often added to comparators using a small amount of positive feedback.

Figure 1 shows the effects of hysteresis on the overall transfer function. Many comparators have a millivolt or two of hysteresis to encourage "snap" action and to prevent local feedback from causing instability in the transition region. Note that the resolution of the comparator can be no less than the hysteresis, so large values of hysteresis are generally not useful.

Early comparators were designed with vacuum tubes and were often used in radio receivers—where they were called "discriminators," not comparators. Most modern comparators used in ADCs include a built-in latch which makes them sampling devices suitable for data converters. A typical structure is shown in Figure 2 for the AM685 ECL (emitter-coupled-logic) latched comparator introduced in 1972 by Advanced Micro Devices, Inc. (see Reference 2).

The input stage preamplifier drives a cross-coupled latch. The latch locks the output in the logic state it was in at the instant when the latch was enabled. The latch thus performs a track-and-hold function, allowing short input signals to be detected and held for further processing. Because the latch operates directly on the input stage, the signal suffers no additional delays—signals only a few nanoseconds wide can be acquired and held. The latched comparator is also less sensitive to instability caused by local feedback than an unlatched one.



**Figure 2: The AM685 ECL Comparator (1972)**

Where comparators are incorporated into IC ADCs, their design must consider resolution, speed, overload recovery, power dissipation, offset voltage, bias current, and the chip area occupied by the architecture which is chosen. There is another subtle but troublesome characteristic of comparators which can cause large errors in ADCs if not understood and dealt with effectively. This error mechanism is the occasional inability of a comparator to resolve a small differential input into a valid output logic level. This phenomenon is known as "metastability"—the ability of a comparator to balance right at its threshold for a short period of time.

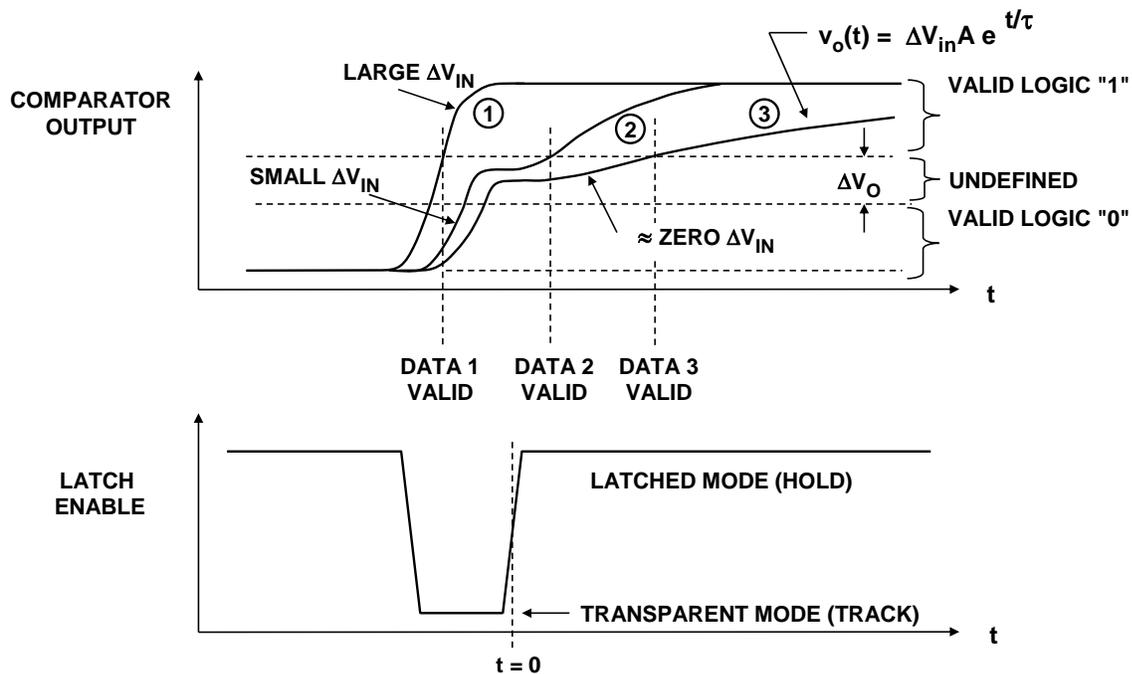
The metastable state problem is illustrated in Figure 3. Three conditions of differential input voltage are illustrated: (1) large differential input voltage, (2) small differential input voltage, and (3) zero differential input voltage. The approximate equation which describes the output voltage,  $V_O(t)$  is given by:

$$V_O(t) = \Delta V_{IN} A e^{t/\tau}, \tag{Eq. 1}$$

Where  $\Delta V_{IN}$  = the differential input voltage at the time of latching,  $A$  = the gain of the preamp at the time of latching,  $\tau$  = regeneration time constant of the latch, and  $t$  = the time that has elapsed after the comparator output is latched (see References 3 and 4).

For small differential input voltages, the output takes longer to reach a valid logic level. If the output data is read when it lies between the "valid logic 1" and the "valid logic 0" region, the data can be in error. If the differential input voltage is exactly zero, and the comparator is perfectly balanced at the time of latching, the time required to reach a valid logic level can be quite long (theoretically infinite). However, hysteresis and noise on the input makes this

condition highly unlikely. The effects of invalid logic levels out of the comparator are different depending upon how the comparator is used in the actual ADC.



**Figure 3: Comparator Metastable State Errors**

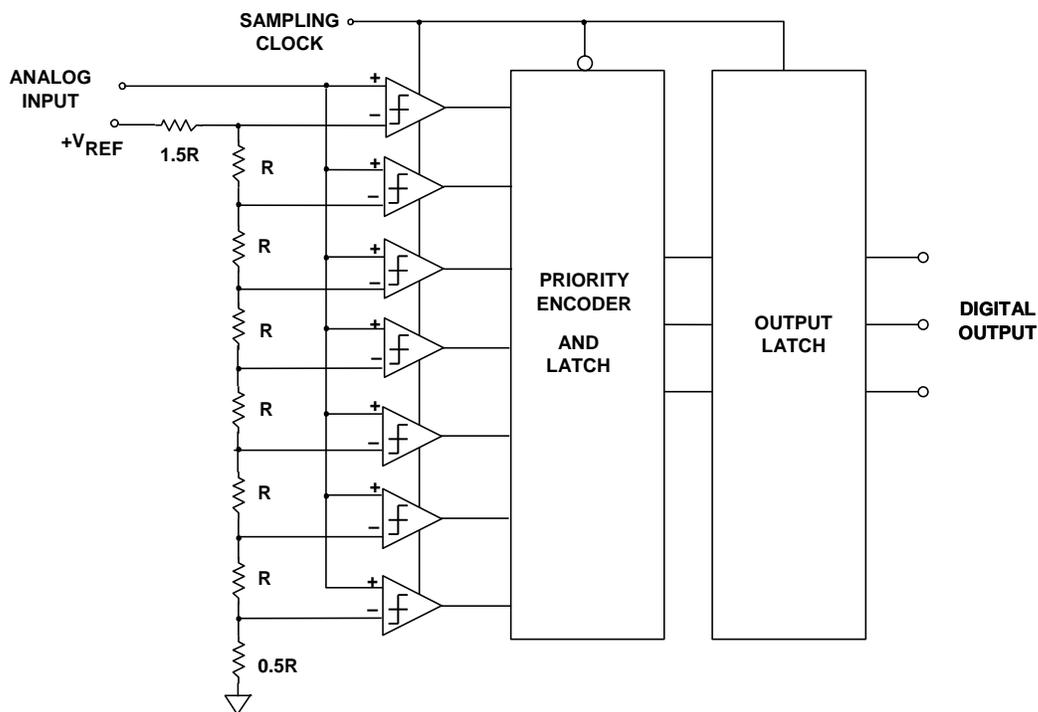
From a design standpoint, comparator metastability can be minimized by making the gain,  $A$ , high, minimizing the regeneration time constant,  $\tau$ , by increasing the gain-bandwidth of the latch, and allowing sufficient time,  $t$ , for the output of the comparator to settle to a valid logic level. It is not the purpose of this discussion to analyze the complex tradeoffs between speed, power, and circuit complexity when optimizing comparator designs, but an excellent treatment of the subject can be found in References 3 and 4.

From a user standpoint, the effect of comparator metastability (if it affects the ADC performance at all) is in the "bit error rate" (BER)—which is not usually specified on most ADC data sheets. The resulting errors are often referred to as "sparkle codes", "rabbits", or "flyers."

Bit error rate should not be a problem in a properly designed ADC in most applications, however the system designer should be aware that the phenomenon exists. An application example where it can be a problem is when the ADC is used in a digital oscilloscope to detect small-amplitude single-shot randomly occurring events. The ADC can give false indications if its BER is not sufficiently small. More discussion of sparkle codes can be found in [Tutorial MT-011](#).

## FLASH CONVERTERS

Flash ADCs (sometimes called "parallel" ADCs) are the fastest type of ADC and use large numbers of comparators. An N-bit flash ADC consists of  $2^N$  resistors and  $2^N - 1$  comparators arranged as in Figure 4. Each comparator has a reference voltage from the resistor string which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input voltage larger than their reference voltage and a "1" logic output, and all the comparators above that point will have a reference voltage larger than the input voltage and a "0" logic output. The  $2^N - 1$  comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a "thermometer" code. Since  $2^N - 1$  data outputs are not really practical, they are processed by a decoder to generate an N-bit binary output.



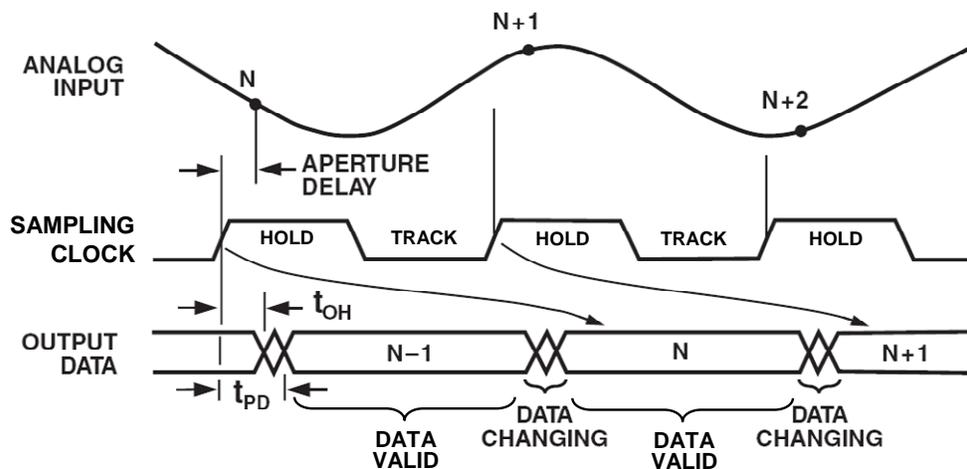
**Figure 4: 3-bit All-Parallel (Flash) Converter**

The input signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder N-bit output by only a few gate delays on top of that, so the process is very fast. In addition, the individual comparators provide an inherent "sample-and-hold" function, so theoretically a flash converter does not need a separate SHA, provided the comparators are perfectly dynamically matched. In practice, however, the addition of a proper external sample-and-hold usually enhances the dynamic performance of most flash converters because of the inevitable slight timing mismatches which occur between comparators.

Because the flash converter uses large numbers of resistors and comparators and is limited to low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation because of the large number of high speed comparators (especially at sampling rates greater than 50 MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents (typically  $> 10$  mA).

## TYPICAL FLASH CONVERTER TIMING

Simplified timing for an early commercial flash converter ([AD9048](#) 8-bit, 35 MSPS) is shown in Figure 5. The input comparators are in the "track" or "transparent" mode when the sampling clock is low. The rising edge of the sampling clock places the comparators in the "hold" or "latched" mode. During the "hold" time, the decoding logic makes its decision based on the comparator outputs. The falling edge of the sampling clock latches the decoded data into an intermediate latch. The next rising edge of the sampling clock transfers the decoded data into an output latch. Note that this results in one cycle of "pipeline delay" in the output data with respect to the corresponding sampling clock edge. The intermediate latch allows for more sophisticated two-stage decoding methods. For instance, the comparator output data might first be decoded as a Gray code, latched on the falling edge of the sampling clock, and converted to binary during the "track" interval. The two-stage decoding is often used to minimize "sparkle codes" which are due to incorrectly interpreting a comparator output. (See Tutorial [MT-011](#) for a complete discussion of sparkle codes and metastable state errors). Some flash converters use even more sophisticated decoding and therefore have more than one clock cycle of pipeline delay.



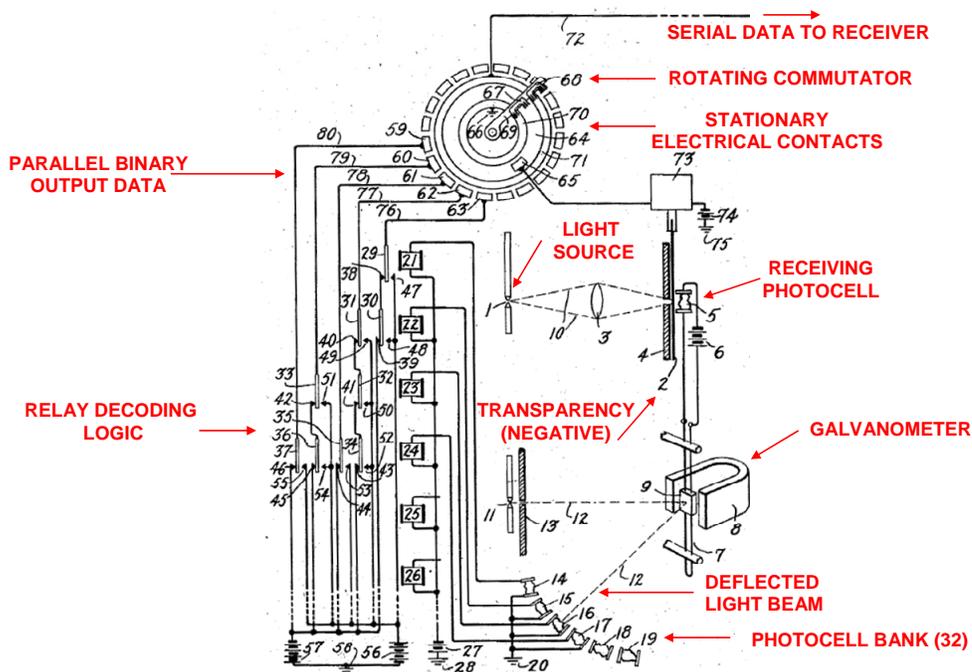
**Figure 5: Data Timing for Typical Flash Converter (AD9048 8-bit, 35 MSPS)**

If simple priority decoding is used, it would be possible to eliminate both the output latch and the intermediate latch and take the binary data directly from the output of the decoding logic. If this were the case, however, the output data is constantly changing during the "track" interval, thereby limiting the "DATA VALID" interval to one-half of the sampling clock period. It is therefore customary to use at least one latch so that the output data stays constant during the

entire sampling period, with the exception of the small amount of "DATA CHANGING" time shown in Figure 5.

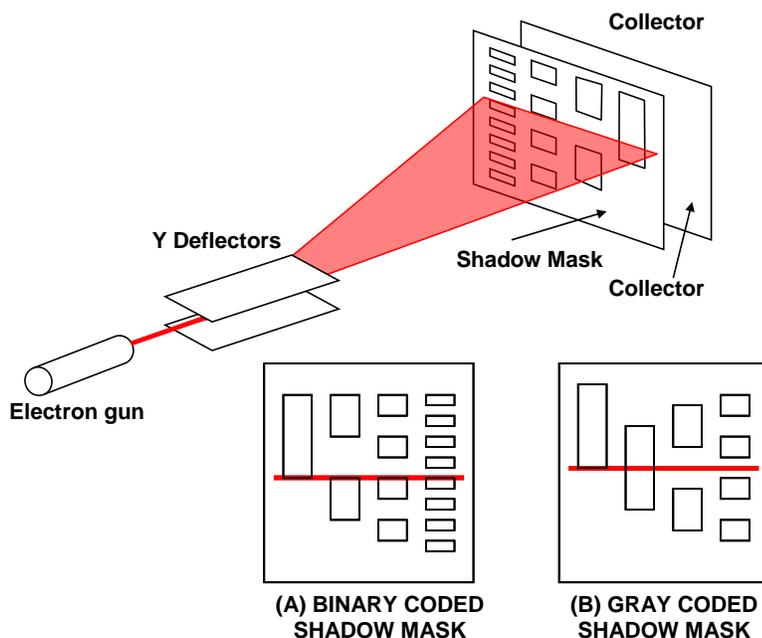
**FLASH CONVERTER HISTORICAL PERSPECTIVE**

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection. Each individual photocell output activates part of a relay network which generates the 5-bit binary code as shown in Figure 6.



**Figure 6: A 5-Bit Flash ADC Proposed by Paul Rainey  
Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent  
1,608,527, Filed July 20, 1921, Issued November 30, 1926**

A significant development in high speed ADC technology during the 1940s was the electron beam coding tube developed at Bell Labs and shown in Figure 7. The tube described by R. W. Sears in Reference 6 was capable of sampling at 96 kSPS with 7-bit resolution. The basic electron beam coder concepts are shown in Figure 6 for a 4-bit device. The tube used a fan-shaped beam creating a "flash" converter delivering a parallel output word.



**Figure 7: The Electron Beam Coder from Bell Labs (1948)**

Early electron tube coders used a binary-coded shadow mask (Figure 7A), and large errors can occur if the beam straddles two adjacent codes and illuminates both of them. The errors associated with binary shadow masks were later eliminated by using a Gray code shadow mask as shown in Figure 7B. This code was originally called the "reflected binary" code, and was invented by Elisha Gray in 1878, and later re-invented by Frank Gray in 1949 (see Reference 7). The Gray code has the property that adjacent levels differ by only one digit in the corresponding Gray-coded word. Therefore, if there is an error in a bit decision for a particular level, the corresponding error after conversion to binary code is only one least significant bit (LSB). In the case of midscale, note that only the MSB changes. It is interesting to note that this same phenomenon can occur in modern comparator-based flash converters due to comparator metastability. With small overdrive, there is a finite probability that the output of a comparator will generate the wrong decision in its latched output, producing the same effect if straight binary decoding techniques are used. In many cases, Gray code, or "pseudo-Gray" codes are used to decode the comparator bank output before finally converting to a binary code output.

In spite of the many mechanical and electrical problems relating to beam alignment, electron tube coding technology reached its peak in the mid-1960s with an experimental 9-bit coder capable of 12-MSPS sampling rates (Reference 8). Shortly thereafter, however, advances in all solid-state ADC techniques made the electron tube technology obsolete.

It was soon recognized that the flash converter offered the fastest sampling rates compared to other architectures, but the problem with this approach is that the comparator circuit itself is quite bulky using discrete transistor circuits and very cumbersome using vacuum tubes.

Constructing a single latched comparator cell using either technology is quite a task, and extending it to even 4-bits of resolution (15 comparators required) makes it somewhat unreasonable. Nevertheless, work was done in the mid 1950s and early 1960s as shown in Robert Staffin and Robert D. Lohman's patent which describes a subranging architecture using both tube and transistor technology (Reference 9). The patent discusses the problem of the all-parallel approach and points out the savings by dividing the conversion process into a coarse conversion followed by a fine conversion.

Tunnel (Esaki) diodes were used as comparators in several experimental early flash converters in the 1960s as an alternative to a latched comparator based solely on tubes or transistors (see References 10-13).

In 1964 Fairchild introduced the first IC comparators, the  $\mu$ A711/712, designed by Bob Widlar. The same year, Fairchild also introduced the first IC op amp, the  $\mu$ A709—another Widlar design. Other IC comparators soon followed including the Signetics 521, National LM361, Motorola MC1650 (1968), AM685/687 (1972/1975). With the introduction of these building block comparators and the availability of TTL and ECL logic ICs, 6-bit rack-mounted discrete flash converters were introduced by Computer Labs, Inc., including the VHS-630 (6-bit, 30 MSPS in 1970) and the VHS-675 (6-bit, 75 MSPS in 1975). The VHS-675 shown in Figure 8 used 63 AM685 ECL comparators preceded by a high-speed track-and-hold, ECL decoding logic, contained a built-in linear power supply (ac line powered), and dissipated a total of 130 W (sale price was about \$10,000 in 1975). Instruments such as these found application in early high speed data acquisition applications including military radar receivers.



19" x 17" x 7"

**VHS-630**

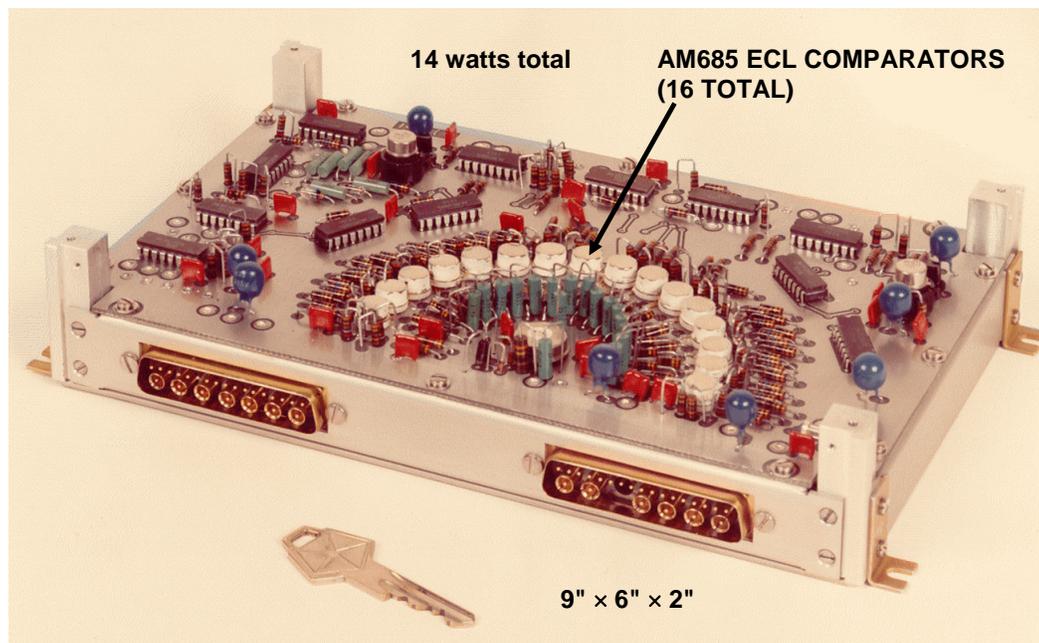
- ◆ 6-Bits, 30 MSPS
- ◆ 32 dual MC1650 MECL III Comparators
- ◆ 100 watts (linear power supplies included)

**VHS-675**

- ◆ 6-Bits, 75 MSPS
- ◆ 64 AM685 Comparators
- ◆ 130 watts (linear power supplies included)

**Figure 8: VHS-Series ADCs from Computer Labs, Inc. VHS-630 (1970), VHS-675 (1975)**

The AM685 comparator was also used as a building block in the 4-bit 100-MSPS board-level flash ADC, the MOD-4100, introduced in 1975 and shown in Figure 9.



**Figure 9: MOD-4100 4-Bit, 100-MSPS Flash Converter, Computer Labs, 1975**

The first integrated circuit 8-bit video-speed 30-MSPS flash converter, the TDC1007J, was introduced by TRW LSI division in 1979 (References 14 and 15). A 6-bit version of the same design, the TDC1014J followed shortly. Also in 1979, Advanced Micro Devices, Inc. introduced the AM6688, a 4-bit 100-MSPS IC flash converter.

Monolithic flash converters became very popular in the 1980s for high speed 8-bit video applications as well as building blocks for higher resolution subranging card-level, modular, and hybrid ADCs. Examples from Analog Devices included the popular [AD9048](#) (8-bit, 35 MSPS) and the [AD9002](#) (8-bit, 150 MSPS). Many flash converters were fabricated on CMOS processes for lower power dissipation. Recently, however, the subranging pipeline architecture has become popular for 8-bit ADCs up to about 250 MSPS. For instance, the [AD9480](#) 8-bit 250-MSPS ADC is fabricated on a high speed BiCMOS process and dissipates less than 400mW compared to the several watts required for a full flash implementation on a similar process.

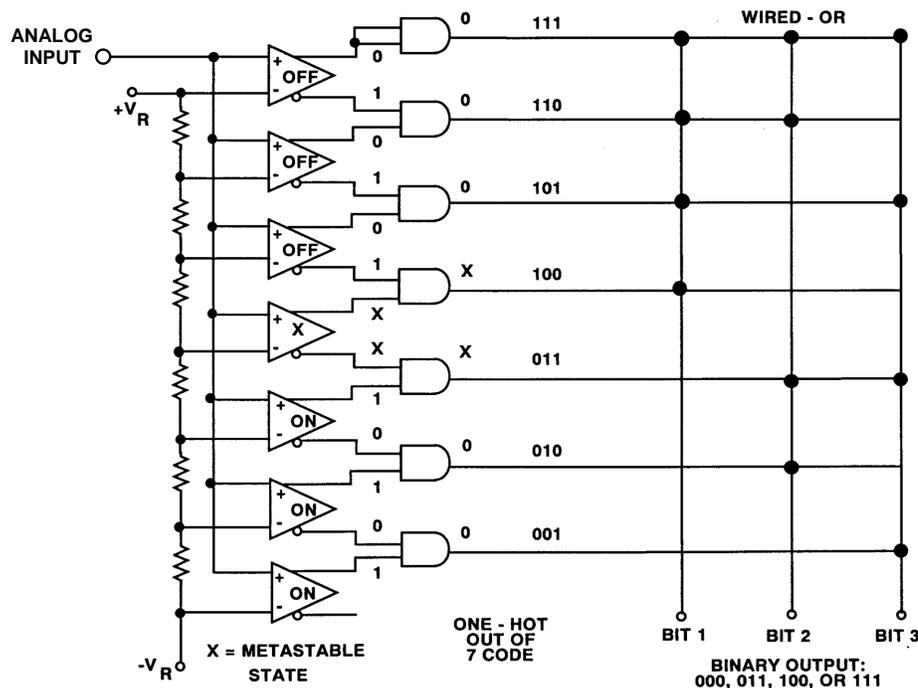
In practice, IC flash converters are currently available up to 10-bits, but more commonly they have 6- or 8-bits of resolution. Their maximum sampling rate can be as high as 1 GHz (these are generally made on Gallium Arsenide processes with several watts of power dissipation), with input full-power bandwidths in excess of 300 MHz.

But as mentioned earlier, full-power bandwidths are not necessarily full-resolution bandwidths. Ideally, the comparators in a flash converter are well matched both for dc and ac characteristics.

Because the sampling clock is applied to all the comparators simultaneously, the flash converter is inherently a sampling converter. In practice, there are delay variations between the comparators and other ac mismatches which cause a degradation in the effective number of bits (ENOBs) at high input frequencies. This is because the inputs are slewing at a rate comparable to the comparator conversion time. For this reason, track-and-holds are often required ahead of flash converters to achieve high SFDR on high frequency input signals.

The input to a flash ADC is applied in parallel to a large number of comparators. Each has a voltage-variable junction capacitance, and this signal-dependent capacitance results in most flash ADCs having reduced ENOB and higher distortion at high input frequencies. For this reason, most flash converters must be driven with a wideband op amp which is tolerant to the capacitive load presented by the converter as well as high speed transients developed on the input.

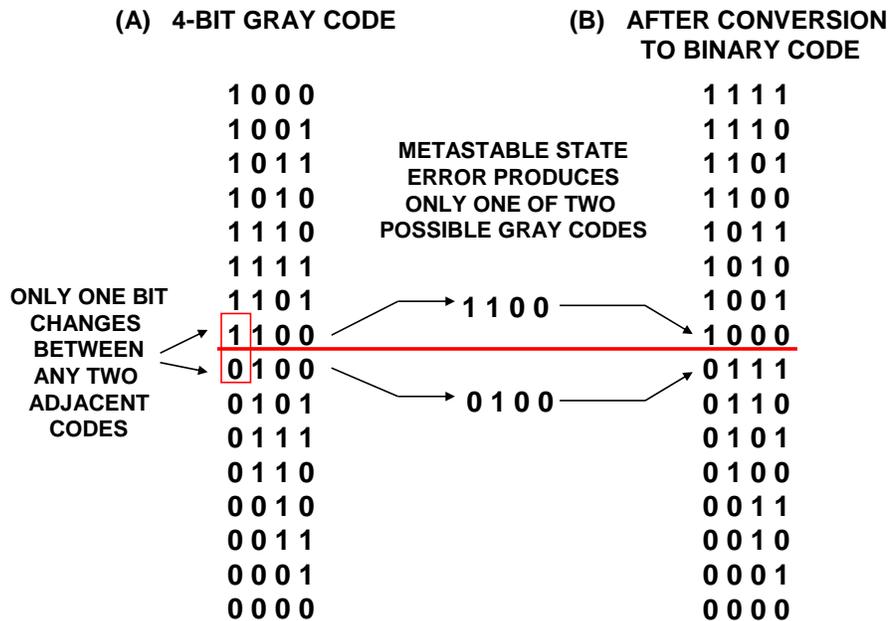
Comparator metastability in a flash converter can severely impact the bit error rate (BER). Figure 10 shows a simple flash converter with one stage of binary decoding logic. The two-input AND gates convert the thermometer code output of the parallel comparators into a "one-hot out of 7" code. The decoding logic is simply a "wired-or" array, a technique popular with emitter-coupled logic (ECL). Assume that the comparator labeled "X" has metastable outputs labeled "X". The desired output code should be either 011 or 100, but note that the 000 code (both gate outputs high) and the 111 code (both gate outputs low) are also possible due to the metastable states, representing a 1/2 FS error.



**Figure 10: Metastable Comparator Output States May Cause Error Codes in Data Converters**

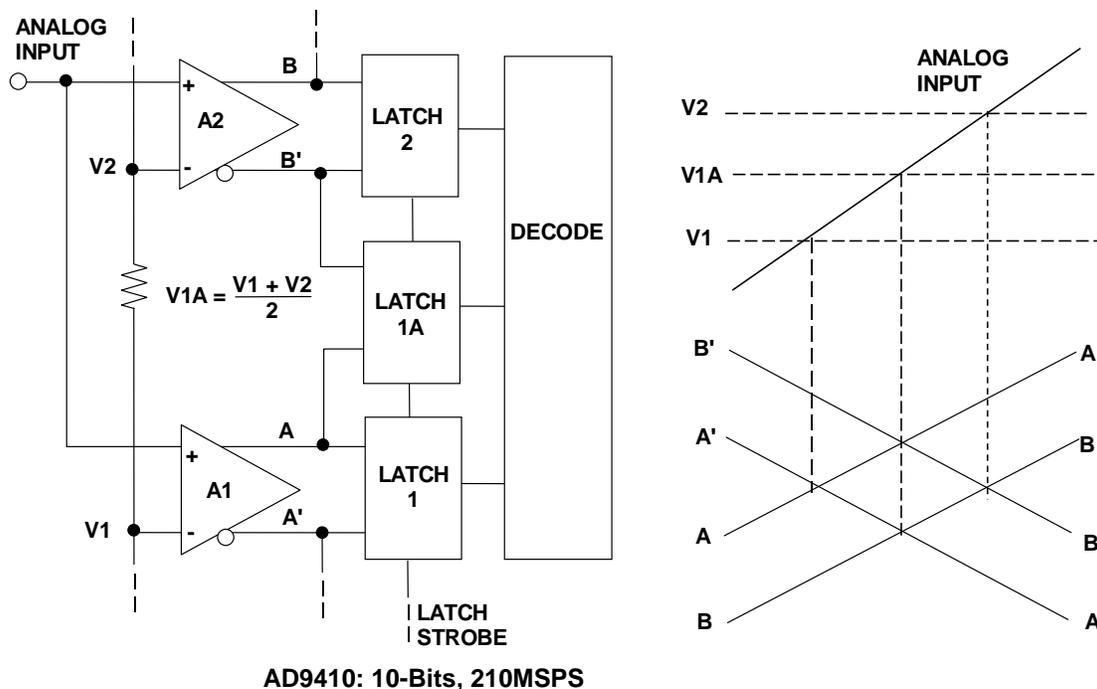
Metastable state errors in flash converters can be reduced by several techniques, one of which involves decoding the comparator outputs in Gray code followed by a Gray-to-binary conversion as in the Bell Labs electron beam encoder previously described. The advantage of Gray code decoding is that a metastable state in any of the comparators can produce only a 1-LSB error in the Gray code output. The Gray code is latched and then converted into a binary code which, in turn, will only have a maximum of 1-LSB error as shown in Figure 11.

The same principles have been applied to several modern IC flash converters to minimize the effects of metastable state errors as described in References 3, 16, 17, for example.



**Figure 11: Gray Code Decoding Reduces Amplitude of Metastable State Errors**

Power dissipation is always a big consideration in flash converters, especially at resolutions above 8 bits. A clever technique was used in the [AD9410](#) 10-bit, 210-MSPS ADC called "interpolation" to minimize the number of preamplifiers in the flash converter comparators and also reduce the power. The method is shown in Figure 12 (see Reference 18).



**Figure 12: "Interpolating" Flash Reduces the Number of Preamplifiers by Factor of Two**

The preamplifiers (labeled "A1", "A2", etc.) are low-gain  $g_m$  stages whose bandwidth is proportional to the tail currents of the differential pairs. Consider the case for a positive-going ramp input which is initially below the reference to AMP A1,  $V_1$ . As the input signal approaches  $V_1$ , the differential output of A1 approaches zero (i.e.,  $A = A'$ ), and the decision point is reached. The output of A1 drives the differential input of LATCH 1. As the input signals continues to go positive, A continues to go positive, and B' begins to go negative. The interpolated decision point is determined when  $A = B'$ . As the input continues positive, the third decision point is reached when  $B = B'$ . This novel architecture reduces the ADC input capacitance and thereby minimizes its change with signal level and the associated distortion. The AD9410 also uses an input sample-and-hold circuit for improved ac linearity.

## SUMMARY

The flash converter still maintains its position as the fastest possible ADC architecture for a given IC process. However, power and real estate considerations generally limit the resolution to 6 or 8 bits. Commercial Gallium Arsenide flash converters are available with sampling rates over 1 GHz, however cost and power dissipation limit their popularity. Higher resolution, lower power, lower cost ADCs can be implemented at lower sampling rates (up to a few hundred MSPS) using the "pipeline" architecture. This technique makes use of low resolution flash converters as building blocks and is discussed in [Tutorial MT-023](#).

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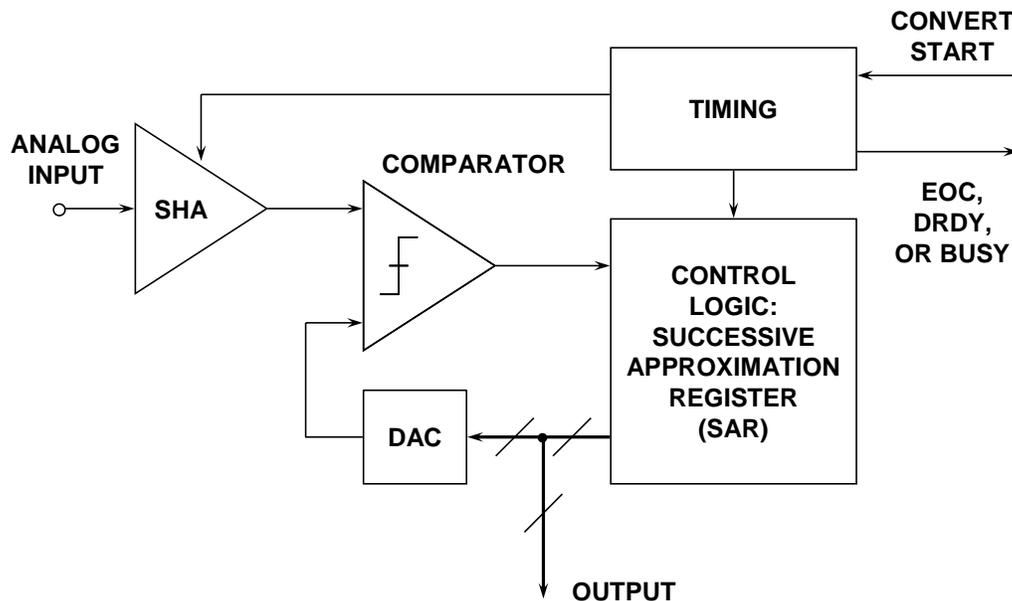
## ADC Architectures II: Successive Approximation ADCs

by Walt Kester

### INTRODUCTION

The successive approximation ADC has been the mainstay of data acquisition systems for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region with 18-bit resolution. The Analog Devices PulSAR<sup>®</sup> family of SAR ADCs uses internal switched capacitor techniques along with auto calibration and offers 18-bits at 2 MSPS ([AD7641](#)) on CMOS processes without the need for expensive thin-film laser trimming. At the 16-bit level, the [AD7625](#) (6 MSPS) and [AD7626](#) (10 MSPS) also represent breakthrough technology.

The basic successive approximation ADC is shown in Figure 1. It performs conversions on command. In order to process ac signals, SAR ADCs must have an input sample-and-hold (SHA) to keep the signal constant during the conversion cycle.



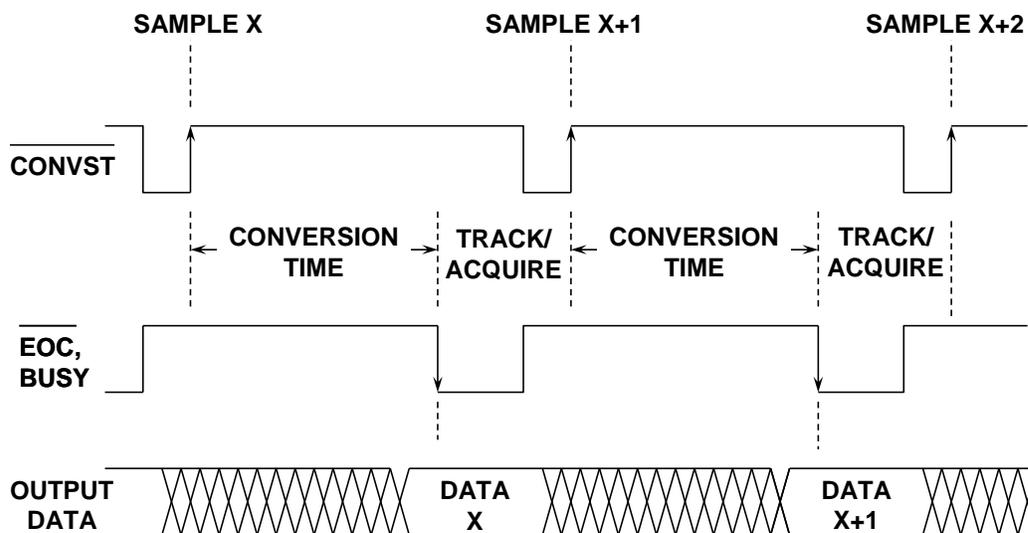
**Figure 1: Basic Successive Approximation ADC  
(Feedback Subtraction ADC)**

On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the *hold* mode, and the internal DAC is set to midscale. The comparator determines whether the SHA output is above or below the DAC output, and the result (bit 1, the most significant bit of the conversion) is stored in the successive approximation register (SAR). The DAC is then set either to  $\frac{1}{4}$  scale or  $\frac{3}{4}$  scale (depending on the value of bit 1), and the comparator makes the decision for bit 2 of the conversion. The result is stored in the register, and the process continues

until all of the bit values have been determined. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit "tests" form the basis of a serial output version SAR-based ADC. Note that the acronym "SAR" actually stands for Successive Approximation Register (the logic block that controls the conversion process), but is universally accepted as the acronym for the architecture itself.

## SAR ADC TIMING

The fundamental timing diagram for a typical SAR ADC is shown in Figure 2. The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, *not*-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed, at which time it goes low (or high). The trailing edge is generally an indication of valid output data, but the data sheet should be carefully studied—in some ADCs additional delay is required before the output data is valid.



**Figure 2: Typical SAR ADC Timing**

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward. The conversion process is generally initiated by asserting a

CONVERT START signal. The  $\overline{\text{CONVST}}$  signal is a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm. The negative-going edge of the  $\overline{\text{CONVST}}$  pulse causes the  $\overline{\text{EOC}}$  or BUSY line to go high. When the conversion is complete, the BUSY line goes low, indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register. However, because of the many variations in terminology and design, the individual data sheet should always be consulted when using a specific ADC. An important characteristic of a SAR ADC is that at the end of the conversion time, the data corresponding to the sampling clock edge is available with no "pipeline" delay. This makes the SAR ADC especially easy to use in "single-shot" and multiplexed applications.

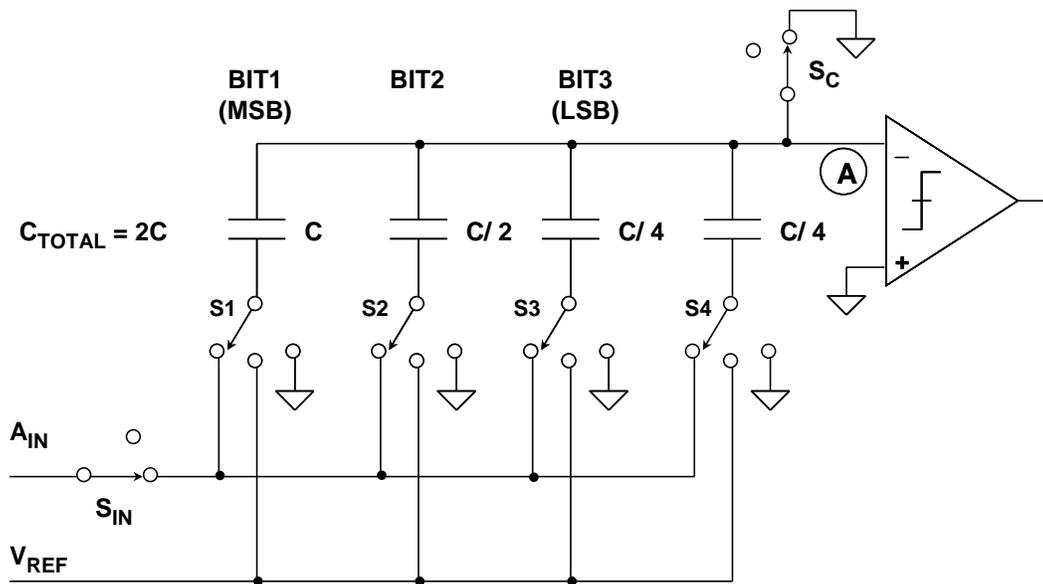
It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases there is no need to synchronize the CONVERT START command to the high frequency clock. The frequency of the external clock, if required, generally falls in the range of 1 MHz to 30 MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal oscillator which is used to perform the conversions and only require the CONVERT START command. Because of their architecture, SAR ADCs generally allow single-shot conversion at any repetition rate from dc to the converter's maximum conversion rate—however, there are some exceptions, so the data sheet should always be consulted.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by high-accuracy photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1 ppm/°C, thereby offering a high degree of temperature stability. Modern fine-line CMOS processes are ideal for the switched capacitor SAR ADC, and the cost is therefore low.

A simple 3-bit capacitor DAC is shown in Figure 3. The switches are shown in the *track*, or *sample* mode where the analog input voltage,  $A_{\text{IN}}$ , is constantly charging and discharging the parallel combination of all the capacitors. The *hold* mode is initiated by opening  $S_{\text{IN}}$ , leaving the sampled analog input voltage on the capacitor array. Switch  $S_{\text{C}}$  is then opened allowing the voltage at node A to move as the bit switches are manipulated. If  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$  are all connected to ground, a voltage equal to  $-A_{\text{IN}}$  appears at node A. Connecting  $S_1$  to  $V_{\text{REF}}$  adds a voltage equal to  $V_{\text{REF}}/2$  to  $-A_{\text{IN}}$ . The comparator then makes the MSB bit decision, and the SAR

either leaves S1 connected to  $V_{REF}$  or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive, respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and  $S_{IN}$  are connected to  $A_{IN}$ ,  $S_C$  is connected to ground, and the converter is ready for another cycle.



SWITCHES SHOWN IN TRACK (SAMPLE) MODE

**Figure 3: 3-Bit Switched Capacitor DAC**

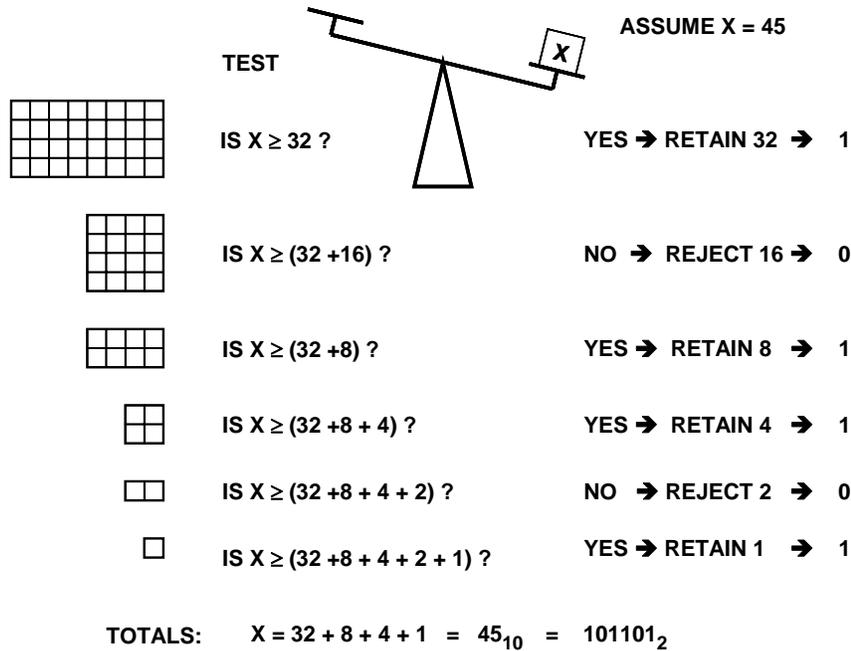
Note that the extra LSB capacitor ( $C/4$  in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to  $2C$  so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R-2R resistive DAC. When a particular bit capacitor is switched to  $V_{REF}$ , the voltage divider created by the bit capacitor and the total array capacitance ( $2C$ ) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is subtracted from node A.

### HISTORICAL PERSPECTIVES ON SAR ADCS

The basic algorithm used in the successive approximation (initially called *feedback subtraction*) ADC conversion process can be traced back to the 1500s relating to the solution of a certain mathematical puzzle regarding the determination of an unknown weight by a minimal sequence of weighing operations (Reference 1). In this problem, as stated, the object is to determine the least number of weights which would serve to weigh an integral number of pounds from 1 lb to 40 lb using a balance scale. One solution put forth by the mathematician Tartaglia in 1556, was to use the series of weights 1 lb, 2 lb, 4 lb, 8 lb, 16 lb, and 32 lb. The proposed weighing algorithm is the same as used in modern successive approximation ADCs. (It should be noted

that this solution will actually measure unknown weights up to 63 lb rather than 40 lb as stated in the problem). The algorithm is shown in Figure 4 where the unknown weight is 45 lbs. The balance scale analogy is used to demonstrate the algorithm.



**Figure 4: Successive Approximation ADC Algorithm**

Early implementations of the successive approximation ADC did not use either DACs or successive approximation registers but implemented similar functions in a variety of ways. In fact, early SAR ADCs were referred to as *sequential coders*, *feedback coders*, or *feedback subtractor coders*. The term *SAR ADC* came about in the 1970s when commercial successive approximation register logic ICs such as the 2503 and 2504 became available from National Semiconductor and Advanced Micro Devices. These devices were designed specifically to perform the register and control functions in successive approximation ADCs and were standard building blocks in many modular and hybrid data converters.

From a data conversion standpoint, the successive approximation ADC architecture formed the building block for the T1 PCM carrier system and is still a popular architecture today, but the exact origin of this architecture is not clear. Although countless patents have been granted relating to refinements and variations on the successive approximation architecture, they do not claim the fundamental principle.

The first mention of the successive approximation ADC architecture (actually a *sequential coder*) in the context of PCM was by J. C. Schelleng of Bell Telephone Laboratories in a patent filed in 1946 (Reference 2). The design does not use an internal DAC, but implements the approximation process in a somewhat novel manner involving the addition of binary weighted reference voltages. Details of this vacuum tube design are discussed in the patent.

A much more elegant implementation of the successive approximation ADC is described by Goodall of Bell Telephone Labs in a 1947 article (Reference 3). This ADC has 5-bit resolution and samples the voice channel at a rate of 8 kSPS. The voice signal is first sampled, and the corresponding voltage stored on a capacitor. It is then compared to a reference voltage which is equal to  $\frac{1}{2}$  the full-scale voltage. If it is greater than the reference voltage, the MSB is registered as a "1," and an amount of charge equal to  $\frac{1}{2}$  scale is subtracted from the storage capacitor. If the voltage on the capacitor is less than  $\frac{1}{2}$  scale, then no charge is removed, and the bit is registered as a "0". After the MSB decision is completed, the cycle continues for the second bit, but with the reference voltage now equal to  $\frac{1}{4}$  scale. The process continues until all bit decisions are completed. This concept of charge redistribution is similar to modern switched-capacitor DACs.

Both the Schelleng and the Goodall ADCs use a process of addition/subtraction of binary weighted reference voltages to perform the SAR algorithm. Although the DAC function is there, it is not performed using a traditional binary weighted DAC. The ADCs described by H. R. Kaiser et. al. (Reference 4) and B. D. Smith (Reference 5) in 1953 use an actual binary weighted DAC to generate the analog approximation to the input signal, similar to modern SAR ADCs. Smith also points out that non-linear ADC transfer functions can be achieved by using a non-uniformly weighted DAC. This technique formed the basis of companding voiceband codecs used in early PCM systems. (See [Tutorial MT-018](#), "Intentionally Nonlinear DACs.") Before this non-linear ADC technique was developed, linear ADCs were used, and the compression and expansion functions were performed by diode/resistor networks which had to be individually calibrated and held at a constant temperature to prevent drift errors (Reference 6).

Of course, no discussion on ADC history would be complete without crediting the truly groundbreaking work of Bernard M. Gordon at EPSCO (now Analogic, Incorporated). Gordon's 1955 patent application (Reference 7) describes an all-vacuum tube 11-bit, 50-kSPS successive approximation ADC—representing the first commercial offering of a complete converter (see Figure 5). The DATRAC was offered in a 19"  $\times$  26"  $\times$  15" housing, dissipated several hundred watts, and sold for approximately \$8000.00.

In a later patent (Reference 8), Gordon describes the details of the logic block required to perform the successive approximation algorithm. The SAR logic function was later implemented in the 1970s by National Semiconductor and Advanced Micro Devices—the popular 2502/2503/2504 family of IC logic chips. These chips were to become an integral building block of practically all modular and hybrid successive approximation ADCs of the 1970s and 1980s.

- ◆ 19" × 15" × 26"
- ◆ 150 lbs
- ◆ \$8,500.00



Courtesy,  
Analogic Corporation  
8 Centennial Drive  
Peabody, MA 01960

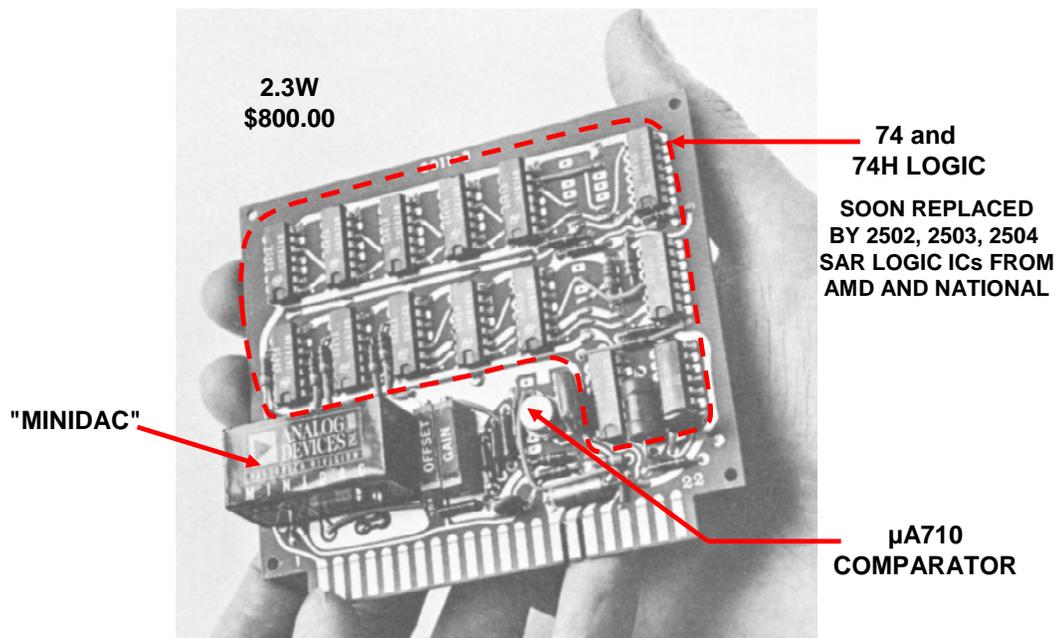
<http://www.analogic.com>

**Figure 5: 1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC  
Designed by Bernard M. Gordon at EPSCO**

## **ANALOG DEVICES ENTERS THE DATA CONVERTER ARENA IN 1969**

In 1965, Ray Stata and Matt Lorber founded Analog Devices, Inc. (ADI) in Cambridge, MA. The initial product offerings were high performance modular op amps, but in 1969 ADI acquired Pastoriza Electronics, a leader in data converter products, thereby making a solid commitment to both data acquisition and linear products.

Pastoriza had a line of data acquisition products, and Figure 6 shows a photograph of a 1969 12-bit, 10- $\mu$ s general purpose successive approximation ADC, the ADC-12U, that sold for approximately \$800.00. The architecture was successive approximation, and the ADC-12U utilized a  $\mu$ A710 comparator, a modular 12-bit "Minidac," and 14 7400-series logic packages to perform the successive approximation conversion algorithm.



**Figure 6: ADC-12U 12-Bit, 10- $\mu$ s SAR ADC from Pastoriza Division of Analog Devices, 1969**

The "Minidac" module was actually constructed from "quad switch" ICs (AD550) and a thin film network (AD850). These early DAC building blocks are discussed further in [Tutorial MT-015](#), "DAC Architectures II: Binary DACs."

Notice that in the ADC-12U, the implementation of the successive approximation algorithm required 14 logic packages. In 1958, Bernard M. Gordon had filed a patent on the logic to perform the successive approximation algorithm (Reference 19), and in the early 1970s, Advanced Micro Devices and National Semiconductor introduced commercial *successive approximation register* logic ICs: the 2502 (8-bit, serial, not expandable), 2503 (8-bit, expandable) and 2504 (12-bit, serial, expandable). These were designed specifically to perform the register and control functions in successive approximation ADCs. These became standard building blocks in many modular and hybrid data converters.

Analog Devices continued to pioneer in data conversion after 1969. Modules gradually evolved into hybrid circuits during the 1970s. Hybrids generally utilize ceramic substrates with either thick or thin film conductors. Individual die are bonded to the substrate (usually with epoxy), and wire bonds make the connections between the bond pads and the conductors. The hybrid is usually hermetically sealed in some sort of ceramic or metal package. Accuracy was achieved by trimming thick or thin film resistors after assembly and interconnection, but before sealing. Manufacturers used thin film networks, discrete thin film resistors, deposited thick or thin film resistors, or some combination of the above.



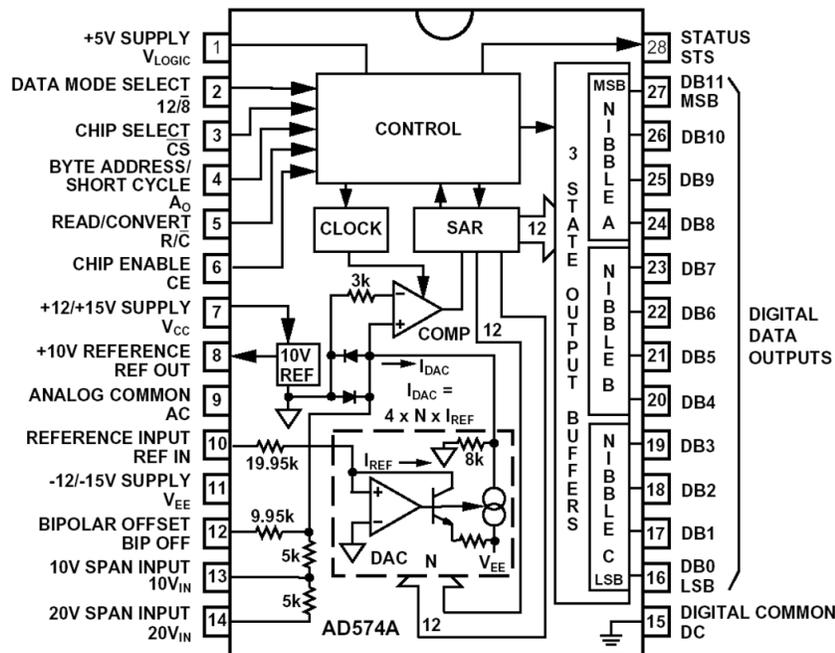


Figure 8: The Industry-Standard [AD574](#) 12-Bit, 35- $\mu$ s IC ADC, 1978

### MODERN SAR ADCs

Because of their popularity, successive approximation ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. Many SAR ADCs now offer on-chip input multiplexers, making them the ideal choice for multichannel data acquisition systems. It would be impossible to attempt to discuss all types of SAR ADCs in this tutorial, so we will only give a few highlights of modern breakthrough products.

An example of modern charge redistribution successive approximation ADCs is Analog Devices' PulSAR<sup>®</sup> series. The [AD7641](#) is a 18-bit, 2-MSPS, fully differential, ADC that operates from a single 2.5 V power supply (see Figure 9). The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, error correction circuits, internal reference, and both serial and parallel system interface ports. The AD7641 is hardware factory calibrated and comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

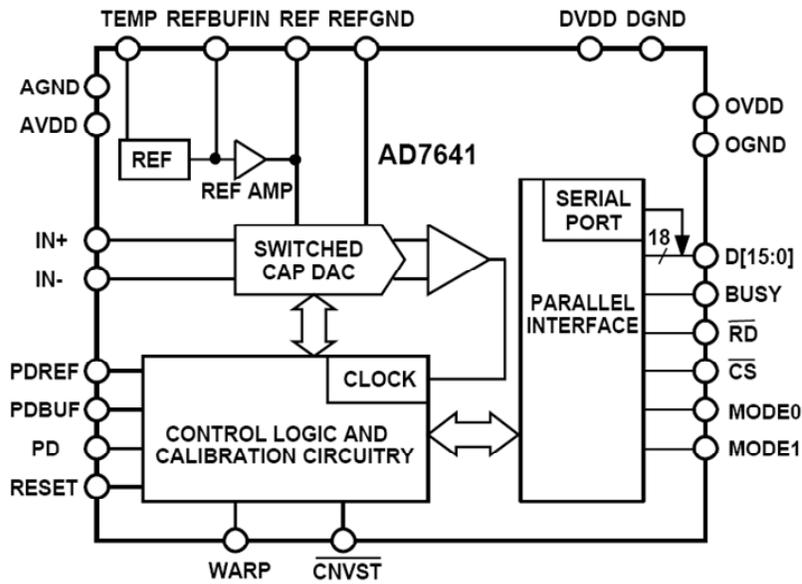


Figure 9: [AD7641](#) 18-Bit 2-MSPS Switched Capacitor PulSAR<sup>®</sup> ADC

### PROCESSING INDUSTRIAL-LEVEL SIGNALS

Many low voltage single-supply SAR ADCs have been introduced over the last few years, however their input range is usually limited to less than or equal to the supply voltage. In many situations this is not a problem; but there still exist many industrial applications which require digitization of bipolar signals (for example,  $\pm 5$  V or  $\pm 10$  V). This requires external circuitry when interfacing to single-supply ADCs. Figure 10 shows two possible approaches. An external op amp can be used to perform the level shifting and attenuation required to match the  $\pm 10$  V signal to the 0 to +2.5 V input range of the ADC (Figure 10A). An alternative is to utilize a resistor network to perform the attenuation and level shifting (Figure 10B). Both methods require external components.

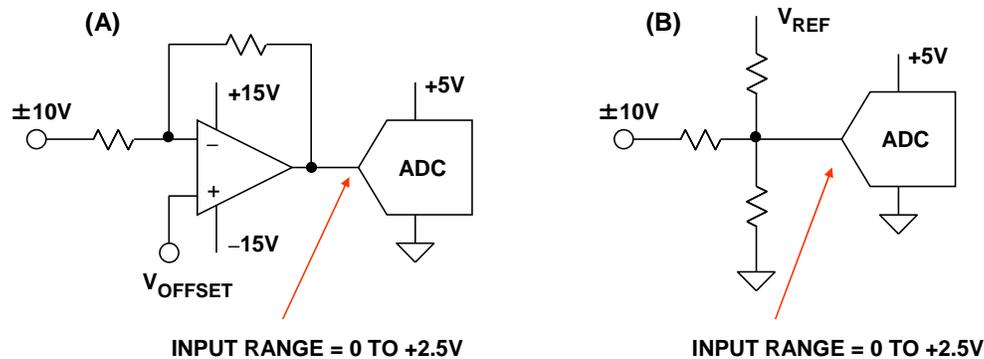
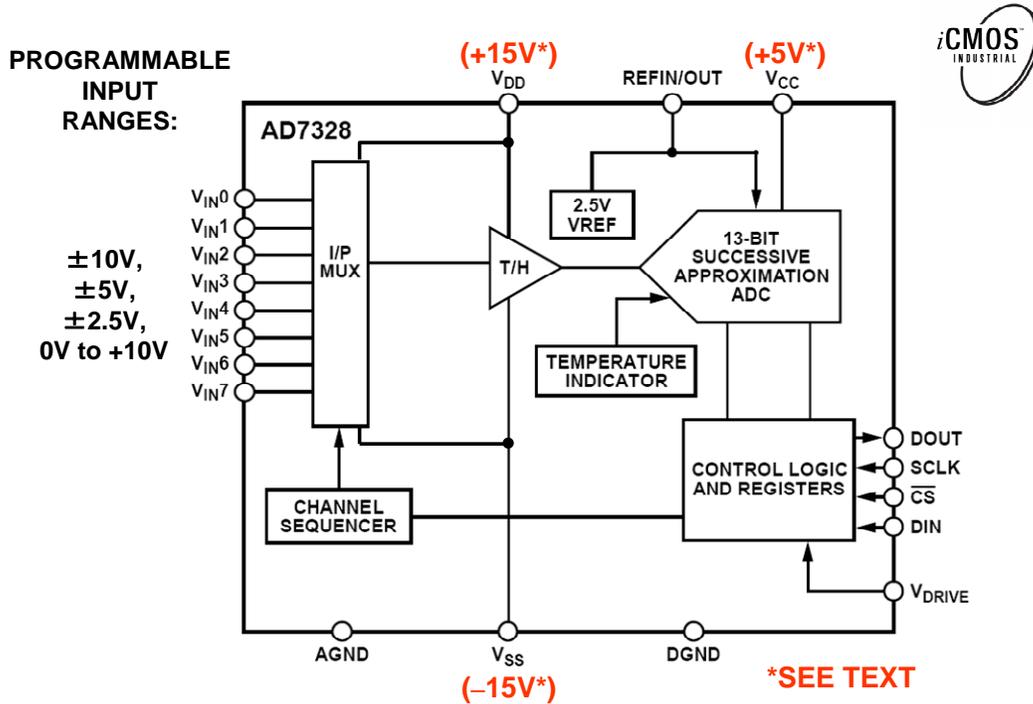


Figure 10: Interfacing Industrial-Level Bipolar Signals to Low-Voltage ADCs

A much better solution available from Analog Devices uses a proprietary industrial CMOS (*iCMOS™*) process which allows the input circuitry to operate on standard industrial  $\pm 15$  V supplies, while operating the ADC core on the low voltage supply (5 V or less). Figure 11 shows the [AD7328](#) 13-bit 8-channel input ADC.



**Figure 11: [AD7328](#) 13-Bit, 1MSPS *iCMOS™* ADC with True Bipolar Inputs**

The AD7328 is designed on the *iCMOS* (industrial CMOS) process. *iCMOS* is a process combining high voltage CMOS and low voltage CMOS. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *iCMOS* components can accept bipolar input signals while providing increased performance, dramatically reducing power consumption, and having a reduced package size. The AD7328 can accept true bipolar analog input signals. The AD7328 has four software-selectable input ranges,  $\pm 10$  V,  $\pm 5$  V,  $\pm 2.5$  V, and 0 V to 10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7328 can be programmed to be single-ended, true differential, or pseudo differential. The ADC contains a 2.5 V internal reference. The AD7328 also allows for external reference operation. If a 3 V external reference is applied to the REFIN/OUT pin, the AD7328 can accept a true bipolar  $\pm 12$  V analog input. Minimum  $\pm 12$  V  $V_{DD}$  and  $V_{SS}$  supplies are required for the  $\pm 12$  V input range.

The low voltage core of the AD7328 operates on the  $V_{CC}$  supply which should be 5 V nominal (4.75 V to 5.5 V) for specified performance. For  $V_{CC}$  between 2.7 V and 4.75 V, the AD7328 will meet its typical specifications. The AD7328 has a separate  $V_{DRIVE}$  pin which sets the I/O logic interface voltage (2.7 V to 5.5 V). The  $V_{DRIVE}$  voltage should not exceed  $V_{CC}$  by more than 0.3 V.

The AD7328 has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

## SUMMARY

The SAR ADC architecture is elegant, efficient, easy to understand, and ideally suited to modern fine-line CMOS processes. The lack of "pipeline" delay (or latency) makes it ideal for single-shot and multiplexed data acquisition applications. CMOS processes allows the addition of a variety of digital functions, such as automatic channel sequencing, auto-calibration, etc. In addition, many SAR ADCs have on-chip temperature sensors and voltage references. Although the SAR ADC had its origins in mathematical puzzles of the 1500s, it is still the converter of choice for modern multichannel data acquisition systems.

## REFERENCES

1. W. W. Rouse Ball and H. S. M. Coxeter, *Mathematical Recreations and Essays*, Thirteenth Edition, Dover Publications, 1987, pp. 50, 51. (*describes a mathematical puzzle for measuring unknown weights using the minimum number of weighing operations. The solution proposed in the 1500's is the same basic successive approximation algorithm used today*).
2. John C. Schelleng, "Code Modulation Communication System," *U.S. Patent 2,453,461*, filed June 19, 1946, issued November 9, 1948. (*an interesting description of a rather cumbersome successive approximation ADC based on vacuum tube technology. This converter was not very practical, but did illustrate the concept. Also in the patent is a description of a corresponding binary DAC*).
3. W. M. Goodall, "Telephony by Pulse Code Modulation," *Bell System Technical Journal*, Vol. 26, pp. 395-409, July 1947. (*describes an experimental PCM system using a 5-bit, 8KSPS successive approximation ADC based on the subtraction of binary weighted charges from a capacitor to implement the internal subtraction/DAC function. It required 5 internal reference voltages*).
4. Harold R. Kaiser, et al, "High-Speed Electronic Analogue-to-Digital Converter System," *U.S. Patent 2,784,396*, filed April 2, 1953, issued March 5, 1957. (*one of the first SAR ADCs to use an actual binary-weighted DAC internally*).
5. B. D. Smith, "Coding by Feedback Methods," *Proceedings of the I. R. E.*, Vol. 41, August 1953, pp. 1053-1058. (*Smith uses an internal DAC and also points out that a non-linear transfer function can be achieved by using a DAC with non-uniform bit weights, a technique which is widely used in today's voiceband ADCs with built-in companding*).
6. L.A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," *Bell System Technical Journal*, Vol. 27, No. 1, January 1948, pp. 1-43. (*describes non-linear diode-based compressors and expanders for generating a non-linear ADC/DAC transfer function*).

7. Bernard M. Gordon and Robert P. Talambiras, "Signal Conversion Apparatus," *U.S. Patent 3,108,266*, filed July 22, 1955, issued October 22, 1963. (*classic patent describing Gordon's 11-bit, 20kSPS vacuum tube successive approximation ADC done at Epsco. The internal DAC represents the first known use of equal currents switched into an R/2R ladder network.*)
8. Bernard M. Gordon and Evan T. Colton, "Signal Conversion Apparatus," *U.S. Patent 2,997,704*, filed February 24, 1958, issued August 22, 1961. (*classic patent describes the logic to perform the successive approximation algorithm in a SAR ADC.*)
9. Walt Kester, [\*Analog-Digital Conversion\*](#), Analog Devices, 2004, ISBN 0-916550-27-3, Chapter 1 and 3. Also available as [\*The Data Conversion Handbook\*](#), Elsevier/Newnes, 2005, ISBN 0-7506-7841-0, Chapter 1 and 3.

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## ADC Architectures III: Sigma-Delta ADC Basics

by Walt Kester

### INTRODUCTION

The sigma-delta ( $\Sigma$ - $\Delta$ ) ADC is the converter of choice for modern voiceband, audio, and high-resolution precision industrial measurement applications. The highly digital architecture is ideally suited for modern fine-line CMOS processes, thereby allowing easy addition of digital functionality without significantly increasing the cost. Because of its widespread use, it is important to understand the fundamental principles behind this converter architecture.

Due to the length of the topic, the discussion of  $\Sigma$ - $\Delta$  ADCs requires two tutorials, MT-022 and [MT-023](#). This first tutorial (MT-022) first discusses the history of  $\Sigma$ - $\Delta$  and the fundamental concepts of oversampling, quantization noise shaping, digital filtering, and decimation. Tutorial [MT-023](#) discusses more advanced topics related to  $\Sigma$ - $\Delta$ , including idle tones, multi-bit  $\Sigma$ - $\Delta$  ADCs, multistage noise shaping  $\Sigma$ - $\Delta$  ADCs (MASH), bandpass  $\Sigma$ - $\Delta$  ADCs, as well as some example applications.

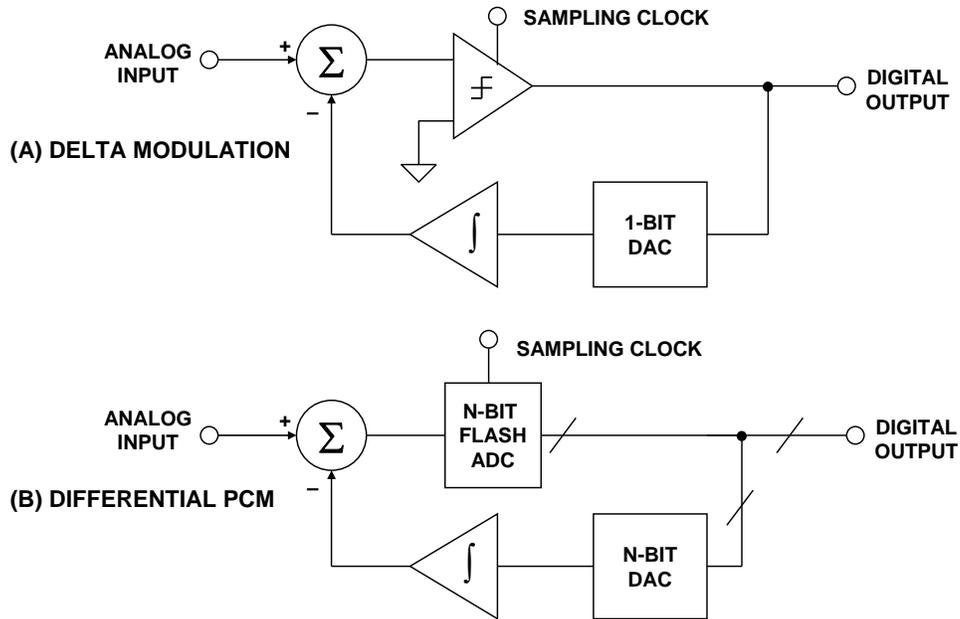
### HISTORICAL PERSPECTIVE

The  $\Sigma$ - $\Delta$  ADC architecture had its origins in the early development phases of pulse code modulation (PCM) systems—specifically, those related to transmission techniques called *delta modulation* and *differential PCM*. (An excellent discussion of both the history and concepts of the  $\Sigma$ - $\Delta$  ADC can be found by Max Hauser in Reference 1). Delta modulation was first invented at the ITT Laboratories in France by E. M. Deloraine, S. Van Mierlo, and B. Derjavitch in 1946 (References 2, 3).

The principle was "rediscovered" several years later at the Phillips Laboratories in Holland, whose engineers published the first extensive studies both of the single-bit and multi-bit concepts in 1952 and 1953 (References 4, 5). In 1950, C. C. Cutler of Bell Telephone Labs in the U.S. filed an important patent on differential PCM which covered the same essential concepts (Reference 6).

The driving force behind delta modulation and differential PCM was to achieve higher transmission efficiency by transmitting the *changes* (delta) in value between consecutive samples rather than the actual samples themselves.

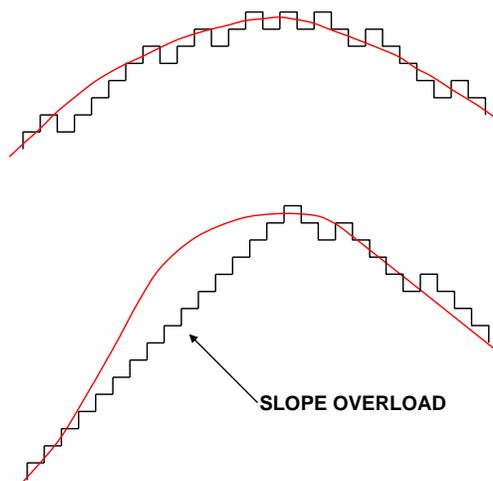
In *delta modulation*, the analog signal is quantized by a one-bit ADC (a comparator) as shown in Figure 1A. The comparator output is converted back to an analog signal with a 1-bit DAC, and subtracted from the input after passing through an integrator. The shape of the analog signal is transmitted as follows: a "1" indicates that a positive excursion has occurred since the last sample, and a "0" indicates that a negative excursion has occurred since the last sample.



**Figure 1: Delta Modulation and Differential PCM**

If the analog signal remains at a fixed dc level for a period of time, an alternating pattern of "0s" and "1s" is obtained. It should be noted that *differential PCM* (see Figure 1B) uses exactly the same concept except a multibit ADC is used rather than a single comparator to derive the transmitted information.

Since there is no limit to the number of pulses of the same sign that may occur, delta modulation systems are capable of tracking signals of any amplitude. In theory, there is no peak clipping. However, the theoretical limitation of delta modulation is that the analog signal must not change too rapidly. The problem of slope clipping is shown in Figure 2. Here, although each sampling instant indicates a positive excursion, the analog signal is rising too quickly, and the quantizer is unable to keep pace.



**Figure 2: Quantization Using Delta Modulation**

Slope clipping can be reduced by increasing the quantum step size or increasing the sampling rate. Differential PCM uses a multibit quantizer to effectively increase the quantum step sizes at the increase of complexity. Tests have shown that in order to obtain the same quality as classical PCM, delta modulation requires very high sampling rates, typically 20× the highest frequency of interest, as opposed to Nyquist rate of 2×.

For these reasons, delta modulation and differential PCM have never achieved any significant degree of popularity, however a slight modification of the delta modulator leads to the basic  $\Sigma$ - $\Delta$  architecture, one of the most popular ADC architectures in use today.

In 1954 C. C. Cutler of Bell Labs filed a very significant patent which introduced the principle of *oversampling* and *noise shaping* with the specific intent of achieving higher resolution (Reference 7). His objective was not specifically to design a Nyquist ADC, but to transmit the oversampled noise-shaped signal without reducing the data rate. Thus Cutler's converter embodied all the concepts in a  $\Sigma$ - $\Delta$  ADC with the exception of *digital filtering* and *decimation* which would have been too complex and costly at the time using vacuum tube technology.

Occasional work continued on these concepts over the next several years, including an important patent of C. B. Brahm filed in 1961 which gave details of the analog design of the loop filter for a second-order multibit noise shaping ADC (Reference 8). Transistor circuits began to replace vacuum tubes over the period, and this opened up many more possibilities for implementation of the architecture.

In 1962, Inose, Yasuda, and Murakami elaborated on the single-bit oversampling noise-shaping architecture proposed by Cutler in 1954 (Reference 9). Their experimental circuits used solid state devices to implement first and second-order  $\Sigma$ - $\Delta$  modulators. The 1962 paper was followed by a second paper in 1963 which gave excellent theoretical discussions on oversampling and noise-shaping (Reference 10). These two papers were also the first to use the name *delta-sigma* to describe the architecture. The name *delta-sigma* stuck until the 1970s when AT&T engineers began using name *sigma-delta*. Since that time, both names have been used; however, sigma-delta may be the more correct of the two.

It is interesting to note that all the work described thus far was related to transmitting an oversampled digitized signal directly rather than the implementation of a Nyquist ADC. In 1969 D. J. Goodman at Bell Labs published a paper describing a true Nyquist  $\Sigma$ - $\Delta$  ADC with a digital filter and a decimator following the modulator (Reference 11). This was the first use of the  $\Sigma$ - $\Delta$  architecture for the explicit purpose of producing a Nyquist ADC. In 1974 J. C. Candy, also of Bell Labs, described a multibit oversampling  $\Sigma$ - $\Delta$  ADC with noise shaping, digital filtering, and decimation to achieve a high resolution Nyquist ADC (Reference 12).

The IC  $\Sigma$ - $\Delta$  ADC offers several advantages over the other architectures, especially for high resolution, low frequency applications. First and foremost, the single-bit  $\Sigma$ - $\Delta$  ADC is inherently monotonic and requires no laser trimming. The  $\Sigma$ - $\Delta$  ADC also lends itself to low cost foundry CMOS processes because of the digitally intensive nature of the architecture. Examples of early monolithic  $\Sigma$ - $\Delta$  ADCs are given in References 13-21. Since that time there have been a constant

stream of process and design improvements in the fundamental architecture proposed in the early works cited above.

Modern CMOS  $\Sigma$ - $\Delta$  ADCs (and DACs, for that matter) are the converters of choice for voiceband and audio applications. The highly digital architectures lend themselves nicely to fine-line CMOS. In addition, high resolution (up to 24 bits) low frequency  $\Sigma$ - $\Delta$  ADCs have virtually replaced the older integrating converters in precision industrial measurement applications.

## BASICS OF $\Sigma$ - $\Delta$ ADCS

There have been innumerable descriptions of the architecture and theory of  $\Sigma$ - $\Delta$  ADCs, but most commence with a maze of integrals and deteriorate from there. Some engineers who do not understand the theory of operation of  $\Sigma$ - $\Delta$  ADCs are convinced, from study of a typical published article, that it is too complex to comprehend easily.

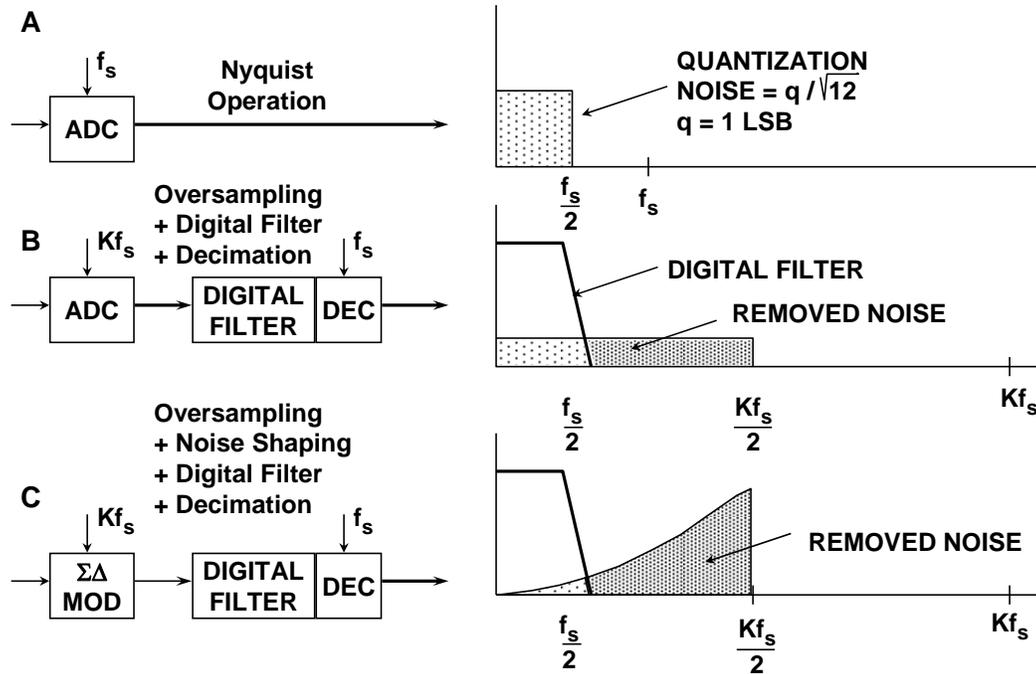
There is nothing particularly difficult to understand about  $\Sigma$ - $\Delta$  ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A  $\Sigma$ - $\Delta$  ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This digital circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know precisely how the filter works to appreciate what it does. To understand how a  $\Sigma$ - $\Delta$  ADC works, familiarity with the concepts of *oversampling*, *quantization noise shaping*, *digital filtering*, and *decimation* is required.

Let us consider the technique of oversampling with an analysis in the frequency domain. Where a dc conversion has a *quantization error* of up to  $\frac{1}{2}$  LSB, a sampled data system has *quantization noise*. A perfect classical N-bit sampling ADC has an rms quantization noise of  $q/\sqrt{12}$  uniformly distributed within the Nyquist band of dc to  $f_s/2$  (where  $q$  is the value of an LSB and  $f_s$  is the sampling rate) as shown in Figure 3A. Therefore, its SNR with a full-scale sinewave input will be  $(6.02N + 1.76)$  dB. (Refer to [Tutorial MT-001](#) for the derivation). If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantization noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}. \quad \text{Eq. 1}$$

If we choose a much higher sampling rate,  $Kf_s$  (see Figure 3B), the rms quantization noise remains  $q/\sqrt{12}$ , but the noise is now distributed over a wider bandwidth dc to  $Kf_s/2$ . If we then apply a digital low pass filter (LPF) to the output, we remove much of the quantization noise, but do not affect the wanted signal—so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC. The factor  $K$  is generally referred to as the *oversampling ratio*. It should be noted at this point that oversampling has an added benefit in that it relaxes the requirements on the analog antialiasing filter. This is a big advantage of  $\Sigma$ - $\Delta$ ,

especially in consumer audio applications where the cost of a sharp cutoff linear phase filter can be significant.

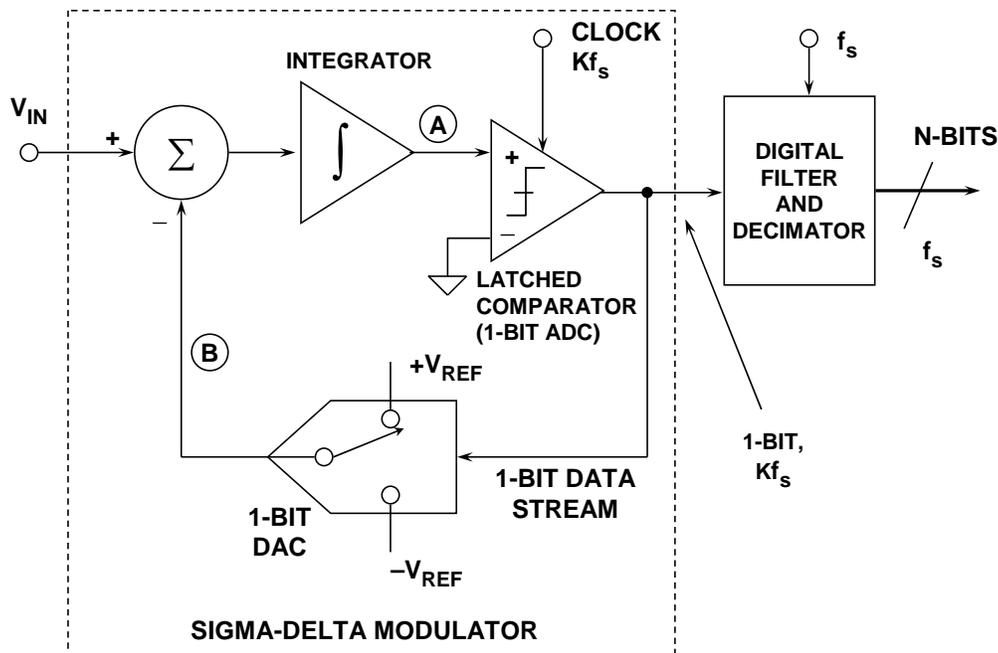


**Figure 3: Oversampling, Digital Filtering, Noise Shaping, and Decimation**

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate ( $Kf_s$ ) and still satisfy the Nyquist criterion. This may be achieved by passing every  $M$ th result to the output and discarding the remainder. The process is known as "decimation" by a factor of  $M$ . Despite the origins of the term (*decem* is Latin for ten),  $M$  can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 3B).

If we simply use oversampling to improve resolution, we must oversample by a factor of  $2^{2N}$  to obtain an  $N$ -bit increase in resolution. The  $\Sigma$ - $\Delta$  converter does not need such a high oversampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that most of it falls outside this passband as shown in Figure 3C.

If we take a 1-bit ADC (a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from the ADC output, we have a first-order  $\Sigma$ - $\Delta$  modulator as shown in Figure 4. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a  $\Sigma$ - $\Delta$  ADC—the  $\Sigma$ - $\Delta$  modulator shapes the quantization noise so that it lies above the passband of the digital output filter, and the ENOB is therefore much larger than would otherwise be expected from the oversampling ratio.

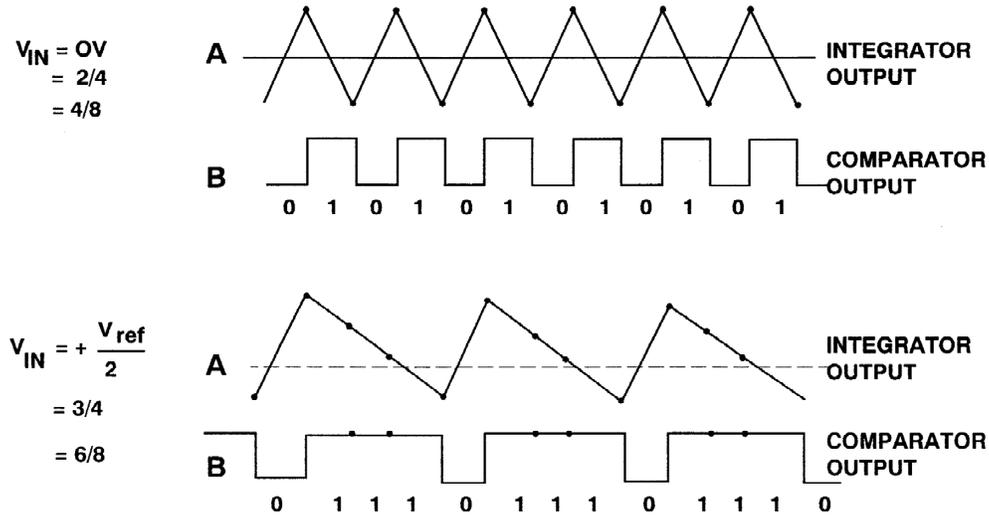


**Figure 4: First-Order Sigma-Delta ADC**

Intuitively, a  $\Sigma$ - $\Delta$  ADC operates as follows. Assume a dc input at  $V_{IN}$ . The integrator is constantly ramping up or down at node A. The output of the comparator is fed back through a 1-bit DAC to the summing input at node B. The negative feedback loop from the comparator output through the 1-bit DAC back to the summing point will force the average dc voltage at node B to be equal to  $V_{IN}$ . This implies that the average DAC output voltage must equal the input voltage  $V_{IN}$ . The average DAC output voltage is controlled by the *ones-density* in the 1-bit data stream from the comparator output. As the input signal increases towards  $+V_{REF}$ , the number of "ones" in the serial bit stream increases, and the number of "zeros" decreases. Similarly, as the signal goes negative towards  $-V_{REF}$ , the number of "ones" in the serial bit stream decreases, and the number of "zeros" increases. From a very simplistic standpoint, this analysis shows that the average value of the input voltage is contained in the serial bit stream out of the comparator. The digital filter and decimator process the serial bit stream and produce the final output data.

For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged, will a meaningful value result. The  $\Sigma$ - $\Delta$  modulator is very difficult to analyze in the time domain because of this apparent randomness of the single-bit data output. If the input signal is near positive full-scale, it is clear that there will be more "1"s than "0"s in the bit stream. Likewise, for signals near negative full-scale, there will be more "0"s than "1"s in the bit stream. For signals near midscale, there will be approximately an equal number of "1"s and "0"s. Figure 5 shows the output of the integrator for two input conditions. The first is for an input of zero (midscale). To decode the output, pass the output samples through a simple digital lowpass filter that averages every four samples. The output of the filter is  $2/4$ . This value represents bipolar zero. If more samples are averaged, more dynamic range is achieved. For example, averaging 4 samples gives 2 bits of resolution,

while averaging 8 samples yields  $4/8$ , or 3 bits of resolution. In the bottom waveform of Figure 5, the average obtained for 4 samples is  $3/4$ , and the average for 8 samples is  $6/8$ .



**Figure 5: Sigma-Delta Modulator Waveforms**

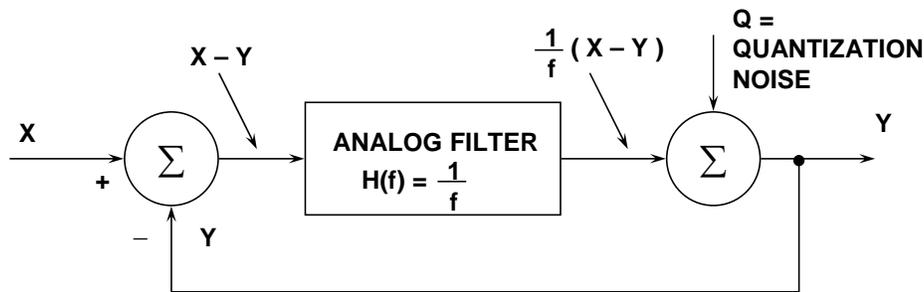
For an interactive tutorial on the time domain characteristics of the  $\Sigma$ - $\Delta$  modulator, refer to the [Sigma-Delta Tutorial](#) located in the Analog Devices' [Design Center](#) which gives a graphical illustration of the behavior of an idealized  $\Sigma$ - $\Delta$  ADC.

The  $\Sigma$ - $\Delta$  ADC can also be viewed as a synchronous voltage-to-frequency converter followed by a counter. If the number of "1"s in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. Obviously, this method of averaging will only work for dc or very slowly changing input signals. In addition,  $2^N$  clock cycles must be counted in order to achieve N-bit effective resolution, thereby severely limiting the effective sampling rate.

It should be noted that because the digital filter is an integral part of the  $\Sigma$ - $\Delta$  ADC, there is a built-in "pipeline" delay (sometimes called "latency") primarily determined by the number of taps in the digital filter. Digital filters in  $\Sigma$ - $\Delta$  ADCs can be quite large (several hundred taps), so the latency may become an issue in multiplexed applications where the appropriate amount of settling time must be allowed after switching channels.

**FREQUENCY DOMAIN ANALYSIS OF A SIGMA-DELTA ADC AND NOISE SHAPING**

Further time-domain analysis is not productive, and the concept of noise shaping is best explained in the frequency domain by considering the simple  $\Sigma$ - $\Delta$  modulator model in Figure 6.



$$Y = \frac{1}{f} (X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f + 1} + \frac{Q f}{f + 1}$$

SIGNAL TERM

NOISE TERM

**Figure 6: Simplified Frequency Domain Linearized Model of a Sigma-Delta Modulator**

The integrator in the modulator is represented as an analog lowpass filter with a transfer function equal to  $H(f) = 1/f$ . This transfer function has an amplitude response which is inversely proportional to the input frequency. The 1-bit quantizer generates quantization noise,  $Q$ , which is injected into the output summing block. If we let the input signal be  $X$ , and the output  $Y$ , the signal coming out of the input summer must be  $X - Y$ . This is multiplied by the filter transfer function,  $1/f$ , and the result goes to one input of the output summer. By inspection, we can then write the expression for the output voltage  $Y$  as:

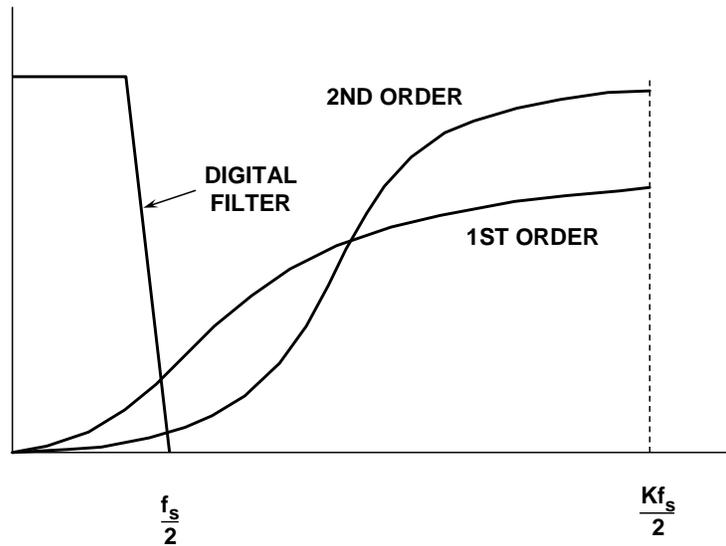
$$Y = \frac{1}{f} (X - Y) + Q. \tag{Eq. 2}$$

This expression can easily be rearranged and solved for  $Y$  in terms of  $X$ ,  $f$ , and  $Q$ :

$$Y = \frac{X}{f + 1} + \frac{Q \cdot f}{f + 1}. \tag{Eq. 3}$$

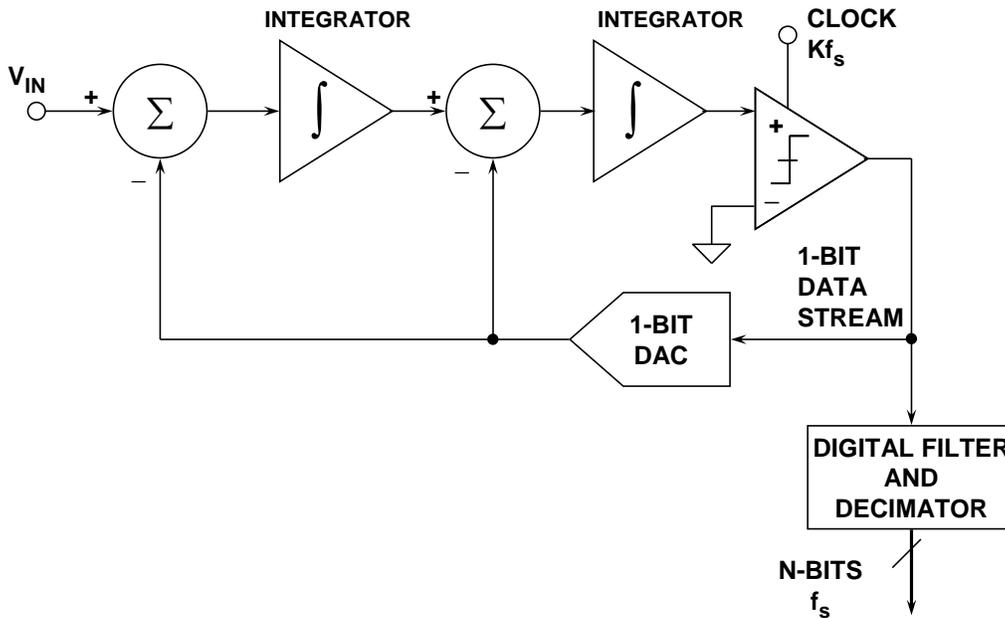
Note that as the frequency  $f$  approaches zero, the output voltage  $Y$  approaches  $X$  with no noise component. At higher frequencies, the amplitude of the signal component approaches zero, and the noise component approaches  $Q$ . At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a lowpass effect on the signal, and a highpass effect on the quantization noise. Thus the analog filter performs the noise shaping function in the  $\Sigma$ - $\Delta$  modulator model. For a given input frequency, higher order analog filters offer more attenuation. The same is true of  $\Sigma$ - $\Delta$  modulators, provided certain precautions are taken.

By using more than one integration and summing stage in the  $\Sigma$ - $\Delta$  modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given oversampling ratio as is shown in Figure 7 for both a first and second-order  $\Sigma$ - $\Delta$  modulator.



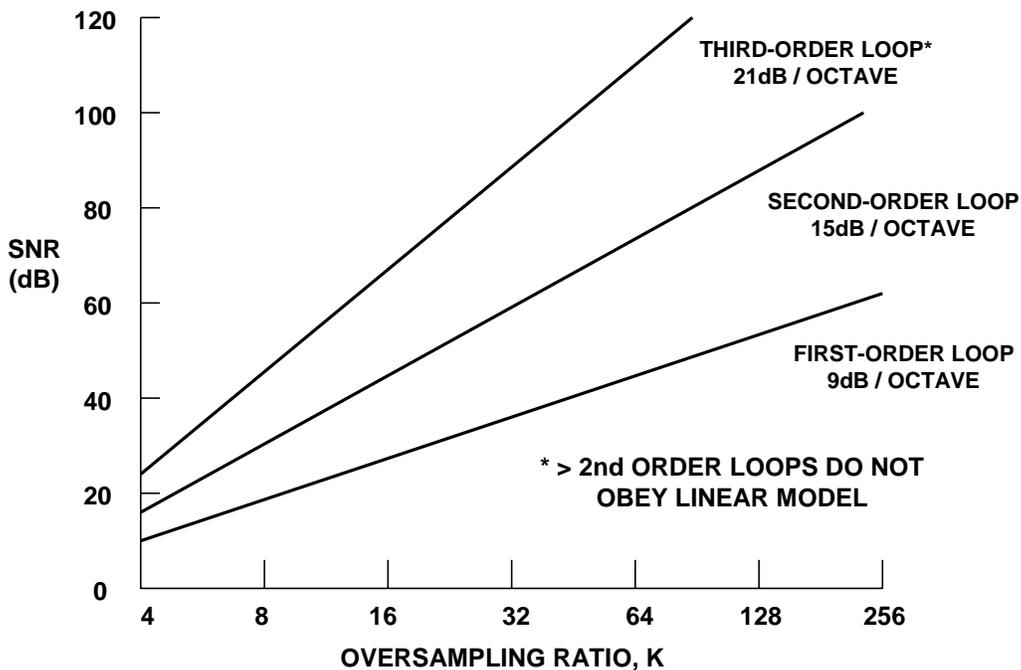
**Figure 7: Sigma-Delta Modulators Shape Quantization Noise**

The block diagram for the second-order  $\Sigma$ - $\Delta$  modulator is shown in Figure 8. Third, and higher, order  $\Sigma$ - $\Delta$  ADCs were once thought to be potentially unstable at some values of input—recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, the DSP in the digital filter and decimator can be made to recognize incipient instability and react to prevent it.



**Figure 8: Second-Order Sigma-Delta ADC**

Figure 9 shows the relationship between the order of the  $\Sigma$ - $\Delta$  modulator and the amount of oversampling necessary to achieve a particular SNR. For instance, if the oversampling ratio is 64, an ideal second-order system is capable of providing an SNR of about 80 dB. This implies approximately 13 effective number of bits (ENOB). Although the filtering done by the digital filter and decimator can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in the quantization noise unless post-filtering techniques were employed. Additional resolution can be obtained from the 1-bit system by increasing the oversampling ratio and/or by using a higher-order modulator. Other methods are often used to achieve higher resolution, such as the multi-bit  $\Sigma$ - $\Delta$  architecture, and are discussed in Tutorial [MT-023](#).



**Figure 9: SNR Versus Oversampling Ratio for First, Second, and Third-Order Loops**

**SUMMARY**

This tutorial has covered the basics of  $\Sigma$ - $\Delta$  ADCs from a historical perspective including the important concepts of oversampling, digital Filtering, noise shaping, and decimation. Tutorial [MT-023](#) covers some of the more advanced concepts and applications of  $\Sigma$ - $\Delta$  ADCs, such as idle tones, multi-bit  $\Sigma$ - $\Delta$ , MASH, and bandpass  $\Sigma$ - $\Delta$ .

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## ADC Architectures IV: Sigma-Delta ADC Advanced Concepts and Applications

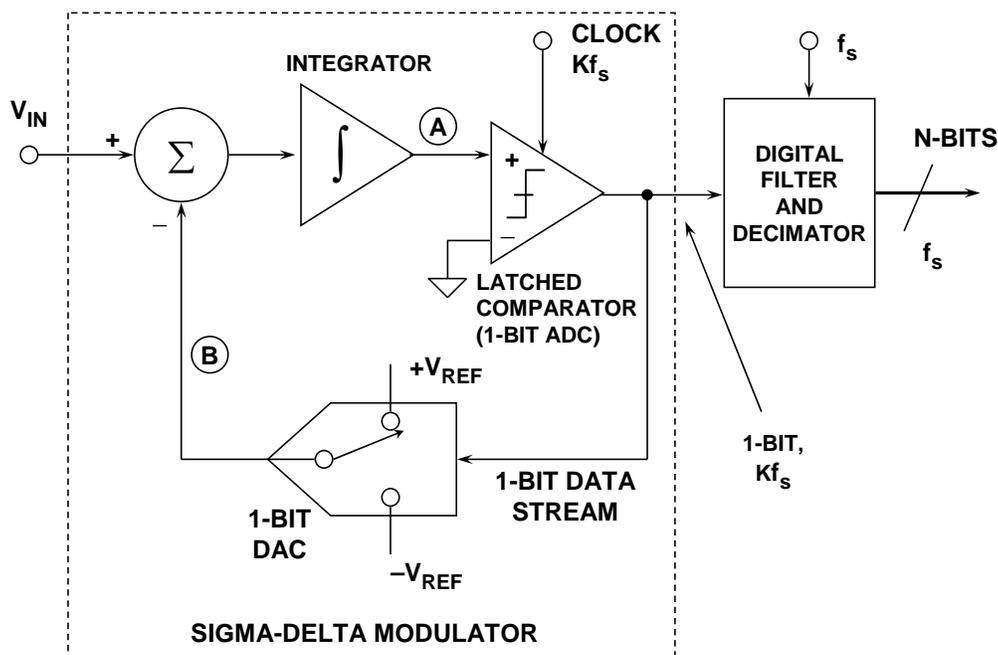
by Walt Kester

### INTRODUCTION

[Tutorial MT-022](#) discussed the basics of  $\Sigma$ - $\Delta$  ADCs. In this tutorial, we will look at some of the more advanced concepts including idle tones, multi-bit  $\Sigma$ - $\Delta$ , MASH, bandpass  $\Sigma$ - $\Delta$ , as well as some example applications.

### IDLE TONE CONSIDERATIONS

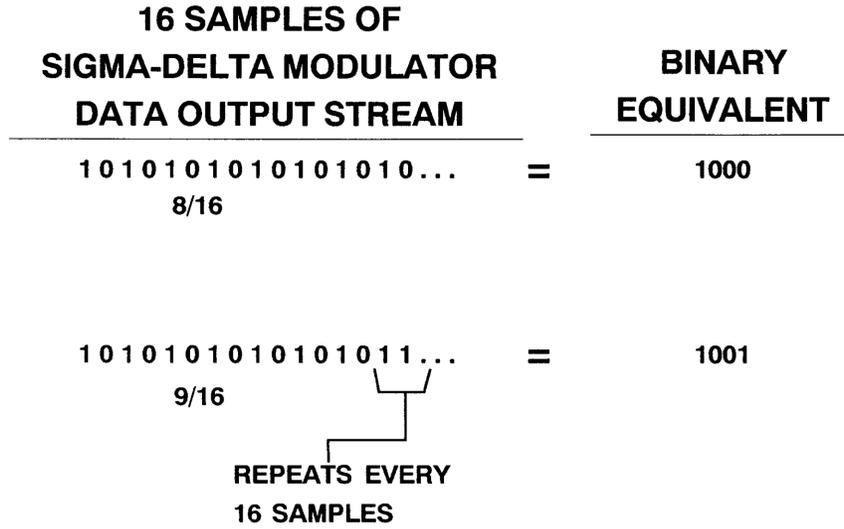
In our discussion of  $\Sigma$ - $\Delta$  ADCs up to this point, we have made the assumption that the quantization noise produced by the  $\Sigma$ - $\Delta$  modulator (see Figure 1) is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the first-order modulator. Consider the case where we are averaging 16 samples of the modulator output in a 4-bit  $\Sigma$ - $\Delta$  ADC.



**Figure 1: First-Order Sigma-Delta ADC**

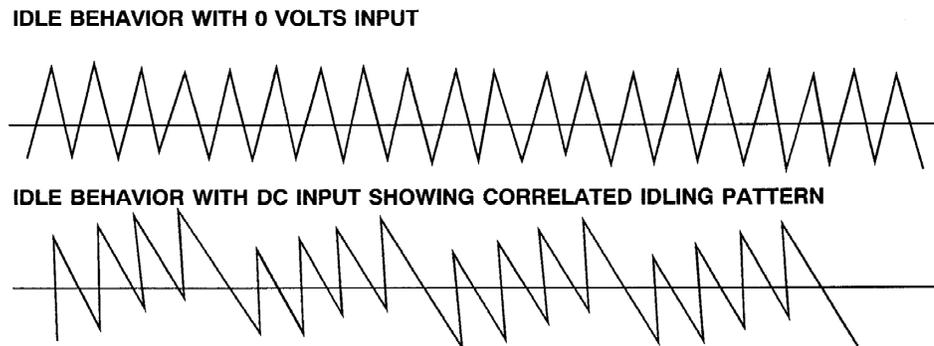
Figure 2 shows the bit pattern for two input signal conditions: an input signal having the value  $8/16$ , and an input signal having the value  $9/16$ . In the case of the  $9/16$  signal, the modulator output bit pattern has an extra "1" every 16th output. This will produce energy at  $Kf_s/16$ , which translates into an unwanted tone. If the oversampling ratio ( $K$ ) is less than 8, this tone will fall

into the passband. In audio, the idle tones can be heard just above the noise floor as the input changes from negative to positive fullscale.

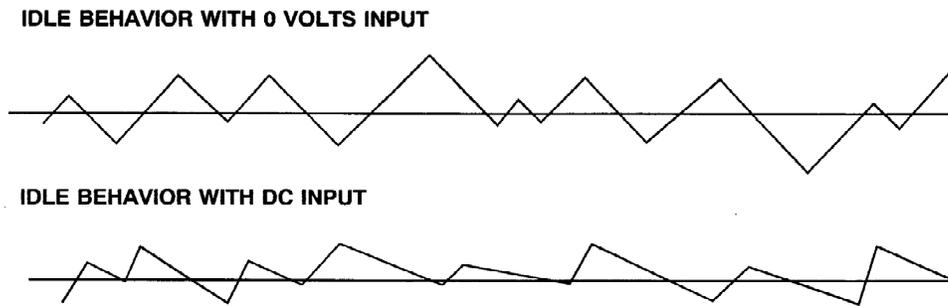


**Figure 2: Repetitive Bit Pattern in Sigma-Delta Modulator Output**

Figure 3 shows the correlated idling pattern behavior for a first order  $\Sigma$ - $\Delta$  modulator, and Figure 4 shows the relatively uncorrelated pattern for a second-order modulator. For this reason, virtually all  $\Sigma$ - $\Delta$  ADCs contain at least a second-order modulator loop, and some use up to fifth-order loops.



**Figure 3: Idling Patterns for First-Order Sigma-Delta Modulator (Integrator Output)**



**Figure 4: Idling Patterns for Second-Order Sigma-Delta Modulator (Integrator Output)**

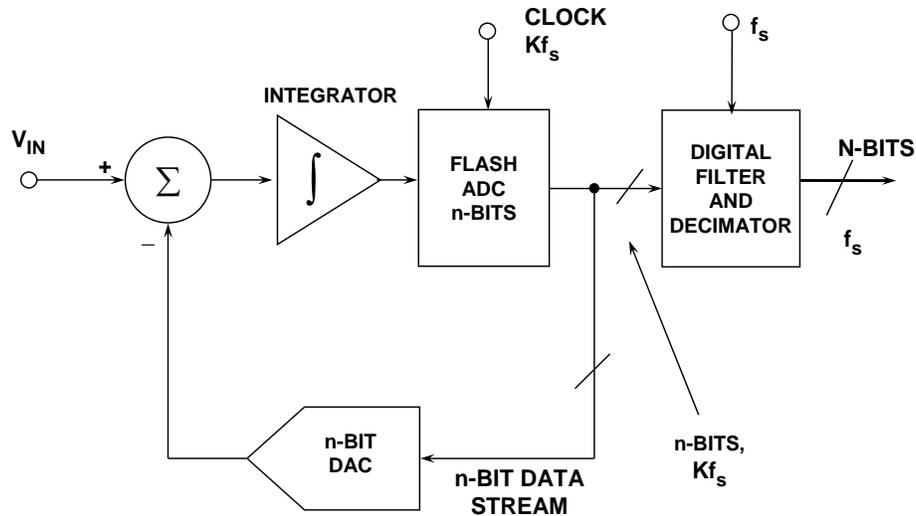
## HIGHER ORDER LOOP CONSIDERATIONS

In order to achieve wide dynamic range,  $\Sigma$ - $\Delta$  modulator loops greater than second-order are necessary, but present real design challenges. First of all, the simple linear models previously discussed are no longer fully accurate. Loops of order greater than two are generally not guaranteed to be stable under all input conditions. The instability arises because the comparator is a nonlinear element whose effective "gain" varies inversely with the input level. This mechanism for instability causes the following behavior: if the loop is operating normally, and a large signal is applied to the input that overloads the loop, the average gain of the comparator is reduced. The reduction in comparator gain in the linear model causes loop instability. This causes instability even when the signal that caused it is removed.

In actual practice, such a circuit would normally oscillate on power-up due to initial conditions caused by turn-on transients. The [AD1879](#) dual audio ADC released in 1994 by Analog Devices used a 5<sup>th</sup> order loop. Extensive nonlinear stabilization techniques were required in this and similar higher-order loop designs (References 1-5).

## MULTI-BIT SIGMA-DELTA CONVERTERS

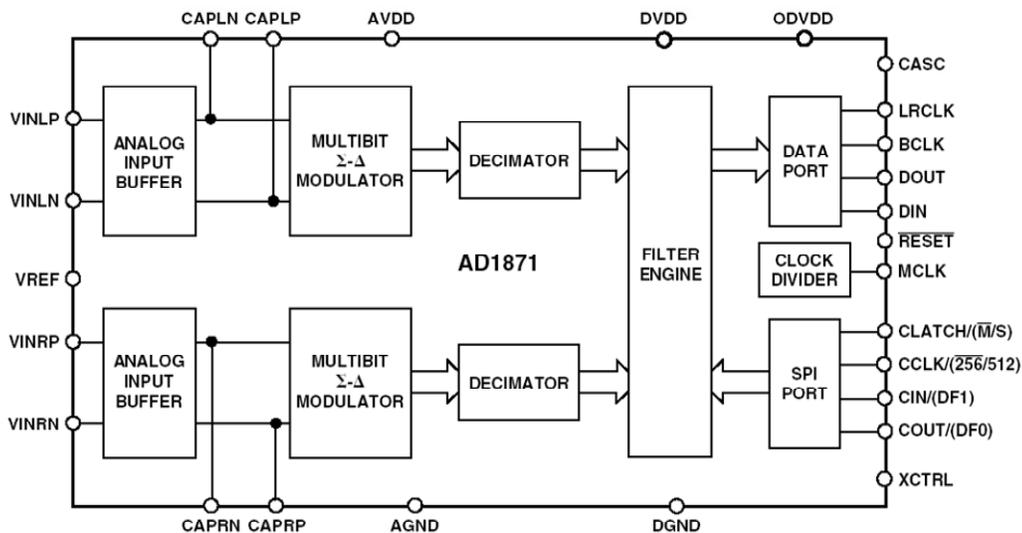
So far we have considered only  $\Sigma$ - $\Delta$  converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 5 shows a multi-bit  $\Sigma$ - $\Delta$  ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order loops can generally be used. Idling patterns tend to be more random thereby minimizing tonal effects.



**Figure 5: Multi-Bit Sigma-Delta ADC**

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is required to approach 16-bit performance levels. This makes the multi-bit architecture extremely impractical to implement on mixed-signal ICs using traditional binary DAC techniques.

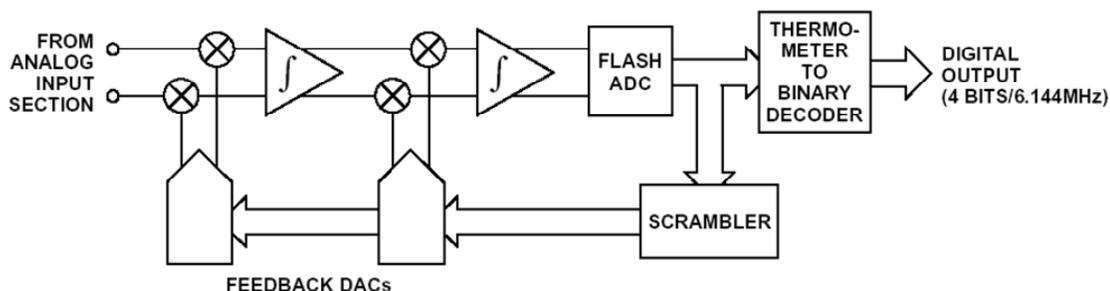
However, fully decoded thermometer DACs (see [Tutorial MT-014](#)) coupled with proprietary data scrambling techniques as used in a number of Analog Devices' audio ADCs and DACs, including the 24-bit stereo [AD1871](#) (see References 6 and 7) can achieve high SNR and low distortion using the multi-bit architecture. The multi-bit data scrambling technique both minimizes idle tones and ensures better differential linearity. A simplified block diagram of the AD1871 ADC is shown in Figure 6.



**Figure 6: [AD1871](#) 24-Bit 96-kSPS Stereo Audio Multi-Bit Sigma-Delta ADC**

The AD1871's analog  $\Sigma$ - $\Delta$  modulator section comprises a second order multi-bit implementation using Analog Device's proprietary technology for best performance. As shown in Figure 7, the two analog integrator blocks are followed by a flash ADC section that generates the multi-bit samples.

The output of the flash ADC, which is thermometer encoded, is decoded to binary for output to the filter sections and is scrambled for feedback to the two integrator stages. The modulator is optimized for operation at a sampling rate of 6.144 MHz (which is  $128 \times f_s$  at 48-kHz sampling and  $64 \times f_s$  at 96-kHz sampling). The A-weighted dynamic range of the AD1871 is typically 105 dB.

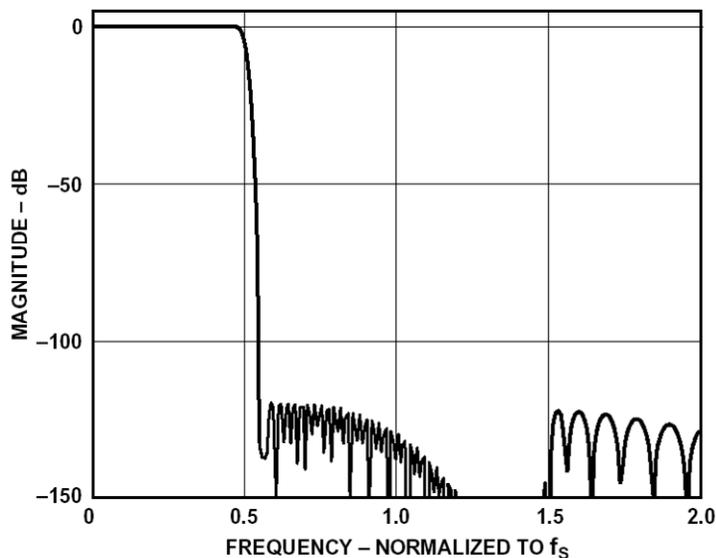


**Figure 7: Details of the AD1871 Second-Order Modulator and Data Scrambler**

## DIGITAL FILTER IMPLICATIONS ON MULTIPLEXED APPLICATIONS

The digital filter is an integral part of all  $\Sigma$ - $\Delta$  ADCs—there is no way to remove it. The settling time of this filter affects certain applications especially when using  $\Sigma$ - $\Delta$  ADCs in multiplexed applications. The output of a multiplexer can present a step function input to an ADC if there are different input voltages on adjacent channels. In fact, the multiplexer output can represent a full-scale step voltage to the  $\Sigma$ - $\Delta$  ADC when channels are switched. Adequate filter settling time must be allowed, therefore, in such applications. This does not mean that  $\Sigma$ - $\Delta$  ADCs shouldn't be used in multiplexed applications, just that the settling time of the digital filter must be considered. Some newer  $\Sigma$ - $\Delta$  ADCs such are actually optimized for use in multiplexed applications.

For example, the group delay through the AD1871 digital filter is 910  $\mu$ s (sampling at 48 kSPS) and 460  $\mu$ s (sampling at 96 kSPS)—this represents the time it takes for a step function input to propagate through one-half the number of taps in the digital filter. The total settling time is therefore approximately twice the group delay time. The input oversampling frequency is 6.144 MSPS for both conditions. The frequency response of the digital filter in the AD1871 ADC is shown in Figure 8. This filter uses a finite impulse response (FIR) design, and therefore has linear phase over the audio passband. Duplicating this performance using an analog filter would require considerable design effort as well as rather costly components.



**Figure 8: [AD1871](#) 24-Bit, 96-kSPS Stereo Sigma-Delta ADC Digital Filter Characteristics**

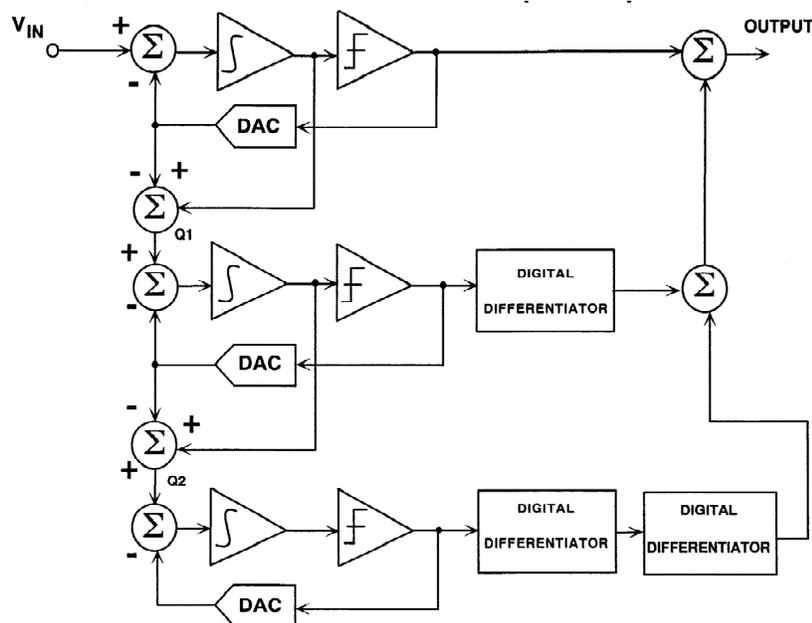
In other applications, such as low frequency, high resolution 24-bit measurement  $\Sigma$ - $\Delta$  ADCs (such as the AD77xx-series), other types of digital filters may be used. For instance, the SINC<sup>3</sup> response is popular because it has zeros at multiples of the throughput rate. A 10-Hz throughput rate produces zeros at 50 Hz and 60 Hz which aids in ac power line rejection.

Regardless of the type of digital filter,  $\Sigma$ - $\Delta$  ADCs require that sufficient settling time is allowed after the application of a step function input.

### MULTISTAGE NOISE SHAPING (MASH) SIGMA-DELTA CONVERTERS

As has been discussed, nonlinear stabilization techniques can be difficult for 3<sup>rd</sup> order loops or higher. In many cases, the multi-bit architecture is preferable. An alternative approach to either of these, called multistage noise shaping (MASH), utilizes cascaded stable first-order loops (see References 8 and 9). Figure 9 shows a block diagram of a three-stage MASH ADC. The output of the first integrator is subtracted from the first DAC output to yield the first stage quantization noise, Q1. Q1 is then quantized by the second stage. The output of the second integrator is subtracted from the second DAC output to yield the second stage quantization noise which is in turn quantized by the third stage.

The output of the first stage is summed with a single digital differentiation of the second stage output and a double differentiation of the third stage output to yield the final output. The result is that the quantization noise Q1 is suppressed by the second stage, and the quantization noise Q2 is suppressed by the third stage yielding the same suppression as a third-order loop. Since this result is obtained using three first-order loops, stable operation is assured.

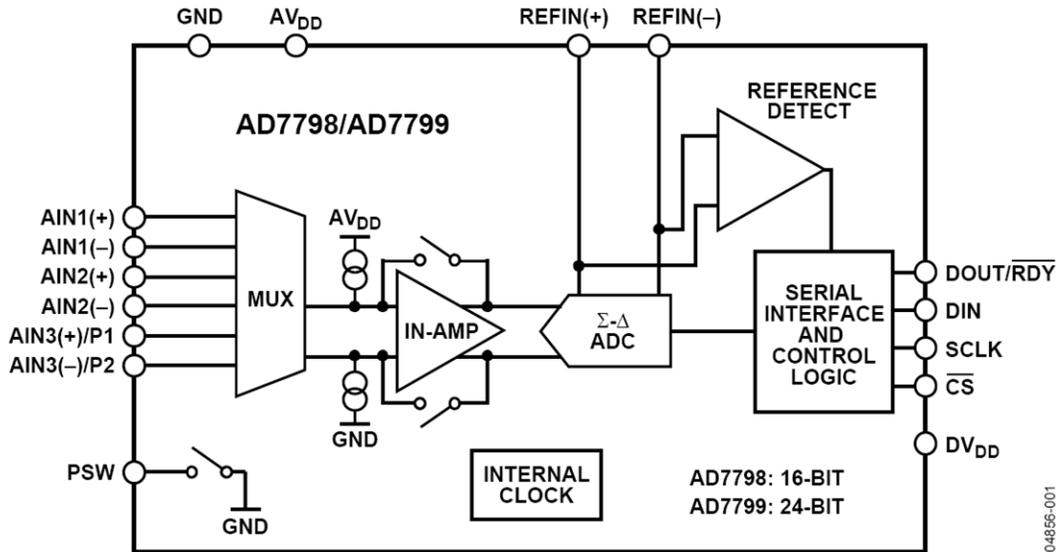


**Figure 9: Multi-Stage Noise Shaping Sigma-Delta ADC (MASH)**

## HIGH RESOLUTION MEASUREMENT SIGMA-DELTA ADCS

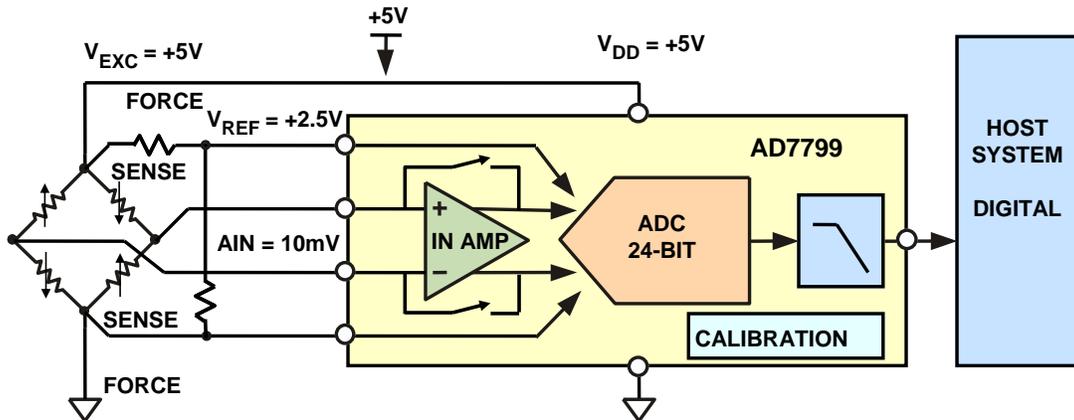
While older integrating architectures such as dual-slope are still used in digital voltmeters, CMOS  $\Sigma$ - $\Delta$  ADCs are the dominant converter for today's industrial measurement applications. These converters offer excellent 50-Hz/60-Hz power line common-mode rejection and resolutions up to 24 bits with various digital features, such as on-chip calibration. Many have programmable gain amplifiers (PGAs) which allow the direct digitization of small signals from bridge and thermocouple transducers without the need for additional external signal conditioning circuits.

In order to better understand the capability of  $\Sigma$ - $\Delta$  measurement ADCs and the power of the technique, a modern example, the 24-bit [AD7799](#), will be examined in detail. The AD7799 is a member of the AD77xx family and is shown in Figure 10. This ADC was specifically designed to interface directly to low-level sensor outputs such as bridges in weigh scale applications. The device accepts low-level signals directly from a bridge and outputs a serial digital word. There are three multiplexed and buffered differential inputs which drive an internal instrumentation amplifier. The in-amp can be programmed for eight different gains: 1, 2, 4, 8, 16, 32, 64, and 128.



**Figure 10: [AD7799](#) Sigma-Delta Single-Supply Bridge ADC**

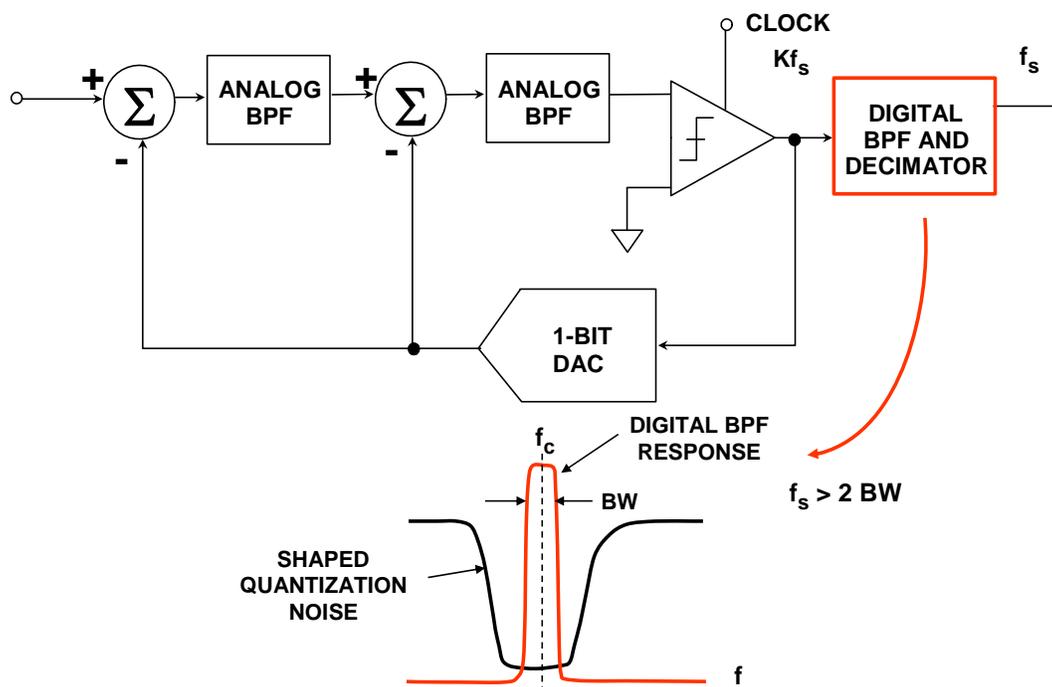
Figure 11 shows a direct connection between a bridge-based load cell and a high resolution  $\Sigma$ - $\Delta$  ADC, the AD7799. The fullscale bridge output of 10 mV is digitized to approximately 16 noise-free bits by the ADC at a throughput rate of 4.17 Hz. Ratiometric operation eliminates the need for a precision voltage reference. The AD7799 can be operated at throughput rates from 4.17 Hz to 500 Hz. The part operates with a power supply from 2.7 V to 5.25 V and consumes 380  $\mu$ A typical.



**Figure 11: Load Cell Conditioning Using a High Resolution Sigma-Delta ADC**

## BANDPASS SIGMA-DELTA CONVERTERS

The  $\Sigma$ - $\Delta$  ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from dc. Thus, their quantization noise is pushed up in frequency. At present, most commercially available  $\Sigma$ - $\Delta$  ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system dc offsets). But there is no particular reason why the filters of the  $\Sigma$ - $\Delta$  modulator should be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a  $\Sigma$ - $\Delta$  ADC with bandpass filters (BPFs) as shown in Figure 12, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see References 10, 11, and 12). If the digital filter is then programmed to have its pass-band in this region, we have a  $\Sigma$ - $\Delta$  ADC with a bandpass, rather than a lowpass characteristic. Such devices would appear to be useful in direct IF-to-digital conversion, digital radios, ultrasound, and other undersampling applications. However, the modulator and the digital BPF must be designed for the specific set of frequencies required by the system application, thereby somewhat limiting the flexibility of this approach.



**Figure 12: Replacing Integrators with Resonators Gives a Bandpass Sigma-Delta ADC**

In an undersampling application of a bandpass  $\Sigma$ - $\Delta$  ADC, the minimum sampling frequency must be at least twice the signal bandwidth,  $BW$ . The signal is centered around a carrier frequency,  $f_c$ . A typical digital radio application using a 455-kHz center frequency and a signal bandwidth of 10 kHz is described in Reference 11. An oversampling frequency  $Kf_s = 2$  MSPS and an output rate  $f_s = 20$  kSPS yielded a dynamic range of 70 dB within the signal bandwidth.

An early example of a bandpass  $\Sigma$ - $\Delta$  ADC is the [AD9870](#) IF Digitizing Subsystem having a nominal oversampling frequency of 18 MSPS, a center frequency of 2.25 MHz, and a bandwidth of 10 kHz to 150 kHz (see details in Reference 12).

The [AD9874](#) and [AD9864](#) are general purpose IF subsystems that digitize low level 10-300 MHz IF signals with bandwidths up to 270 kHz (see details in Reference 13). The signal chain contains a low noise amplifier, mixer, bandpass  $\Sigma$ - $\Delta$  ADC and a decimation filter with programmable decimation factor. An AGC circuit provides 12 dB of continuous gain adjustment.

## SUMMARY

Sigma-delta ADCs and DACs have proliferated into many modern applications including measurement, voiceband, audio, etc. The technique takes full advantage of low cost CMOS processes and therefore makes integration with highly digital functions such as DSPs practical. Modern techniques such as the multi-bit data scrambled architecture minimize problems with idle tones which plagued early  $\Sigma$ - $\Delta$  products. Resolutions up to 24-bits are currently available, and the requirements on analog antialiasing/anti-imaging filters are greatly relaxed due to oversampling. The internal digital filter in audio  $\Sigma$ - $\Delta$  ADCs can be designed for linear phase, which is a major requirement in those applications. For high resolution  $\Sigma$ - $\Delta$  ADCs designed for measurement applications, the digital filter is generally designed so that zeros occur at the mains frequencies of 50 Hz and 60 Hz.

Many  $\Sigma$ - $\Delta$  converters offer a high level of user programmability with respect to output data rate, digital filter characteristics, and self-calibration modes. Multi-channel  $\Sigma$ - $\Delta$  ADCs are now available for data acquisition systems, and most users are well-educated with respect to the settling time requirements of the internal digital filter in these applications.

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