2017 Paper E2.1: Digital Electronics II

Answer ALL questions.

There are THREE questions on the paper.

Question ONE counts for 40% of the marks, other questions 30% each

Time allowed: 2 hours

(Not to be removed from the Examination Room)

Information for Candidates:

The following notation is used in this paper:

1. Unless explicitly indicated otherwise, digital circuits are drawn with their inputs on the left and their outputs on the right.
2. Within a circuit, signals with the same name are connected together even if no connection is shown explicitly.
3. The notation X2:0 denotes the three-bit number X2, X1 and X0. The least significant bit of a binary number is always designated bit 0.
4. Signed binary numbers use 2's complement notation.

1. (a) *Figure 1.1* shows the circuit of a finite state machine (FSM) having a single input signal X and a state defined by the 2-bit binary number Y[1:0]. When X = 0, the state sequence is: 0, 1, 2, 3, 0, …. etc. and when X = 1, the state sequence is: 0, 2, 3, 1, 0, … etc. .

(i) Draw a state diagram for the circuit.

[3]

(ii) Complete the timing diagram shown in *Figure 1.2*.

[2]

(iii) Specify the FSM in Verilog HDL using one-hot state encoding.

[3]

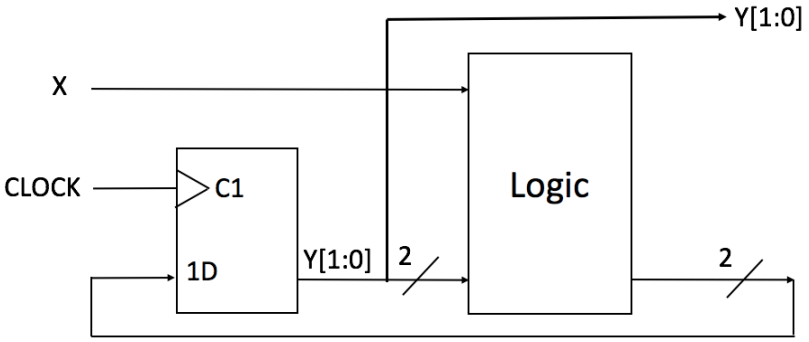

Figure 1.1

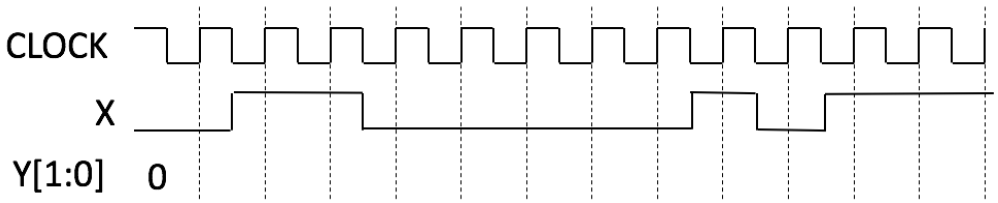

Figure 1.2

(b) *Figure 1.3* shows a pipelined circuit with three flip-flops: FF1, FF2 and FF3, and two combinational logic circuit modules: P and Q. All flip-flops are rising-edge triggered. The clock-to-output and the setup time of the flip-flops are 2 ns and 3 ns respectively. The propagation delays of P and Q are in the range of 2 ns – 6 ns and 3 ns – 5 ns respectively.

(i) Derive the maximum operating frequency of the circuit.

[3]

(ii) If FF2 is triggered on the falling edge instead of the rising edge as shown in *Figure 1.4*, derive the maximum operating frequency of the circuit. State any assumptions used.

[5]

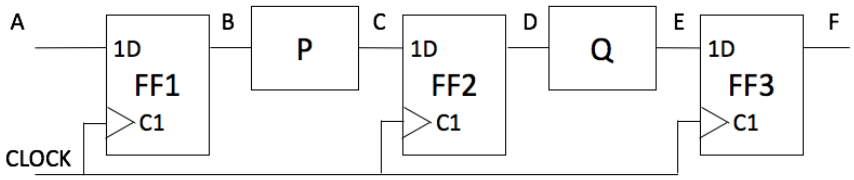

Figure 1.3

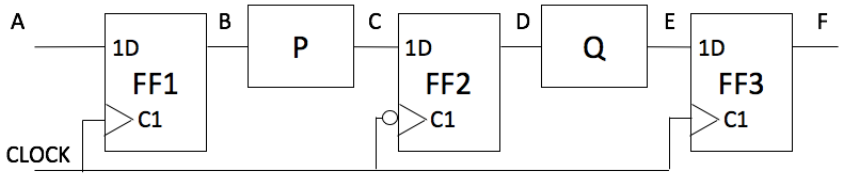

Figure 1.4

(c) A circuit with a 4-bit unsigned input X[3:0] and a 4-bit unsigned output Y[3:0] is required to perform a decoding function as described by the following pseudo-code:

```
if X < 5
      Y = X
else if  X < 12
      Y = X + 3
else
      Y = X - 2
```

(i) Design this decoder circuit in Verilog HDL with the following interface declarations:

```
module decoder (X, Y);
   input    [3:0] X;
   output   [3:0] Y;
```

[6]

(ii) If the decoder is implemented using Altera Cyclone V FPGA, estimate the number of Advance Logic Modules (ALM) required.

[2]

(d) You are required to convert a 12-bit digital number to an analogue voltage over the voltage range of 0 to 3.3V with a Digital-to-Analogue Converter (DAC).

(i) What is the resolution of the analogue output?

[2]

(ii) *Figure 1.5* shows the circuit of a 4-bit DAC using R-2R ladder architecture, four electronic switches and a current summing operational amplifier. Derive the value I_o flowing through the bottom 2R resistor (in terms of R). Hence or otherwise, derive the value of I_{in}, the input current from the voltage reference V_{ref}. What is the output voltage V_{out} of the DAC with the switch setting as shown in *Figure 1.5*?

[6]

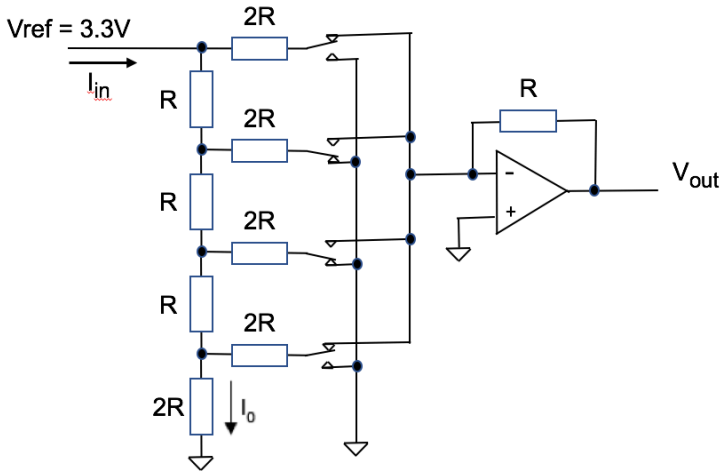

Figure 1.5

(e) A 16-bit microprocessor system has 32k byte of RAM, 8k byte of ROM and two I/O devices each occupy 4 bytes of the memory address space. The microprocessor has a 16-bit address bus A[15:0]. The starting addresses of the RAM, ROM and I/O devices are shown in *Figure 1.6*.

(i) What is the address range of each of the devices?

[4]

(ii) Design in the form of Boolean equations the chip select signals RAM_CS, ROM_CS, IO1_CS and IO2_CS. You may assume that the chip select signals are low-active in all cases.

[4]

Device	Starting Address (in Hex)
RAM	0000
ROM	A000
I/O 1	FE00
I/O 2	FF00

Figure 1.6

2. *Figure 2.1* shows the state diagram of a finite state machine (FSM) which has two inputs, X and Y, and one output, Z. Transitions from a state to itself have been omitted. The symbol "?" denotes "don't care" and "!" is logical inversion.

   (a) Construct the state table for the FSM including both the next state and the value of the output, Z.

   [8]

   (b) Complete the timing diagram of *Figure 2.2* by showing the sequence of states that the state machine follows and the waveform of the output signal.

   [6]

   (c) The FSM is implemented using the circuit shown in *Figure 2.3*. It consists of two flip-flops and a 16 x 3-bit ROM. Determine the contents of the first 8 locations of the ROM given that the state assignments S[1:0] are: A = 00, B = 01, C = 10, D = 11.

   [10]

   (d) Given that the address-to-data access time of the ROM is 5 ns, the D-to-Q delay, and the setup time of the flip-flops are 2 ns and 1 ns respective, what is the maximum frequency at which this FSM will operate correctly?

   [2]

   (e) If one-hot state encoding is used, what is the size of the ROM required to implement this FSM? Hence, or otherwise, explain why one-hot state encoding is less effective in this implementation.

   [4]

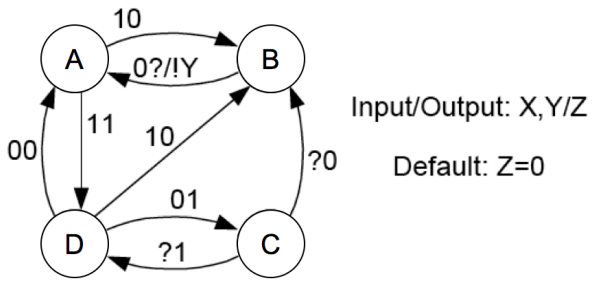

Figure 2.1

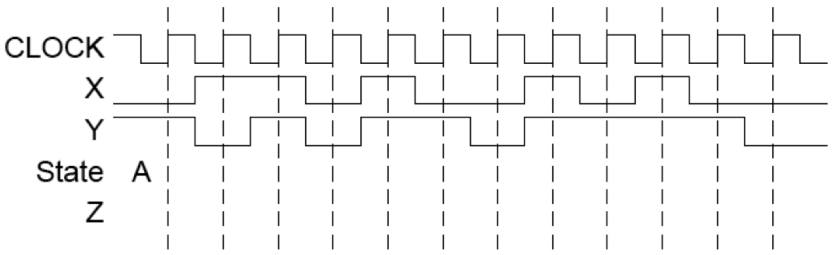

Figure 2.2

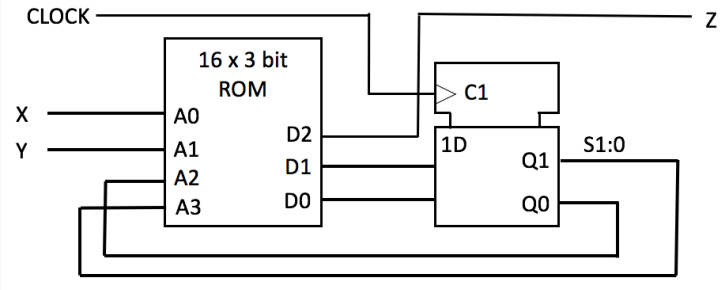

Figure 2.3

3. In a binary serial data transmission scheme, each transmitted bit occupies a bit period having a duration of 1 μs. For a logical 0, the transmitted signal is low throughout the bit period. For a logical 1, a short pulse is transmitted at the start of the bit period. To prevent long intervals without any transmitted pulses, the transmitter inserts an additional period containing a pulse whenever four consecutive zero bits have been transmitted. *Figure 3.1* illustrates the transmission of the bit sequence 11100000101 in which the inserted bit period is marked with an asterisk '*' in the figure. The frequency of CLOCK is 8 MHz.

   (a) The output signal D of the transmitter is connected to the receiver circuit of *Figure 3.2* which consists of a 6-bit counter, three AND gates and one OR gates. On each rising edge of CLOCK the counter is incremented unless D is high in which case it is reset to 0. All pulses on D last for exactly one CLOCK cycle with signal transitions occurring slightly after the CLOCK rising edge.

   Draw a timing diagram showing the data sequence of *Figure 3.1* and the resultant waveforms of D, V, W, X and Y. On your diagram, show the decimal value of Q5:0 during each output pulse on X or Y. Do not attempt to show the waveform of CLOCK on your diagram.

   [15]

   (b) Modify the circuit so that output pulses are suppressed for the bit period that immediately follows a sequence of four consecutive 0 bits. You may use any standard logic elements provided you fully specify their operation.

   [15]

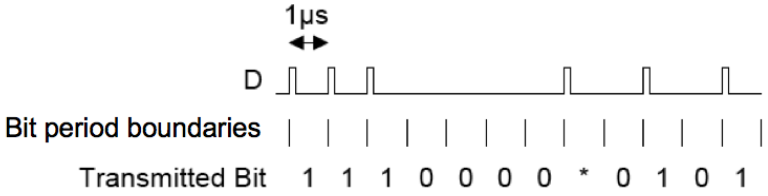

Figure 3.1

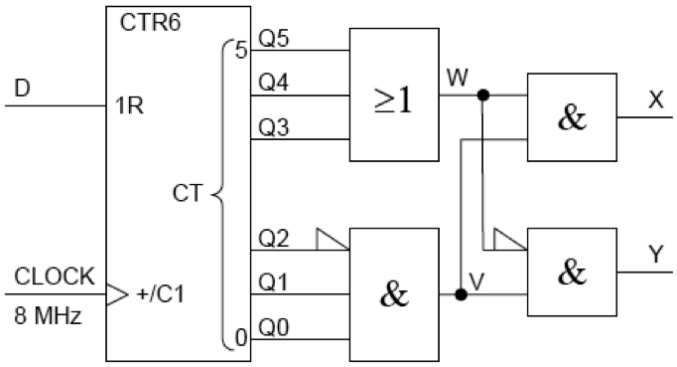

Figure 3.2