Imperial College London

Problem Class

Tutorial Problem Sheet 1

Synchronous Circuits

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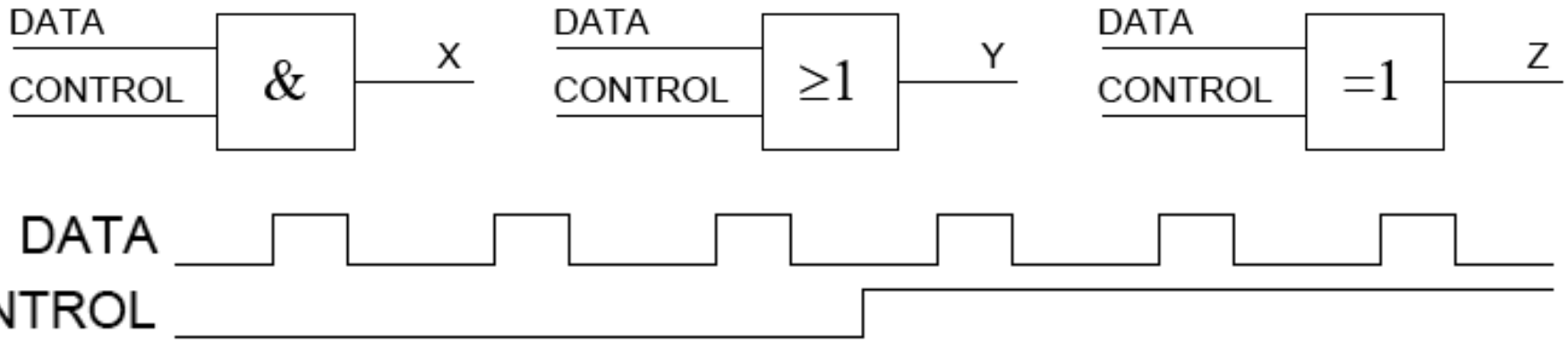
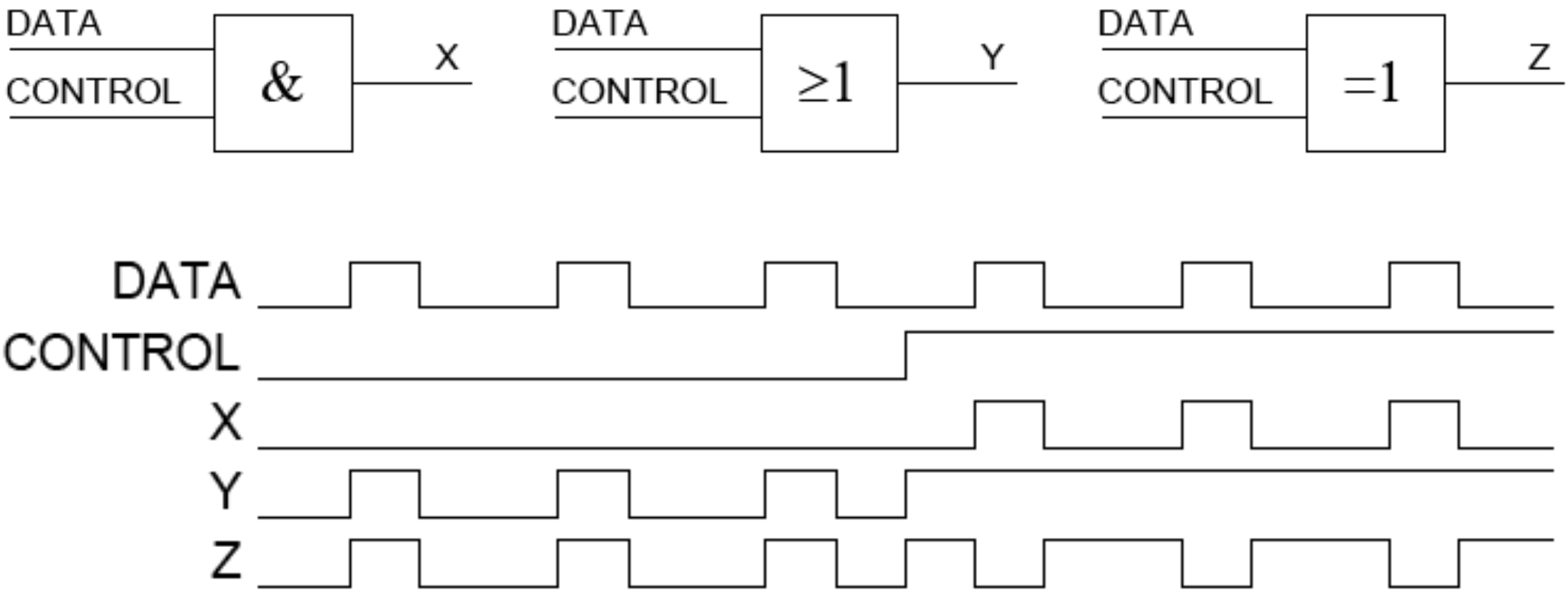
Problem 1 - Test yourself (Sheet 1 Q1)

The diagram shows three gates in which one input (CONTROL) is being used to modify a signal at the other input (DATA). Complete the timing diagram by drawing the waveforms of X, Y and Z. Describe in words the effect each of the gates has on DATA when CONTROL is low and when it is high.

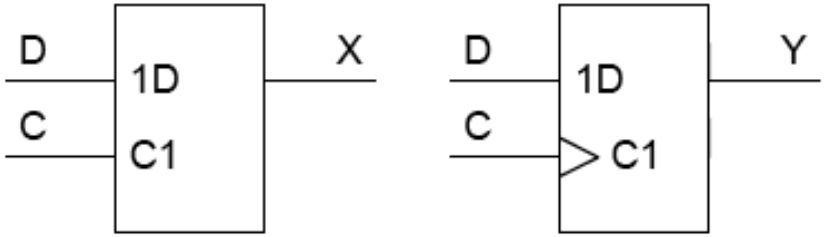


Solution 1: Test yourself

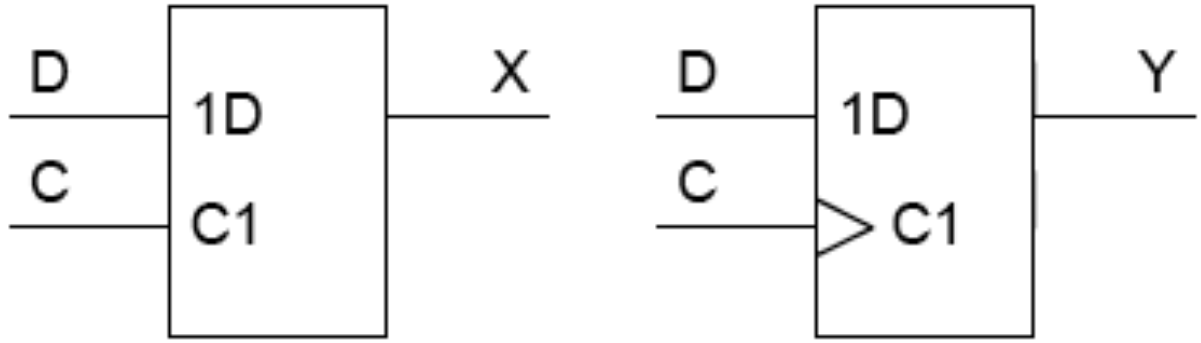


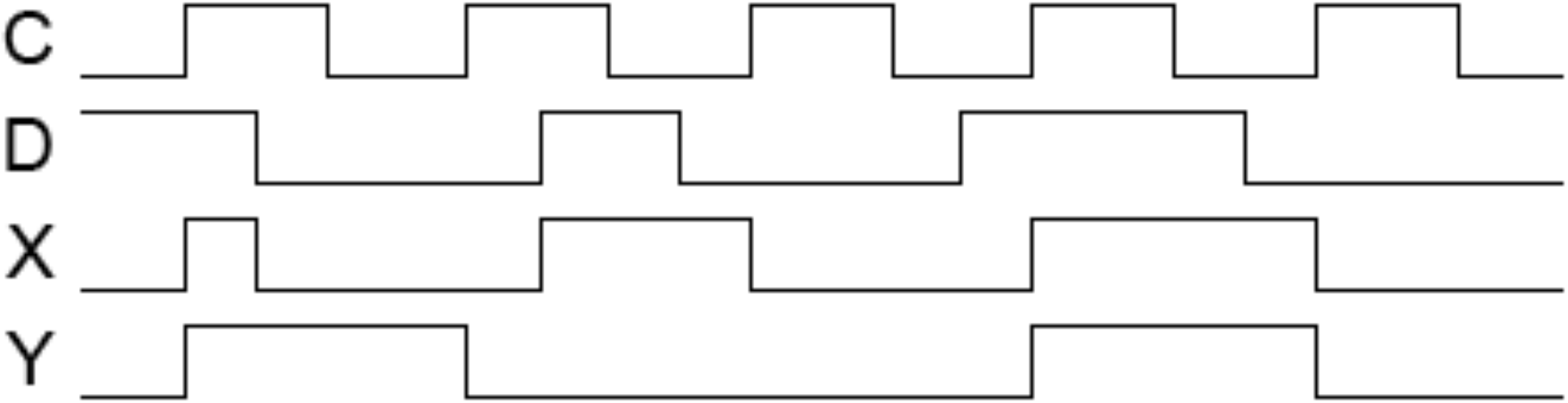
Problem 2 - Test yourself (Sheet 1 Q2)

The circuits below are a D-latch and a D-flipflop. Complete the timing diagram by drawing the waveforms of X and Y assuming that they are both low initially.



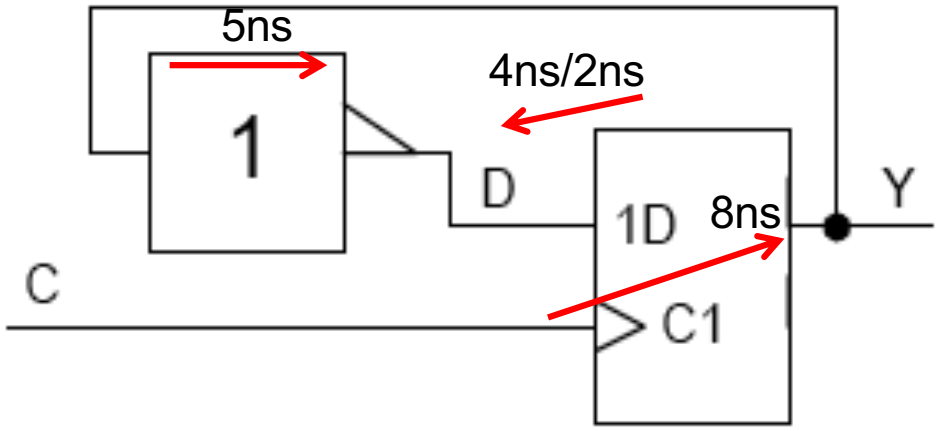
Solution 2: Test yourself





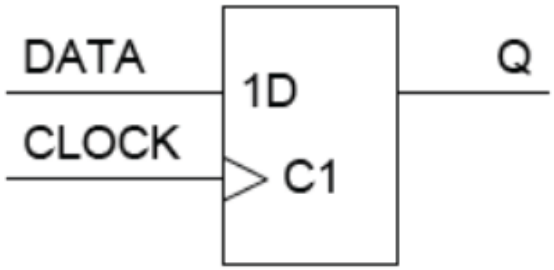
Problem 3: Explain it (Sheet 1 Q3)

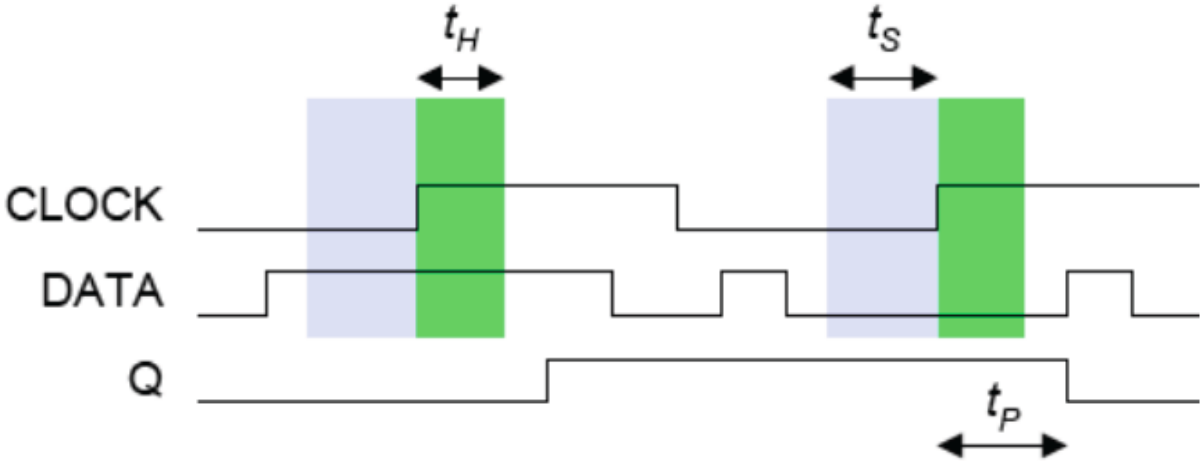
The circuit below forms a ÷2 counter. If the inverter has a propagation delay of 5 ns and the propagation delay, setup time and hold time of the flipflop are 8 ns, 4 ns and 2 ns respectively, calculate the highest clock frequency for reliable operation.



Solution 3: Explain it (setup and hold times)

The DATA input to a flipflop or register must not change at the same time as the CLOCK.



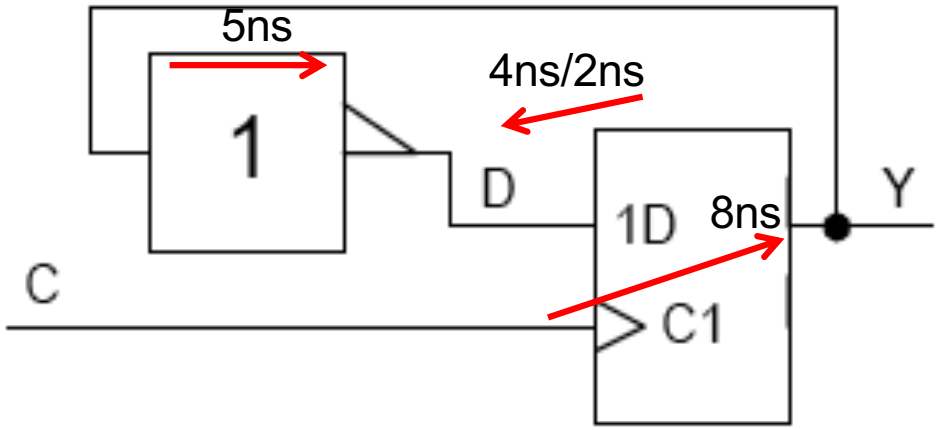


Setup Time: DATA must reach its new value at least t_S before the CLOCK↑ edge.

Hold Time: DATA must be held constant for at least t_H after the CLOCK↑ edge.

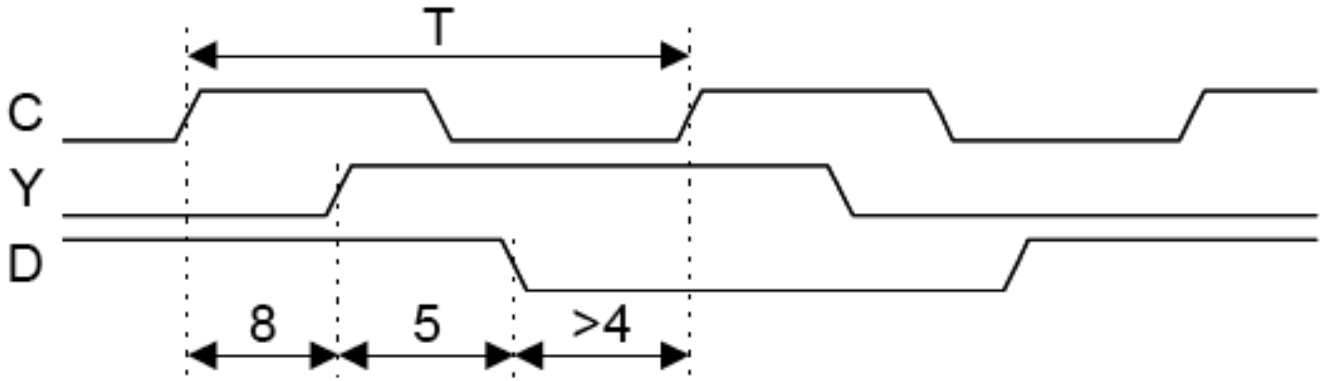
Solution 3: Explain it

The circuit below forms a ÷2 counter. If the inverter has a propagation delay of 5 ns and the propagation delay, setup time and hold time of the flipflop are 8 ns, 4 ns and 2 ns respectively, calculate the highest clock frequency for reliable operation.



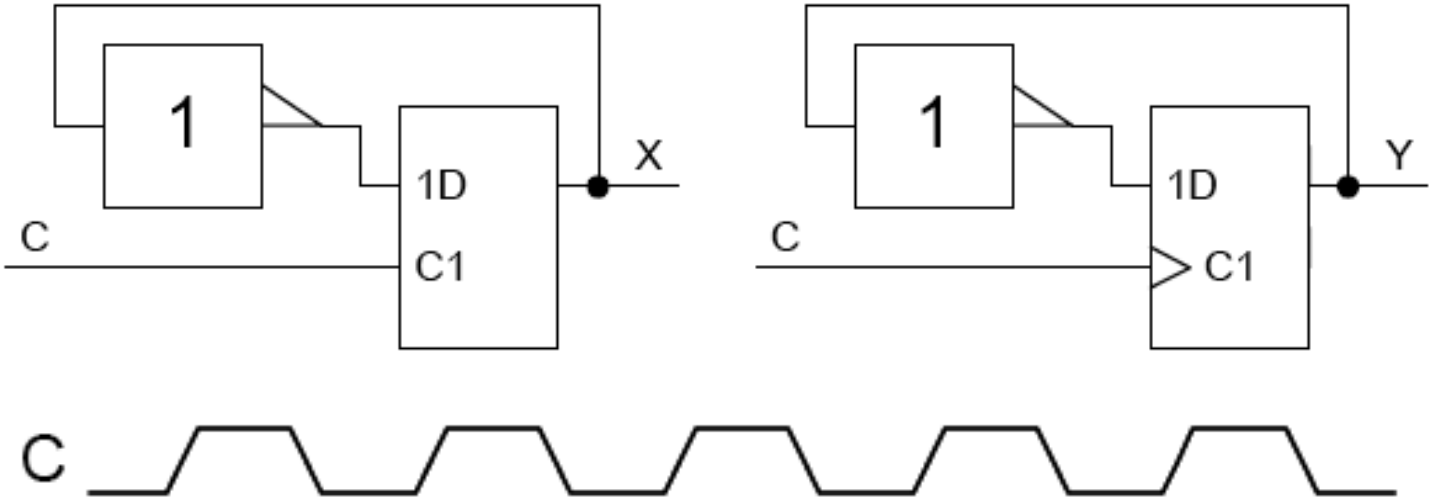
$$T-(5+8)>4 \quad \Rightarrow \quad T>17\,\text{ns}$$

$$\Rightarrow \quad f<58.8\,\text{MHz}$$

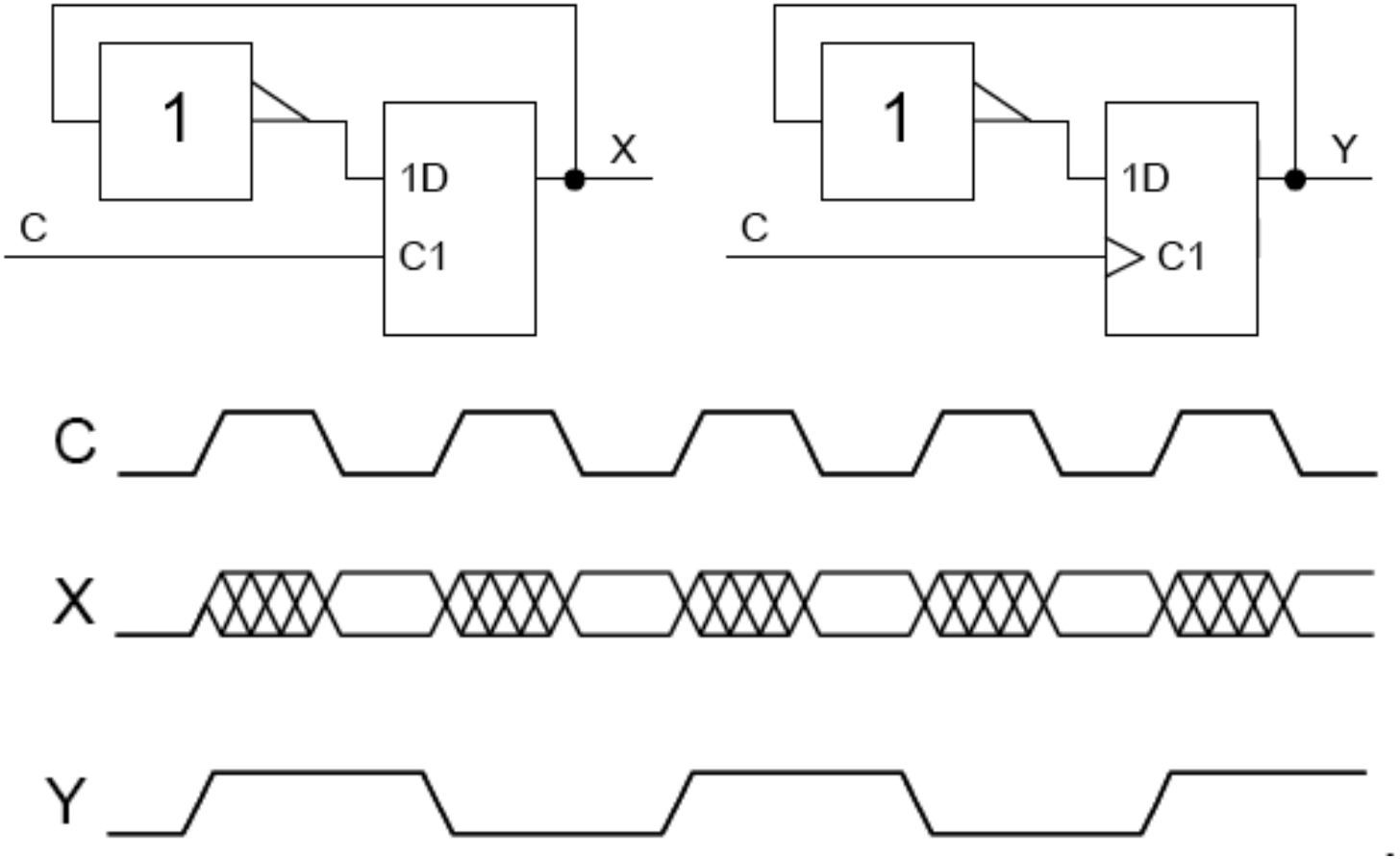


Problem 4: Test yourself (Sheet 1 Q4)

The circuits below are a D-latch and a D-flipflop with their outputs connected to their inputs via an inverter. Draw the waveforms of X and Y assuming that they are both low initially and that C is a uniform square wave. (One of these circuits is a disaster and should never be used)



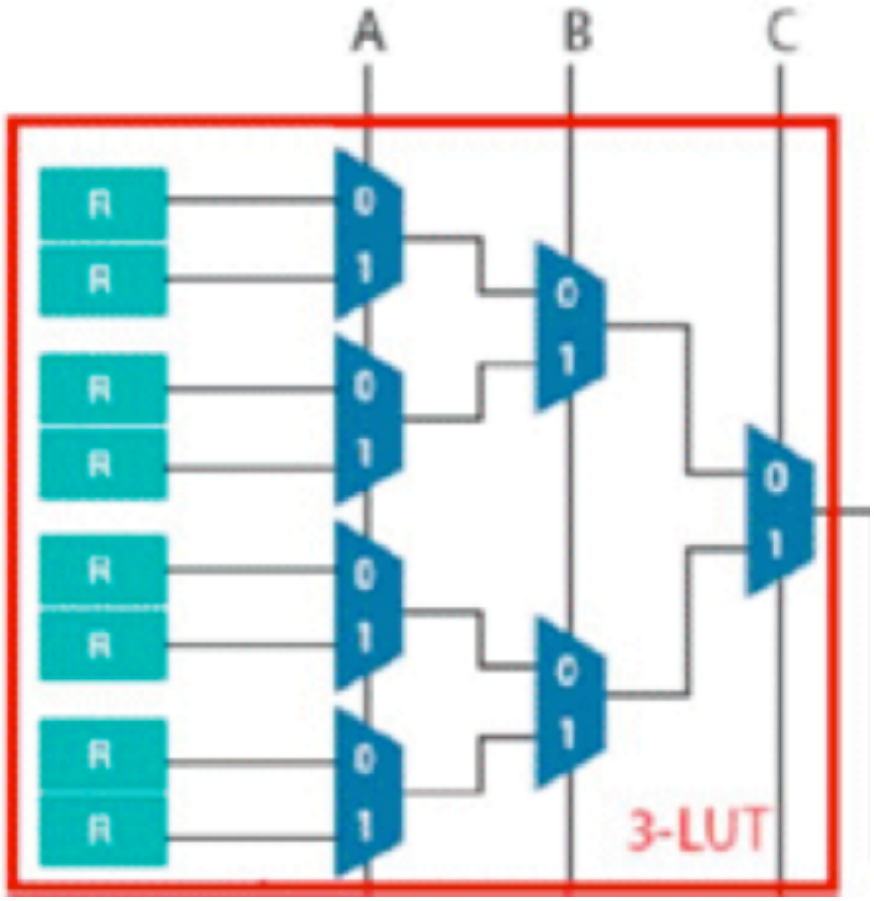
Solution 4: Test yourself



Problem 5: Test yourself (Sheet 1 Q5)

The 3-input Look-up Table (LUT) circuit could be made up from eight 2-to-1 multiplexers as shown here. Determine the configuration bits that must be stored in the eight registers driving this 3-LUT in order to implement the Boolean function:

Y = A*/C + /B*C + /A*B

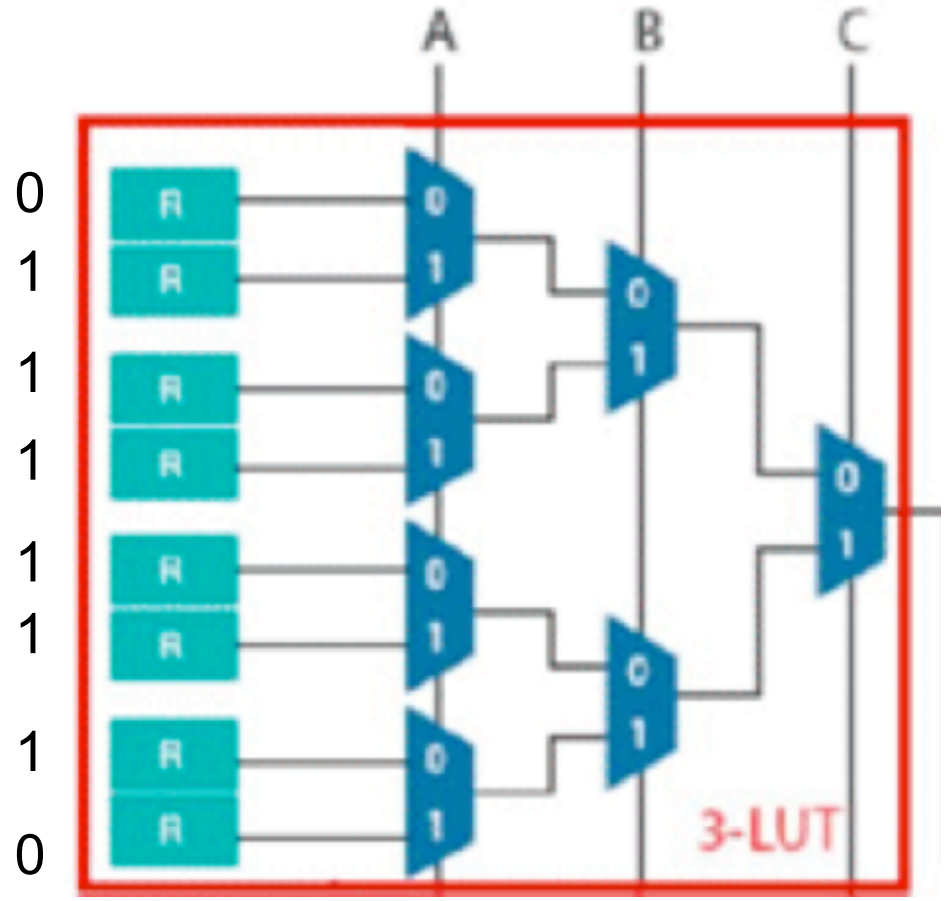


Solution 5: Test yourself

Y = A*/C + /B*C + /A*B

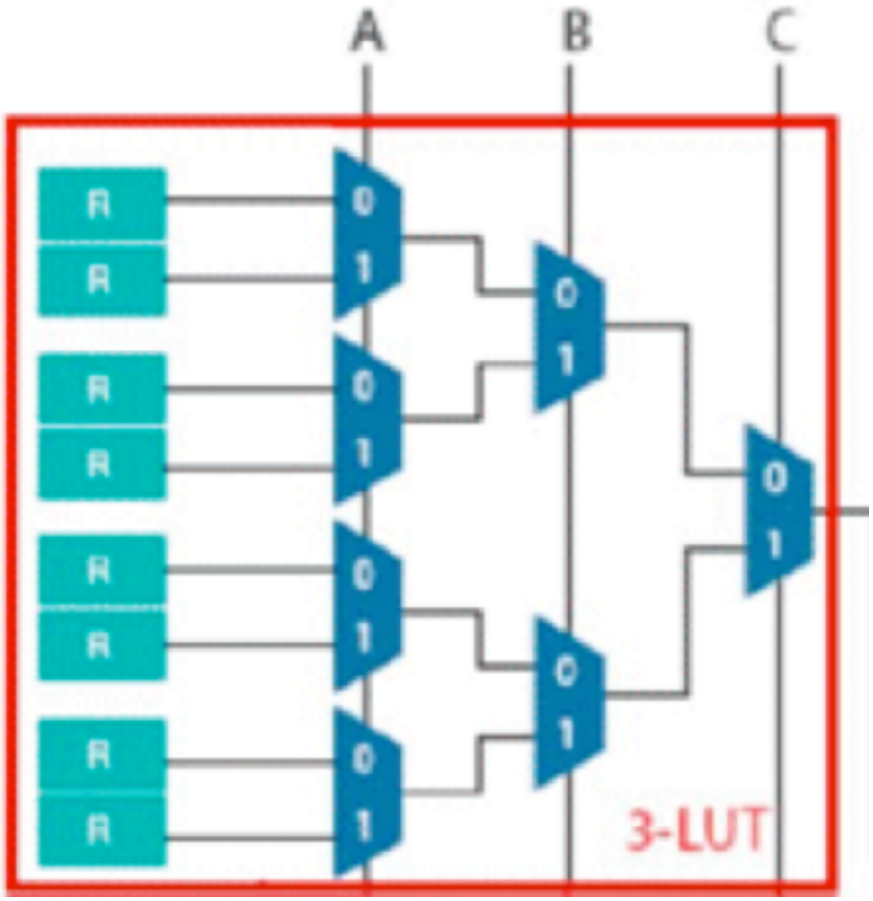
Truth table:

C	B	A	Y output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



Problem 6: Explain it (Sheet 1 Q6)

Design in Verilog HDL the hardware module LE_3LUT that implements the 3-LUT circuit shown above.



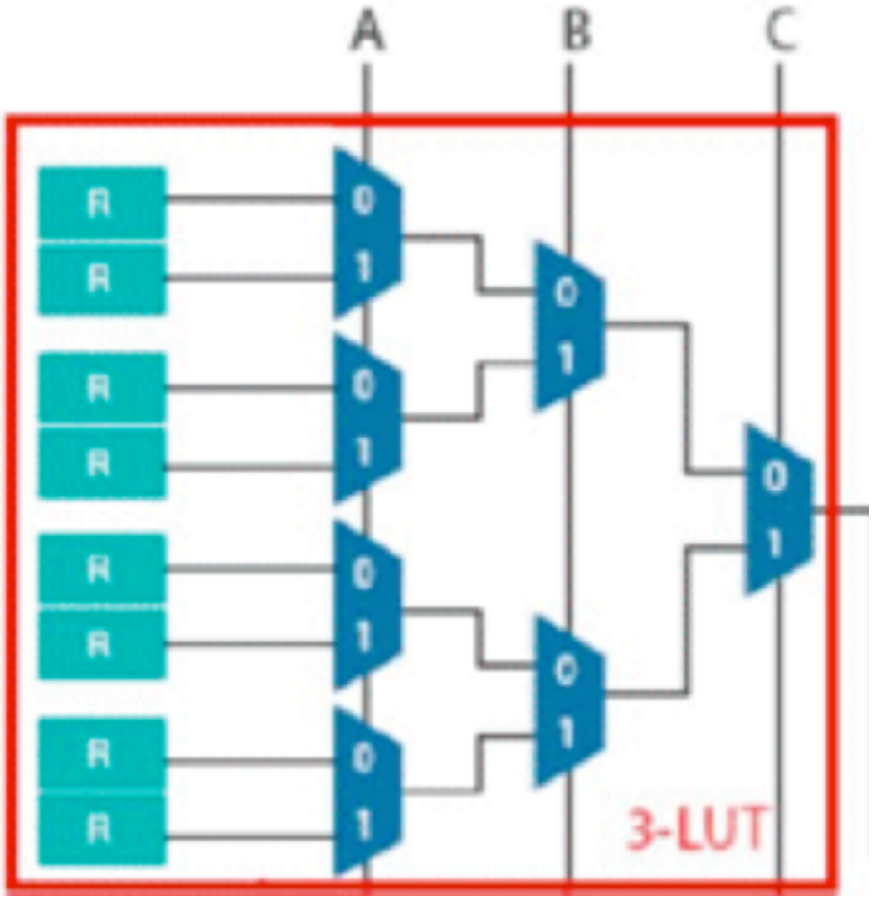
Solution 6: Explain it (Sheet 1 Q6)

```
// Implementation of a 3_LUT circuit
module lut_3 (out, in, A, B, C);

    output          out;
    input [7:0]      in;     // input value to LUT
    input           A, B, C;  // control for LUT

    assign   out =  C ?
        (B ? (A ? in[7] : in[6]) : (A ? In[5] : in[4]))
       :(B ? (A ? In[3] : in[2]) : (A ? In[1] : in[0]));

endmodule
```




```
// … instantiate the LUT
….
lut_3   q6_logic (out, 8'b01111110, A, B,C);
```