Imperial College London

Problem Class 2

Tutorial Problem Sheet 2

Counters & Shift Registers

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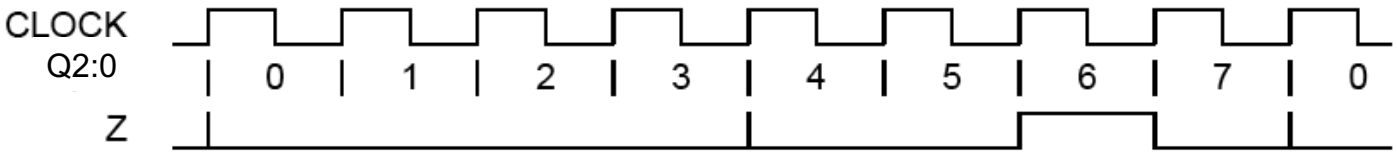
Problem 1: Test yourself (Sheet 2 Q1)

Q2:0 is the output of a 3-bit binary counter whose input is a constant frequency squarewave, CLOCK. Give a Boolean expression for Z in terms of Q2:0 such that Z is high whenever Q2:0 has the value 6. Draw a timing diagram showing the waveforms of CLOCK and Z and the value of Q2:0 during each clock cycle. Indicate on your diagram where glitches might occur in Z.

Solution 1: Test yourself

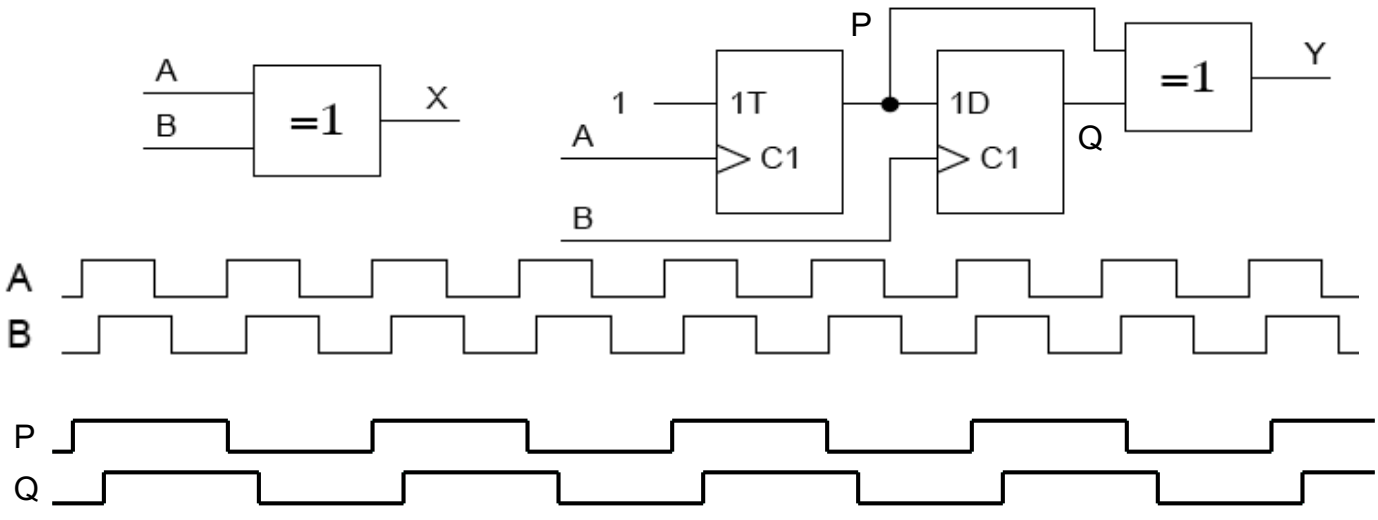
Q[2:0] = 6 when Z = Q2•Q1•~Q0

Glitch only occurs if ALL Q2, Q1 and Q0 change. Therefore only 3 ➔ 4 and 7 ➔ 0



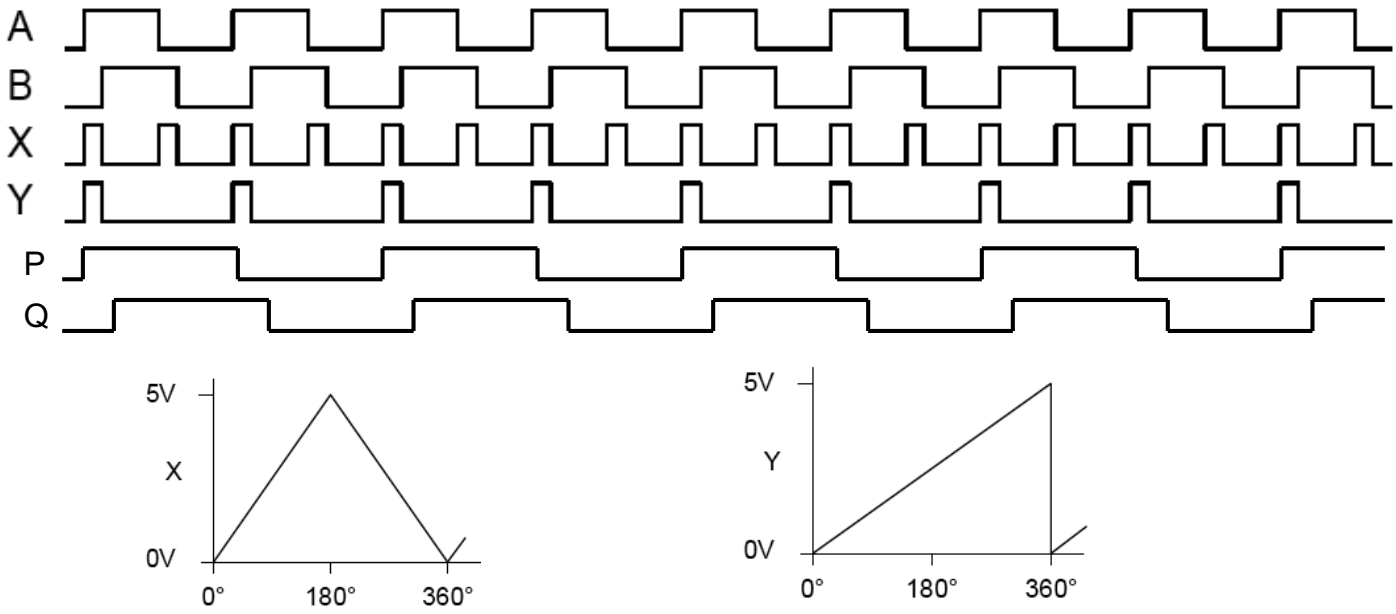
Problem 2: Explain it (Sheet 2 Q2)

The diagram shows two *phase-detector* circuits. Inputs A and B are symmetrical squarewaves with the same frequency but differing phases. Complete the timing diagram by showing the waveforms of X and Y for the case when B lags A by 45°. If logical 0 and 1 correspond to 0 V and 5 V respectively, sketch graphs showing how the DC components (i.e. average values) of X and Y vary with the phase difference.



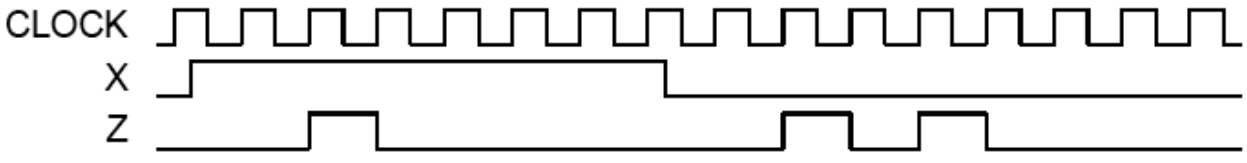
Solution 2: Explain it

The XOR gate goes high twice per cycle whereas the more complicated circuit only goes high once per cycle. The advantage of the complicated circuit is that it covers a full 360° monotonically.



Problem 3: Test yourself (Sheet 2 Q3)

The signal X forms the input to a shift register that is clocked by CLOCK↑. As shown in the timing diagram, the signal Z gives one pulse when X goes high and two pulses when it returns low. If the successive outputs from the shift register are A, B, C, … derive a Boolean expression for Z.



Solution 3: Test yourself

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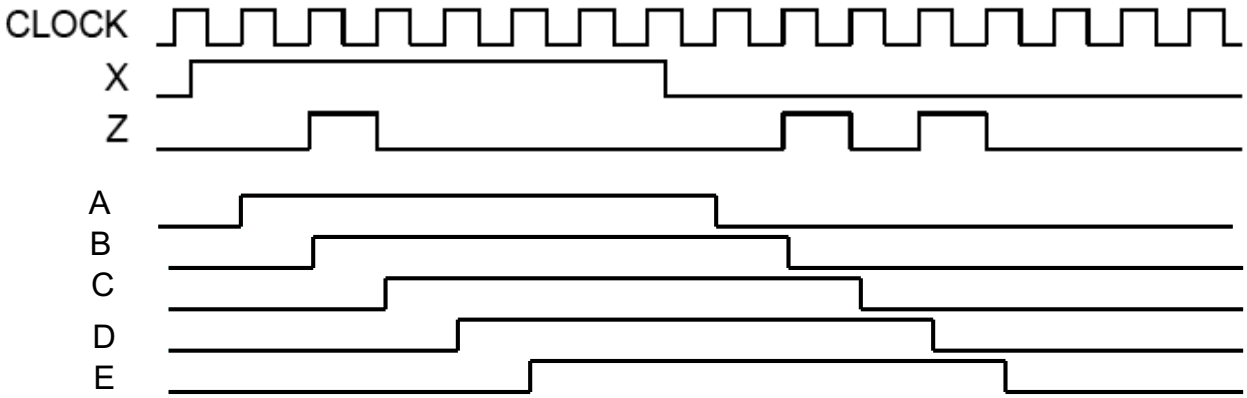
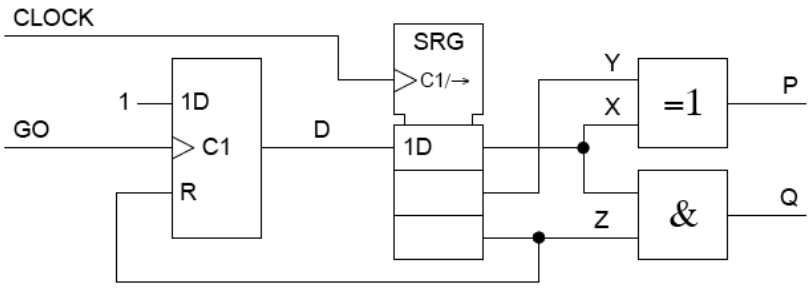
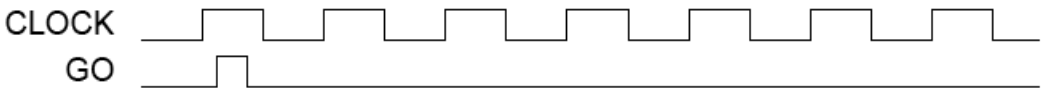


$$Z = B \oplus C + !D \bullet E$$

Problem 4: Test yourself (Sheet 2 Q4)

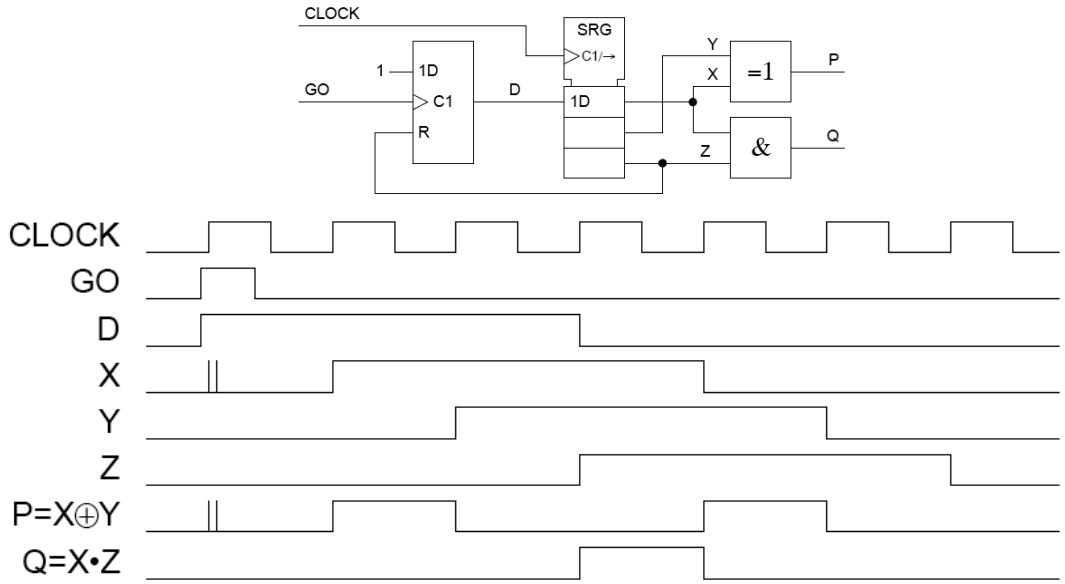
Complete the timing diagram by drawing the waveform of P and Q. Explain why only one of these signals is certain to be glitch-free. If the GO pulse occurs at a random time with respect to the CLOCK, determine the average time delay in CLOCK periods between the GO↑ edge and the Q↑ edge.





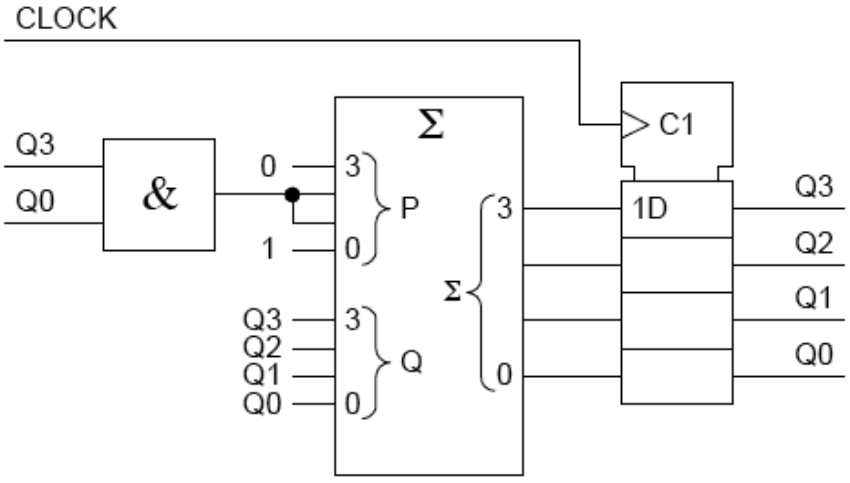
Solution 4: Test yourself

The output of the first shift-register stage can go metastable if D↑ occurs just before the CLOCK↑ edge. This will only affect the P output because Z will be low at the time which will force Q low regardless of X.
The average time delay between GO↑ and Q↑ will be 2½ clock periods.

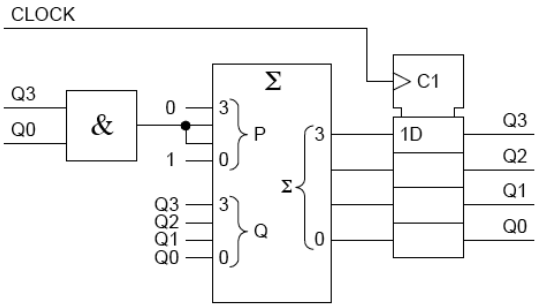


Problem 5 (Sheet 2 Q5): Explain it

The diagram shows an AND gate, a 4-bit register and an adder connected together to form a counter. List the values taken by the P input of the adder for all possible values of Q3:0. Draw a state diagram showing the sequence of values taken by Q3:0 on successive CLOCK pulses.



Solution 5: Explain it



The P input of the adder equals 7 when Q is 9, 11, 13 or 15. For all other values of Q it equals 1. Bearing in mind that the adder result is modulo 16 (i.e. 10+7=1), this results in the following state diagram: