Imperial College London

Problem Class 3

Shift Register part 2 and Finite State Machines Part 1 (Problem Sheet 2 & 3)

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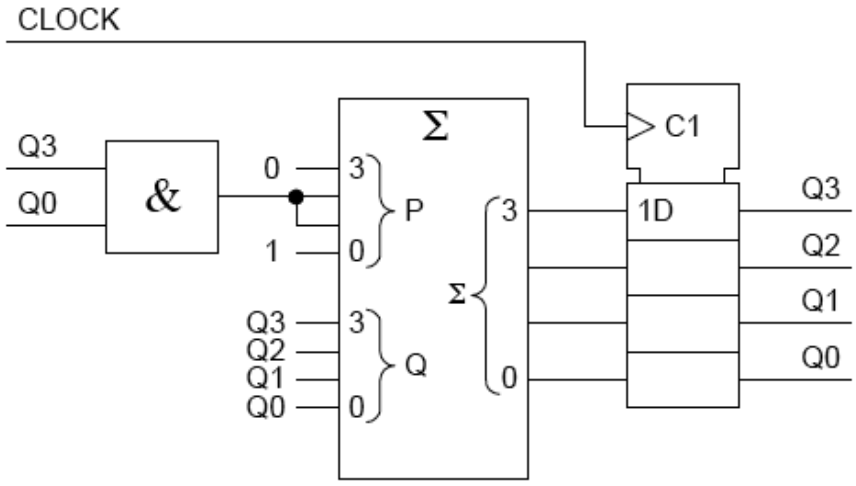
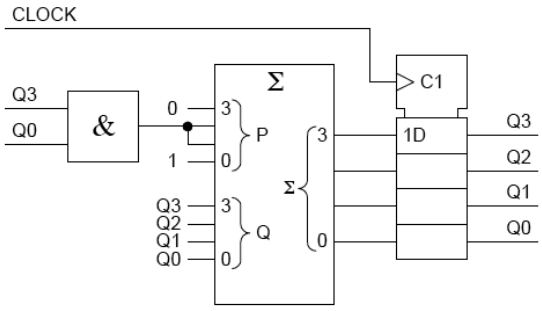
Problem 1 (Sheet 2 Q5): Explain it

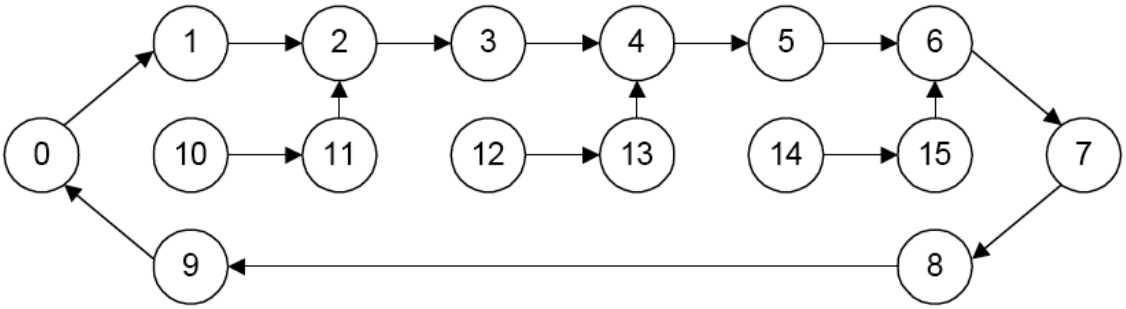
The diagram shows an AND gate, a 4-bit register and an adder connected together to form a counter. List the values taken by the P input of the adder for all possible values of Q3:0. Draw a state diagram showing the sequence of values taken by Q3:0 on successive CLOCK pulses.



Solution 1: Explain it

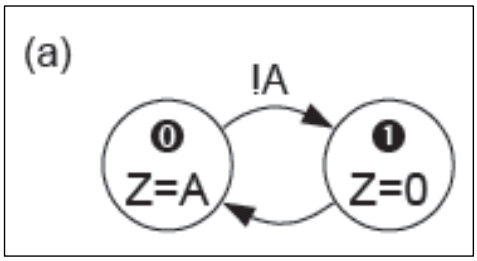


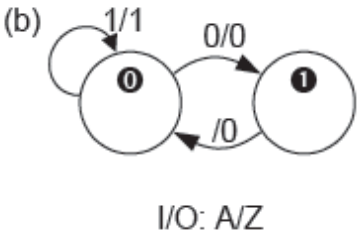
The P input of the adder equals 7 when Q is 9, 11, 13 or 15. For all other values of Q it equals 1. Bearing in mind that the adder result is modulo 16 (i.e. 10+7=1), this results in the following state diagram:



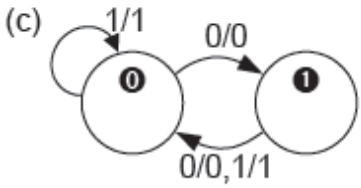
Problem 2: Test yourself (Sheet 3 Q1)

Say which of the following state diagrams denote the same state machine as version (a). Where an arrow is marked 0/1, for example, it means when A=0, the output Z will be 1 and the transition will be taken at the next CLOCK rising edge.

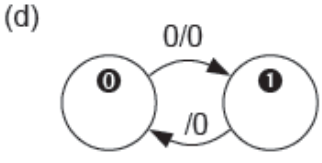




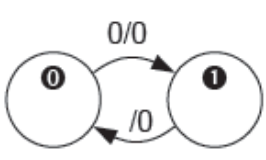
I/O: A/Z



I/O: A/Z



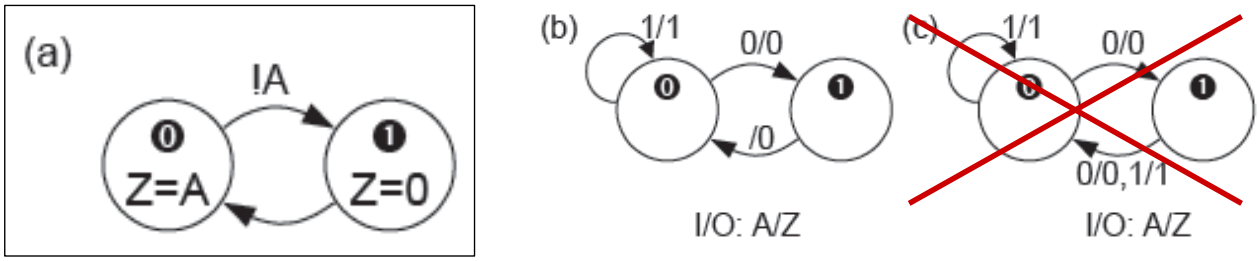
I/O: A/Z
Default: Z=1



I/O: A/Z

Solution 2: Test yourself (Sheet 3 Q1)

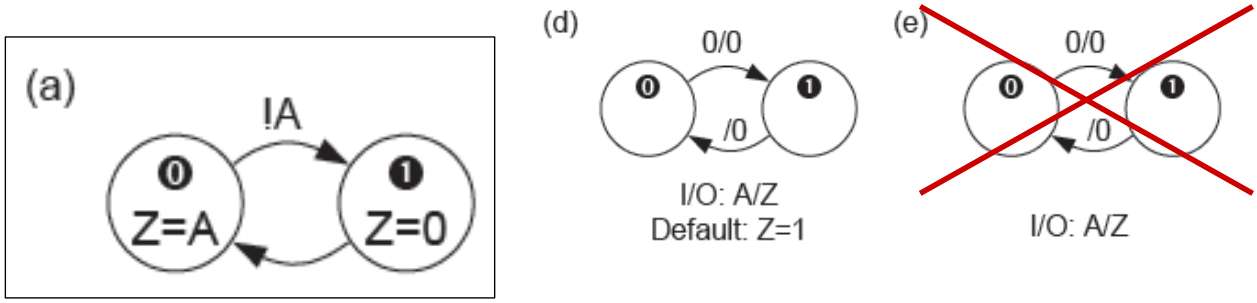
In comparing state diagrams, you should first check the transitions and then check that the outputs are the same in each state. It can be seen that the transitions are the same for all the versions. However the outputs are incorrect in version (c) and version (e).



When output are marked on arrows they refer to the state from which the arrows originate. In version (c) therefore, state 1 has an output Z=A instead of Z=0 as it should be.

Solution 2: Test yourself (Sheet 3 Q1)

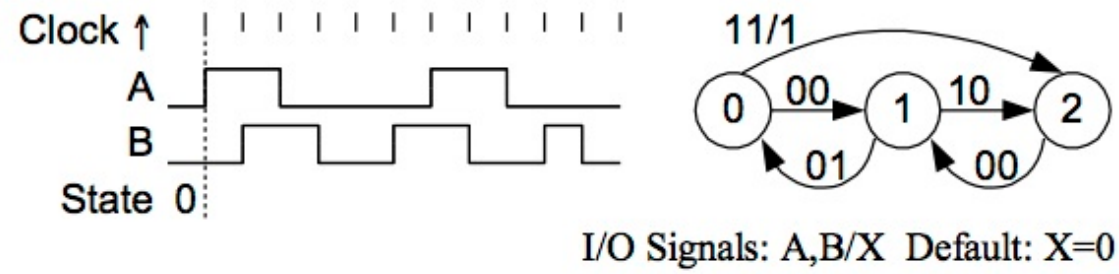
Say which of the following state diagrams denote the same state machine as version (a). Where an arrow is marked 0/1, for example, it means when A=0, the output Z will be 1 and the transition will be taken at the next CLOCK rising edge.



In version (e), the output is not specified for the case A=1 in state 0. It must either be specified by default as in version (d) or else explicitly as in version (b).

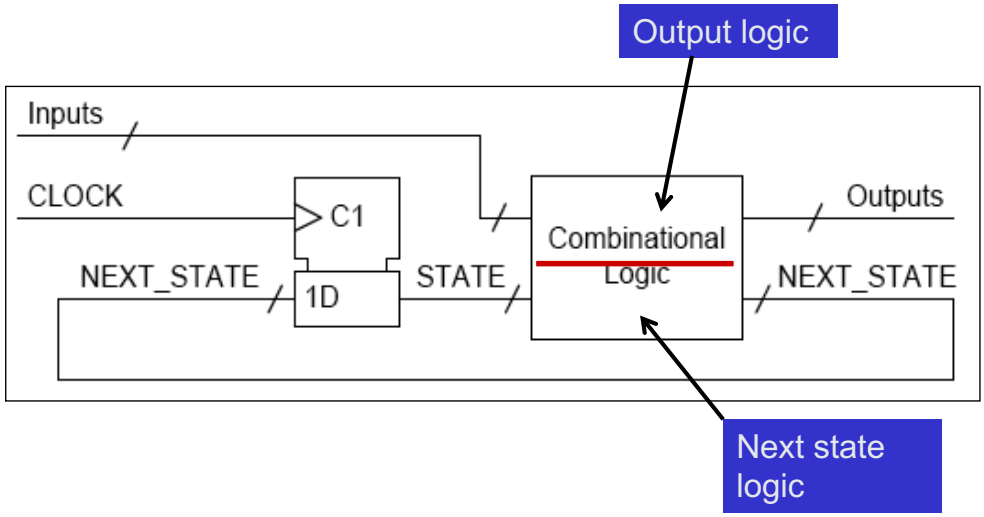
Problem 3: Explain it (Sheet 3 Q2)

The state diagram and input waveforms of a state machine are shown below. All input and state transitions occur shortly after the clock rising edge. Complete the timing diagram by indicating the value of the state during each clock cycle and by drawing the waveform of X. The initial state is 0 as shown.



Synchronous State Machines (L5, S3)

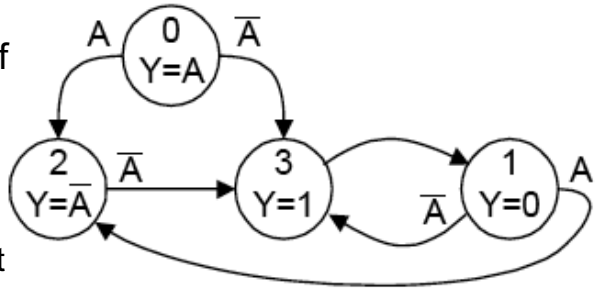
- **Synchronous State Machine (also called Finite State Machine)**
  = Register + Logic

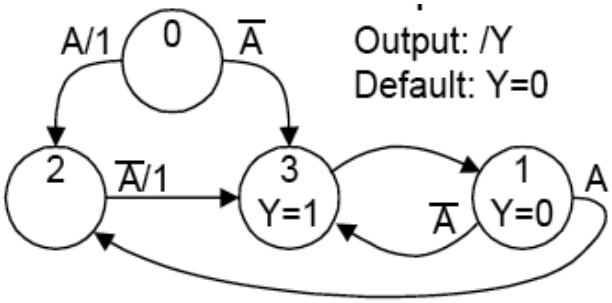


- **Mealey machine –** output can change middle clock cycle
- **Moore machine –** output is associated only with the state the FSM is in

Output Expressions on Arrows (L5, S9)

- It may make the diagram clearer to put output expressions on the arrows instead of within the state circles:
  - Useful if the same Boolean expression determines both the ***next state*** and the ***output signals***
  - For each state, the output specification must be ***either*** inside the circle *or else* on ***every*** emitted arrow
  - If self transitions are omitted, we must declare default values for the outputs

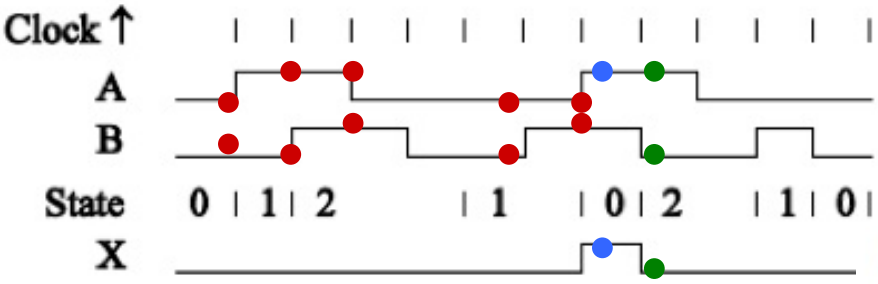


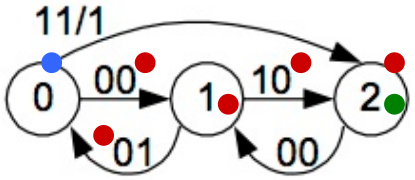


- Outputs written on an arrow apply to the state ***emitting*** the arrow.
- Outputs still apply for the entire time spent in a state
- This does not affect the Moore/Mealy distinction
- This is a notation change only

Solution 3: Explain it (Sheet 3 Q2)

You should first determine the state sequence. The transitions depend on the value of A and B immediately *before* the Clock ↑ edge. A common mistake is to use the values *after* the edge.





I/O Signals: A,B/X Default: X=0

Note that X is only ever high in state 0 and then only if A and B are high. A common mistake is to make X high in state 2 rather than state 0: remember that outputs on transition arrows refer to the preceding state.

Problem 4: Test yourself (Sheet 3 Q3)

A synchronous state machine has its state represented by the 2-bit number S1:0 and has a single input signal DIR. The current state is stored in a D-type register whose input NS1:0 is defined by: $NS1 = S0 \oplus DIR$ and $NS0 = \overline{S1 \oplus DIR}$
Draw the state transition table for the state machine.

Solution 4: Test yourself (Sheet 3 Q3)

This represents a 2-bit bidirectional counter whose counting sequence has only one bit changing at a time.

$$NS1 = S0 \oplus DIR$$
$$NS0 = \overline{S1 \oplus DIR}$$

DIR	S1	S0	NS1	NS0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1