Imperial College London

Problem Class 4

More State Machines (Problem Sheet 3 con't)

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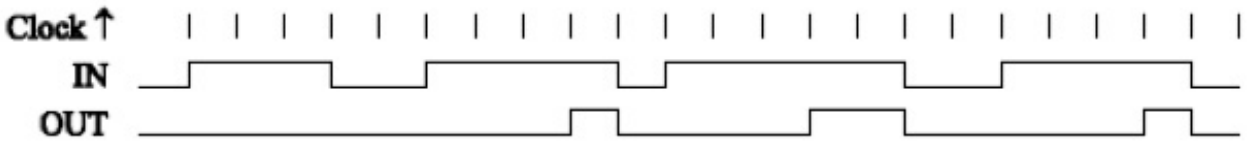
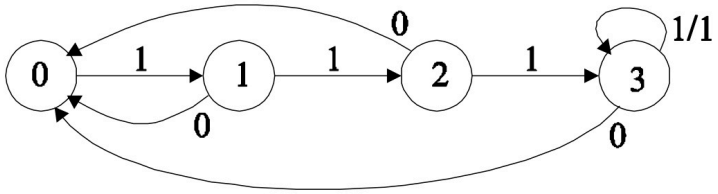
Problem 1: Test yourself (Sheet 3 Q4)

Draw the state diagram for a state machine whose output goes high when the input is high for four or more clock cycles. As shown in the timing diagram, the output should go high during the fourth clock cycle and remain high so long as the input does. Input and state transitions occur shortly after the clock rising edge.

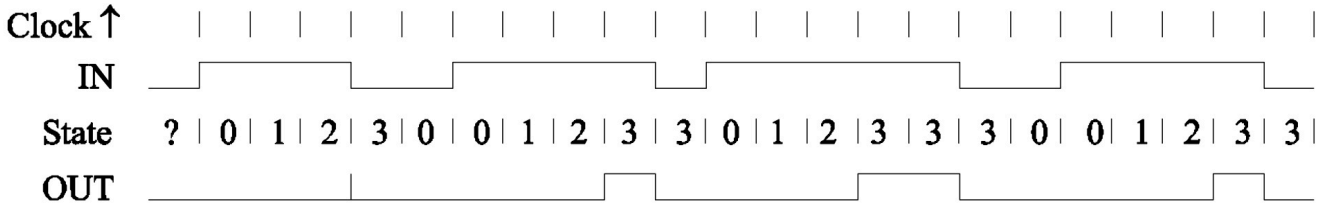


Solution 1: Test yourself (Sheet 3 Q4)

Since the output must go high during the fourth clock cycle in response to the value in that cycle, we must have a Mealy machine: a Moore machine would insert too much delay. If IN=1 during the current cycle then we want OUT=1 if the previous three (or more) cycles had IN=1. We therefore need to remember how many of the previous cycles had IN=1: 0, 1, 2 or ≥3. We therefore need four states.

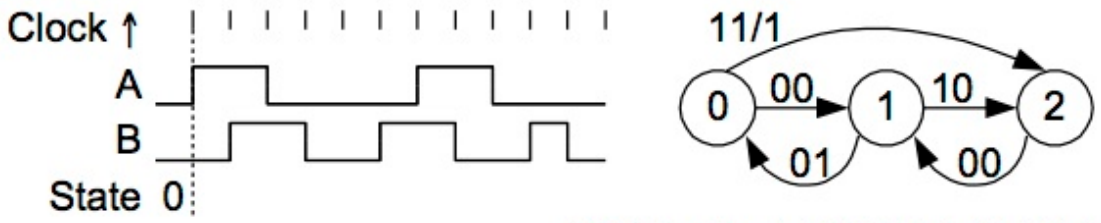


I/O Signals: IN/OUT
Default: OUT=0



Problem 2: Explain it (Sheet 3 Q2)

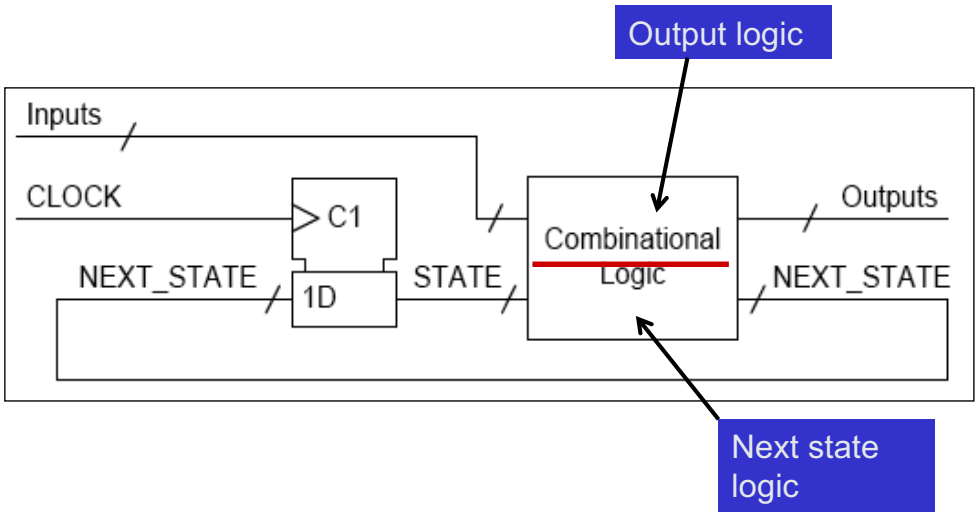
The state diagram and input waveforms of a state machine are shown below. All input and state transitions occur shortly after the clock rising edge. Complete the timing diagram by indicating the value of the state during each clock cycle and by drawing the waveform of X. The initial state is 0 as shown.



I/O Signals: A,B/X Default: X=0

Synchronous State Machines (L5, S3)

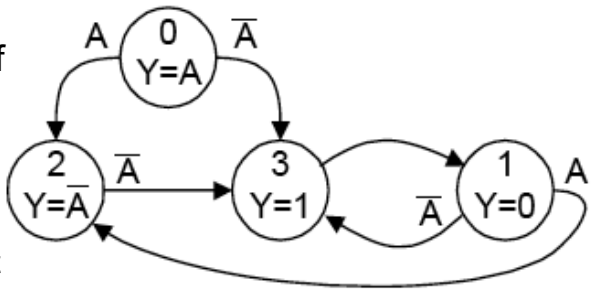
- **Synchronous State Machine (also called Finite State Machine)**
  = Register + Logic

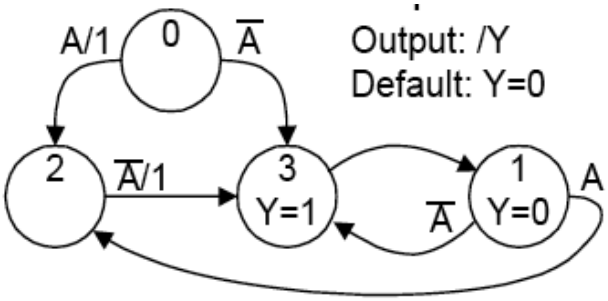


- **Mealey machine –** output can change middle clock cycle
- **Moore machine –** output is associated only with the state the FSM is in

Output Expressions on Arrows (L5, S9)

- It may make the diagram clearer to put output expressions on the arrows instead of within the state circles:
  - Useful if the same Boolean expression determines both the ***next state*** and the ***output signals***
  - For each state, the output specification must be ***either*** inside the circle *or else* on ***every*** emitted arrow
  - If self transitions are omitted, we must declare default values for the outputs

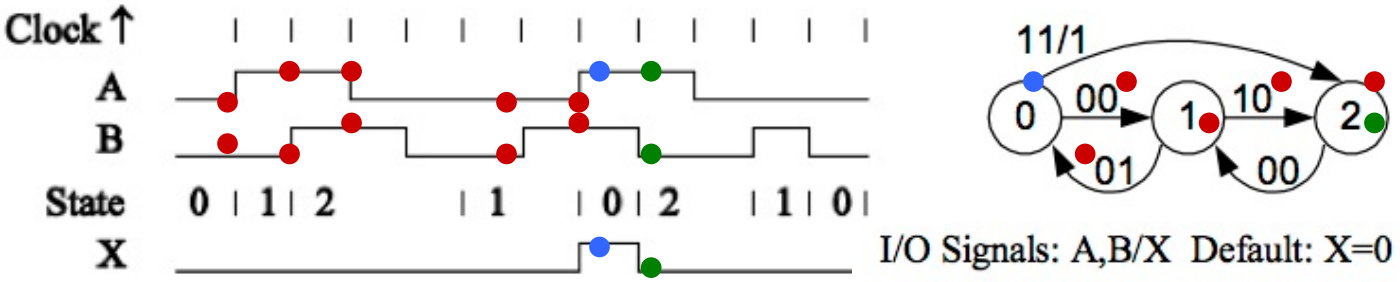




- Outputs written on an arrow apply to the state ***emitting*** the arrow.
- Outputs still apply for the entire time spent in a state
- This does not affect the Moore/Mealy distinction
- This is a notation change only

Solution 2: Explain it (Sheet 3 Q2)

You should first determine the state sequence. The transitions depend on the value of A and B immediately *before* the Clock ↑ edge. A common mistake is to use the values *after* the edge.



Note that X is only ever high in state 0 and then only if A and B are high. A common mistake is to make X high in state 2 rather than state 0: remember that outputs on transition arrows refer to the preceding state.

Problem 3: Test yourself (Sheet 3 Q3)

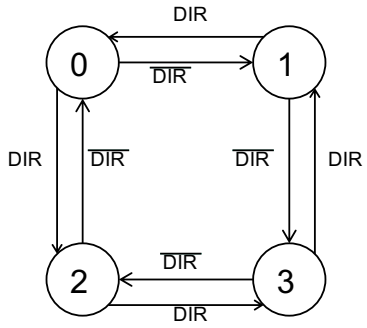
A synchronous state machine has its state represented by the 2-bit number S1:0 and has a single input signal DIR. The current state is stored in a D-type register whose input NS1:0 is defined by: $NS1 = S0 \oplus DIR$ and $NS0 = \overline{S1 \oplus DIR}$
Draw the state transition table for the state machine.

Solution 3: Test yourself (Sheet 3 Q3)

This represents a 2-bit bidirectional counter whose counting sequence has only one bit changing at a time.

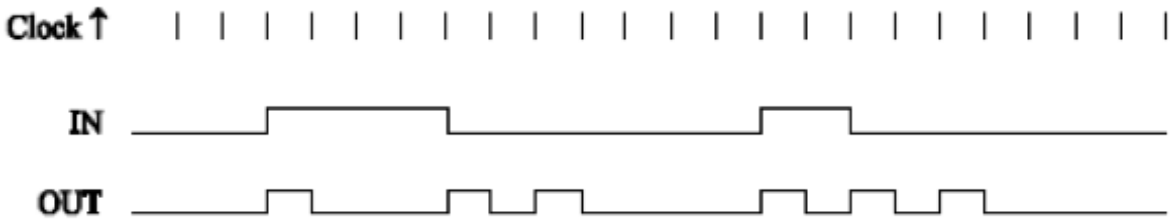
$$NS1 = S0 \oplus DIR$$
$$NS0 = \overline{S1 \oplus DIR}$$

DIR	S1	S0	NS1	NS0
0	0	0	0	1
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1



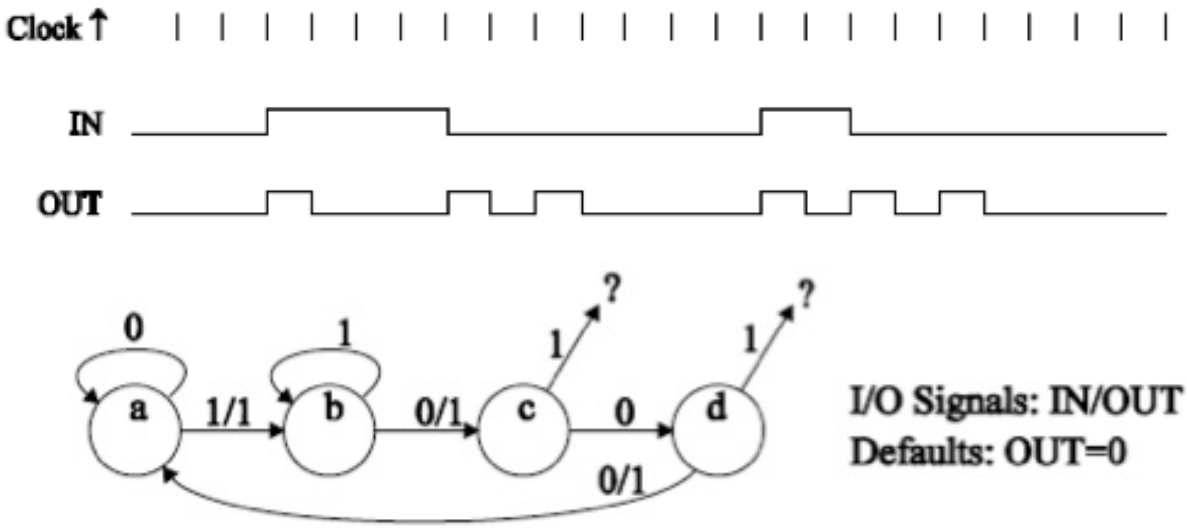
Problem 4: Explain it (Sheet 3 Q7)

Construct the state diagram for a state machine that emits a single pulse on each rising edge of its input and a double pulse on each falling edge as shown below. Each output pulse should last exactly one clock cycle. Assume that the input signal has been synchronized with the clock rising edge.



Solution 4: Explain it (Sheet 3 Q7)

We *must* use a Mealy machine in order to get zero delay between IN and OUT. The only two points of difficulty are 1) what to do if the input goes high in the middle of the double pulse sequence and 2) whether we wish to ensure that consecutive pulses are separated by at least one clock cycle.



Solution 4: Explain it (Sheet 3 Q7)

The following diagram ensures that pulses are distinct (by the addition of states e and f) and abandons pulse sequences when another input transition occurs