



Introduction to Quartus II Software

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The Altera® Quartus® II design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA and CPLD design. Quartus II software delivers the highest productivity and performance for Altera FPGAs, CPLDs, and HardCopy® ASICs.

Quartus II software delivers superior synthesis and placement and routing, resulting in compilation time advantages. Compilation time reduction features include:

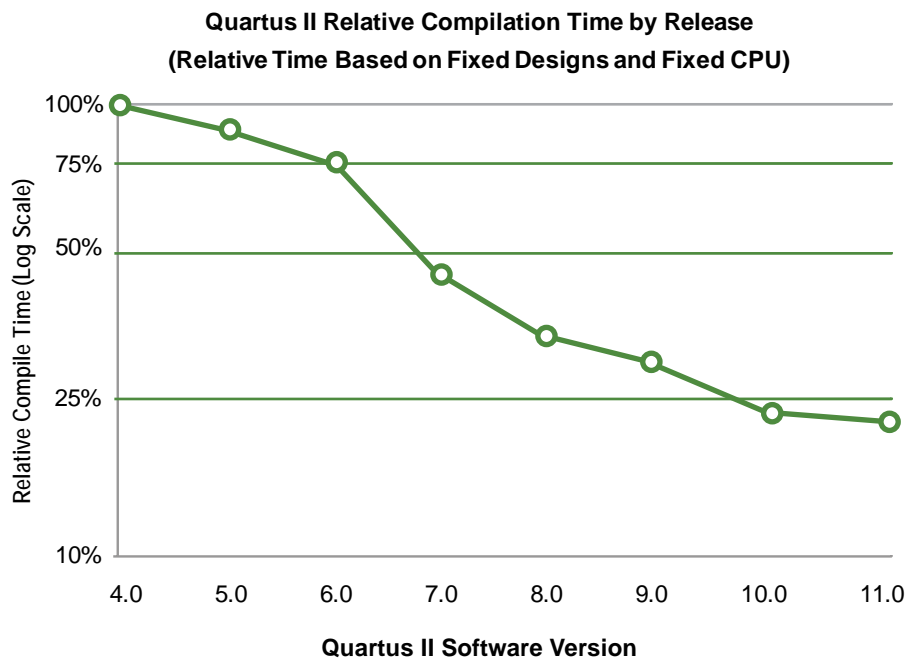
- Multiprocessor support
- Rapid Recompile
- Incremental compilation

Incremental Compilation and Rapid Recompile

Quartus II Analysis and Synthesis, together with the Quartus II Fitter, incrementally compiles only the parts of your design that change between compilations. By compiling only changed partitions, incremental compilation reduces compilation time by up to 70 percent.

For small engineering change orders (ECOs), the Rapid Recompile feature maximizes your productivity by reducing your compilation time by 65 percent on average, and improves design timing preservation.

Compilation Time Comparison



Simulation

You can perform the functional and timing simulation of your design with the ModelSim®-Altera Edition software, or any EDA simulators supported by Quartus II software. The Quartus II NativeLink feature allows you to run your third-party simulator and other EDA tools from within Quartus II software.



The Qsys system integration tool saves significant time and effort in the FPGA design process by automatically generating interconnect logic to connect IP functions and subsystems. Qsys is the next-generation SOPC Builder tool powered by a new FPGA-optimized Network-on-a-Chip (NoC) technology delivering high-performance, scalable systems, and improved design reuse opportunities.

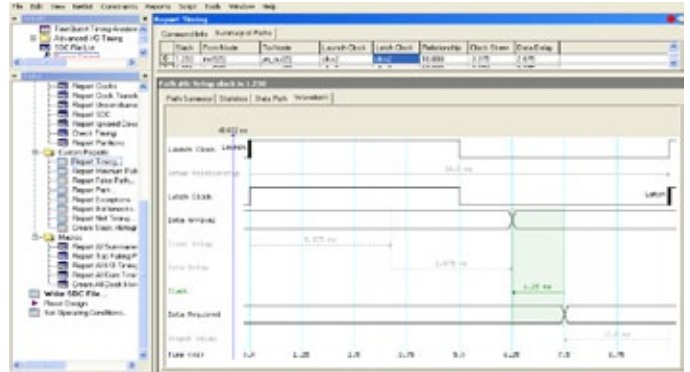
Design Entry

Your design can begin as HDL or a schematic. The MegaWizard™ Plug-In Manager helps you create or modify design files that contain custom megafunction variations, which you can then instantiate in a design file.

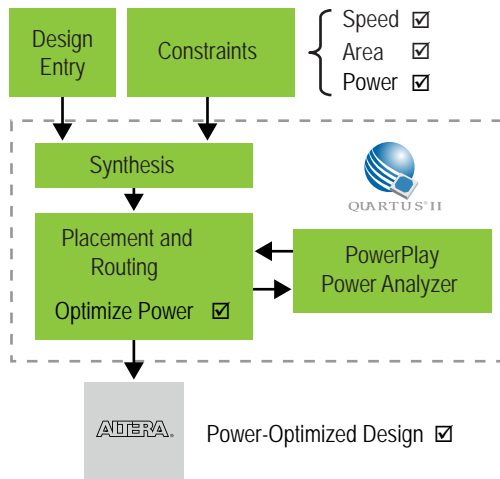
Timing and Power Analysis

The Quartus II TimeQuest timing analyzer allows you to analyze the timing characteristics of your design. Altera is the only FPGA vendor with comprehensive Synopsys Design Constraints (SDC) support in its second-generation, easy-to-use timing analyzer. The TimeQuest analyzer offers a complete GUI and scripting environment to create timing constraints and reports. It also includes a timing analysis wizard that makes it easy to create initial constraints.

TimeQuest Timing Analyzer



PowerPlay Power Analyzer Flow



The Quartus II PowerPlay power analysis and optimization tools allow you to estimate power consumption throughout the design cycle. They use power optimization technology, which provides on average a 10-percent reduction in power consumption. The Altera PowerPlay Early Power Estimator estimates power consumption and produces a Microsoft Excel-based spreadsheet with estimate information. The PowerPlay power analyzer performs post-fitting power analysis and reports power characteristics by device resource and design entity.

Verification

Quartus II software offers several tools to help you analyze the results of compilation and fitting. Verification with the SignalTap™ II logic analyzer and the System Console allows you to probe your design as it functions on the device and in the system.

Links to Online Resources

Video: Basic Compilation Flow

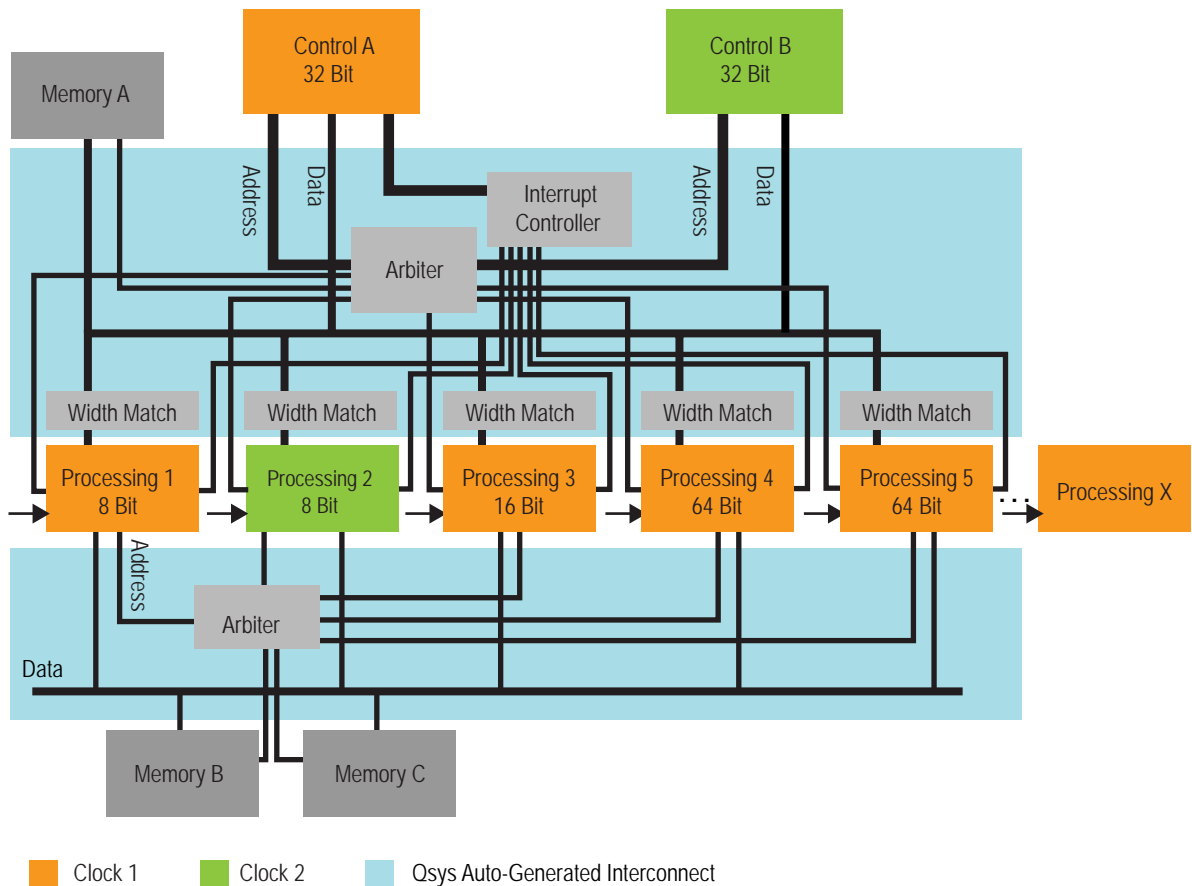
Documentation: Design Planning with the Quartus II Software

Design Entry

Qsys

The Qsys system integration tool saves significant time and effort in the FPGA design process by automatically generating interconnect logic to connect custom HDL design blocks, commonly referred to as design modules; intellectual property (IP) cores; and components. Qsys is powered by a new FPGA-optimized NoC-based technology delivering higher performance. Qsys also raises the level of abstraction and increases productivity by enabling design reuse and scalable systems.

Qsys Interconnect Fabric Example



Quartus II Block Editor

The Quartus II Block Editor allows you to enter and edit graphic design information in the form of schematics and block diagrams. The Block Editor reads and edits Block Design Files (.bdf) that contain blocks and symbols representing logic.

MegaWizard Plug-In Manager

The MegaWizard Plug-In Manager helps you create or modify design files that contain custom megafunction variations, which you can then instantiate in a design file. The MegaWizard Plug-In Manager allows you to set values for parameters and optional ports.

Design Partitions

You can assign design entities to design partitions—logical design blocks that are preserved or recompiled during incremental compilation. Incremental compilation saves you time and effort by recompiling only those design partitions you are optimizing. Quartus II software preserves previous compilation results for partitions that already meet your design requirements. The Design Partition Planner allows you to view a graphical representation of your design hierarchy and assists you in creating effective design partitions.

Links to Online Resources

Video: Design Entry

Webcast: Why You Should Evaluate Qsys System Integration Tool

Quartus II Online Help: About Design Entry

Web: Design Entry and Planning Resource Center

Documentation: Creating a System with Qsys

Incremental Design Planning and Methodology

Quartus II software is tailored to several different design methodologies, including incremental compilation design flows and block-based design flows. In a team-based incremental compilation flow, the design is divided into partitions. Each team member can functionally verify a partition independently, and then simply provide the source code for the partition to a project lead for integration. Using placeholders, the project lead can compile the larger design even if the source code is not yet complete for a partition.

Compiling all design partitions in a single Quartus II project ensures that the design is compiled with a consistent set of assignments.

Incremental design encompasses the following:

- Synthesis
- Design partitioning
- Full compilation
- Simulation, verification, and analysis, followed by changes to the design
- Recompile of only changed elements of the design hierarchy

Links to Online Resources

Video: Incremental Compilation

Video: Rapid Recompile

Web: Incremental Compilation Resource Center

Online Help: About Incremental Compilation

Documentation: Best Practices for Incremental Compilation Partitions and Floorplan Assignments

Documentation: Quartus II Handbook: Incremental Compilation for Hierarchical and Team-Based Design

Quartus Integrated Synthesis and the Fitter

Quartus II software includes a comprehensive integrated synthesis solution and advanced integration with leading third-party synthesis software vendors. Quartus II integrated synthesis fully supports the Verilog HDL and VHDL languages, and includes algorithms to minimize gate count, remove redundant logic, and use device architecture efficiently. Quartus II integrated synthesis includes advanced synthesis options and compiler directives to guide the synthesis process to achieve optimal results.

The Quartus II Fitter places and routes your design for the target device. Using the database created by Quartus II integrated synthesis, the Fitter matches the logic and timing requirements of the project with the available resources of the target device. It assigns each logic function to the best logic cell location for routing and timing, and selects appropriate interconnection paths and pin assignments.

Netlist Viewers and the Chip Planner

The Quartus II RTL Viewer, State Machine Viewer, and Technology Map Viewer provide powerful ways to view your initial and fully mapped synthesis results during the debugging, optimization, and constraint entry processes. The Chip Planner supports ECOs by allowing quick and efficient changes to your logic late in the design cycle. It provides a visual display of your post placement-and-routing design mapped to device architecture, and allows you to create, move, and delete specific routing and resource usage.

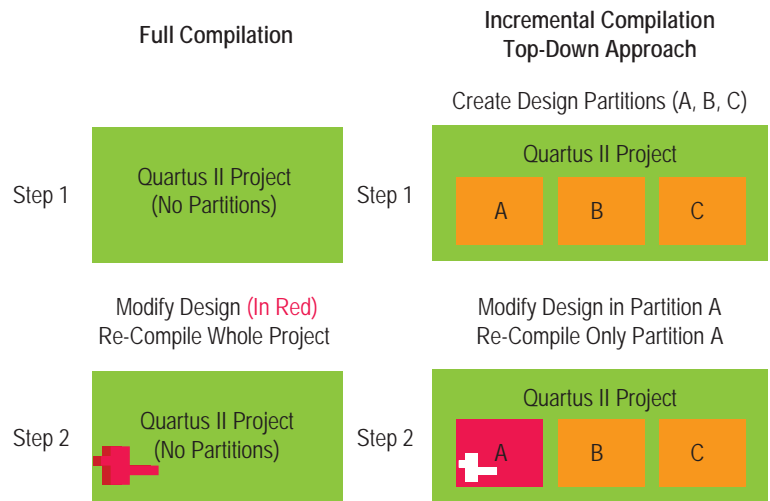
Links to Online Resources

Web: Synthesis and Netlist Viewers Resource Center

Online Help: About the Netlist Viewers

Online Help: About the Chip Planner

Compare Full and Incremental Compilation



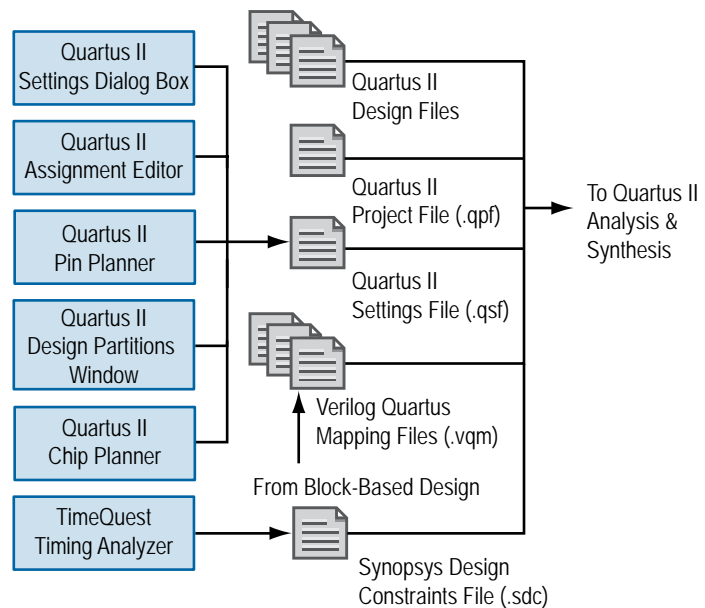
Making Assignments

Assignments allow you to specify various options and settings for the logic in your design. When you make resource assignments in your design, Quartus II software attempts to match those resource assignments with the resources on the device, meet any other constraints you have set, and then optimize the remaining logic in the design. The Assignment Editor and Pin Planner are interfaces for creating and editing pin, node, and entity-level assignments in Quartus II software. The Pin Planner allows you to make assignments to individual pins and also groups of pins. It includes a package view of the device with different colors and symbols that represent the different types of pins and additional symbols that represent I/O banks. The symbols used in the Pin Planner are very similar to the symbols used in device family data sheets.

Links to Online Resources

- Online Help: About Assignments
- Online Help: About the Pin Planner
- Documentation: Constraining Designs
- Documentation: I/O Management

Assignment Entry Flow



Simulation

You can perform functional and timing simulation of your design with the ModelSim-Altera Edition software or any EDA simulators supported by Quartus II software. Quartus II software provides the following features for performing simulation:

- NativeLink integration with simulation tools
- Generation of output netlist files
- Functional and timing simulation libraries
- Generation of testbench templates and memory initialization
- Generation of input for power analysis

Altera provides functional simulation libraries for designs that contain Altera-specific components, and atom-based timing simulation libraries for designs compiled in Quartus II software.

Quartus II software also allows you to use the EDA tools you are familiar with for other stages of the design flow, including synthesis, timing analysis, and formal verification.

Links to Online Resources

- Video: ModelSim Simulation
- Web: EDA Partners
- Online Help: About Using the ModelSim Software with the Quartus II Software
- Documentation: Simulating Altera Designs

The TimeQuest Timing Analyzer

The TimeQuest timing analyzer is a powerful ASIC-style timing analysis tool that uses industry-standard constraint, analysis, and reporting methodologies. You can use SDC commands and formatting to direct the analysis, and also to instruct the Quartus II Fitter to optimize the placement of logic in the device in order to meet timing constraints.

The TimeQuest analyzer analyzes the timing paths in the design, calculates the propagation delay along each path, checks for timing constraint violations, and reports results. If the TimeQuest analyzer reports timing violations, you can customize the reports to view precise timing information about specific paths. You can then determine whether the design requires additional timing constraints or exceptions, logic changes, or placement-and-routing constraints.

Links to Online Resources

Video: [TimeQuest Timing Analysis](#)

Web: [TimeQuest Timing Analyzer Resource Center](#)

Online Help: [About TimeQuest Timing Analysis](#)

Documentation: [The Quartus II TimeQuest Timing Analyzer](#)

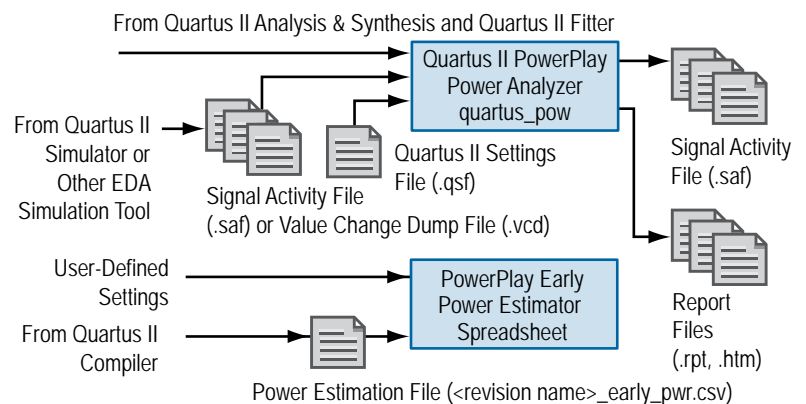
Documentation: [Best Practices for the Quartus II TimeQuest Timing Analyzer](#)

The PowerPlay Power Analyzer

The Quartus II PowerPlay power analysis tools allow you to estimate static and dynamic power consumption throughout the design cycle. The PowerPlay power analyzer produces a power report that highlights—by block type and entity—the power consumed, allowing you to plan for thermal conditions and power supply requirements.

The PowerPlay power analyzer accepts information from a variety of data sources, and analyzes it with several factors affecting power consumption. The result is a high-quality power estimate. It reports total calculated dynamic and static thermal power consumption, current consumed from voltage sources, a summary of the signal activities used for analysis, and a confidence metric detailing the various inputs on which it bases the power analysis.

Power Analysis Flow



Links to Online Resources

Video: [PowerPlay Power Analyzer - Power Analysis](#)

Web: [PowerPlay Power Analyzer Support Resources](#)

Online Help: [About the PowerPlay Power Analyzer](#)

Online Help: [Performing an Early Power Estimate Using the PowerPlay Early Power Estimator](#)

Documentation: [PowerPlay Power Analysis](#)

Verification

Quartus II software provides several verification tools that allow you to analyze your design operating in-system and at system speeds:

- The SignalTap II logic analyzer allows you to route signals through the JTAG interface to Quartus II software based on user-defined trigger conditions.
- The SignalProbe feature allows you to use otherwise unused device routing resources to route selected signals to an external logic analyzer or oscilloscope.
- The In-System Memory Content and In-System Sources and Probes Editors allow you to view and modify data in a design at run time.
- The external logic analyzer interface and virtual JTAG interface allow you fully customized interaction with your design.
- The Simultaneous Switching Noise (SSN) Analyzer supports I/O planning by estimating the voltage noise caused by the simultaneous switching of output pins.

System Console

System Console provides you with Tcl scripts and a GUI to perform low-level hardware debugging of your design, to identify a Qsys module by its path, and to open and close a debugging connection to a module. You can use the Transceiver Toolkit component of the System Console to set up channel links in your transceiver-based designs, and then automatically run EyeQ and Auto Sweep testing for a graphical view of your test.

Links to Online Resources

Video: [Transceiver Toolkit](#)

Web: [On-Chip Debugging Design Examples](#)

Documentation: [System Debugging Tools Overview](#)

For More Information

Online Help

<http://quartushelp.altera.com>

Quartus II software includes a browser-based Help system that provides comprehensive documentation for Quartus II software. The Help system is also available separately from the Quartus II software.

Knowledge Database

<http://www.altera.com/support/kdb/kdb-index.jsp>

The Altera Knowledge Database provides support solutions, frequently asked questions, and known issues.

The Quartus II Interactive Tutorial

<http://www.altera.com/education/training/courses/ODSW1050>

Quartus II software includes the Flash-based Quartus II Interactive Tutorial. The modules of this tutorial teach you how to use the basic features of Quartus II design software, including design entry, compilation, timing analysis, programming, incremental compilation, debugging, and the Qsys system integration tool.

Quartus II Handbook

http://www.altera.com/literature/hb/qts/quartusii_handbook.pdf

The Quartus II Handbook provides comprehensive information about the programmable logic design cycle from design to verification.

Altera Software Installation and Licensing manual

http://www.altera.com/literature/manual/quartus_install.pdf

The Altera Software Installation and Licensing manual provides detailed information about software requirements, installation, and licensing for Windows and Linux workstations.

Other Altera Literature

<http://www.altera.com/literature/lit-qts.jsp>

The literature that is available from the Altera website is the most current information about Altera products and features; it is updated frequently, even after a product has been released. Altera continues to add literature on the latest product features and also any additional information as requested by customers.

Web: Ordering Information <http://www.altera.com/buy/software/buy-software.html>

Training: Using the Quartus II Software: An Introduction <http://www.altera.com/education/training/courses/ODSW1100>

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