Imperial College
London

Lecturer Name: Professor Peter Cheung (1081)

Survey Name: SOLE UG Autumn 2018

Digital Electronics 2 (EE2-01)

Individual Lecturer Feedback (Professor Peter Cheung)

1) The lecturer explained the material well					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
40	8	3			

2) The lecturer generated interest and enthusiasm					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
46	5				

3) The lecturer was approachable					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
40	8	2			1

4) Overall, I am satisfied with this lecturer					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
39	12				

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback to this lecturer:

- Great lecturer! Verilog experiment was very very interesting as well!!!!!!
- The lecturer was sometimes when asked questions and very enthusiastic about his subject.
- Very good lecturer, engaging, and the small jokes here and there are very appreciated. You are good at explaining the content, but as I said earlier, less code on the slides would be appreciated.
- An extremely fair and talented genius
- Please don't change. Invite other lecturers to your lectures to show them how to teach effectively.
- This lecturer gave good impression of how the theory would be used in solving problems in the field, and they engaged the class very well. They were very involved with the module, providing very good support in addressing queries. The lecture notes were very long and detailed and provided excellent explanations of concepts.
- Great enthusiasm and very well structured lab experiment to allow practical examples of the course content. This was the best lab out of all the other experiments.
- Great and very approachable lecturer. Really enjoyed working with him !
- Overall very good experience. Sometimes more humility would be appreciated.
- His lecture is really fun and interactive. He speaks on a relatively slow phase and every words are on the point
- Professor Cheung is amazing, and I love the way he adds comments below his slides to elucidate everything clearly. But I feel that problem lectures is a bit problematic because we covered very little from each problem sheet.
- Prof Cheung, is very enthusiastic about this module and it transfers to my fellow students and me.
- The lecturer did not make clear the sort of things which we can expect to find in the exam and what is extra information. Often it was not clear what the important points were to take away from a lecture and what was more background information. I would like to see more example questions.
- You are a role model to all the other lecturers. They should look up to you as to how to structure a module so that its aligned to practicals and the lectures are relevant to it.

  Thank you
- Dr. Cheung was one of the most exciting lecturers I had so far. He was great at showing how cool his subject was and even though it was the module I was least eager for at the start I really liked the experiments he prepared and how enthusiastic he was about them.
- Most of the time, he explains well in the lecture. He usually cracks some jokes in his lecture and ask some questions for us to answer. This enables us to understand the concept easily. Sometimes whenever we ask him a question, he use our questions to ask the students. This is totally unusual but this also makes us understand his lecture well.

Immediately below are the collated numerical results received for the Module.

Module Feedback - Digital Electronics 2 (EE2-01)

1) The content of the module is well structured					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
28	18	2	3		

2) The content of the module is intellectually stimulating					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
36	11	2	2		

3) Where applicable, I have received helpful feedback on my work submitted so far					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
21	17	1	2		10

4) Overall, I am satisfied with the quality of the module					
Definitely Agree	Mostly Agree	Neither Agree or Disagree	Mostly Disagree	Definitely Disagree	Not applicable
31	16	3	1		

The following free text comments were received:

5) Please use this box to provide any additional constructive feedback on this module. Students with a disability are invited to make specific suggestions for improvement that would assist them:

- I find that a lot of the content deals with Verilog and how to write the code for different purposes, which might not be very useful for understanding digital concepts? I feel like we didn't cover much digital theory at all this year actually. But not denying that writing Verilog was fun
- The example to all academics how to: - keep the attention of the class; - integrate labs and lectures together; - provide effective and focused explanations of the topic. Overall the best taught module.
- Would be nice to have the lectures 1 week ahead of this years schedule as half the year group got lectures covering the lab session after they had said lab session
- These lectures were excellently structured, with the reasons for particular approaches to problems well elaborated on and a wealth of interesting areas covered, giving a good overview of the topic. The lectures were also very well paced, and engaging.
- There is just too much code on the slide. Too much of the lecture time is spent explaining code from slides. I think that doing the Digital Veri experiment first should be a necessity (I don't think that AMP or DFT needs to be first). This would really improve the quality of the module.
- This course is the combination of writing a code and understanding the concept. Though the code is almost similar to C++, it is fascinating for me to know. Also, except the time constraint , the other modules such as the RAM and the DAC converter are understandable.
- I didn't find classes that helpful and improving my understanding of the material compared to study groups from year 1.
- Learning a lot of verilog before the labs made it quite difficult to understand. Having 3 weeks with verilog without actually programming anything was not very useful
- Good course and good learning materials provided. Wish for more challenging study questions that resemble exams style material more. Slight contradiction with lecturer saying he will not teach coding from slides then proceeds to explain verilog from powerpoint. Good connections with the lab.
- The module jumps a bit all over the place and could be better structured with more explanation. This module would be appropriate for someone who had already learned all of this material as a review the way it was taught, but for students new to the material it is exceptionally difficult to follow and understand.
- The module was poorly structured. The beginning was mostly confusing because the lectures involved learning Verilog through slides and examples in a lecture environment. It would have been much better to introduce us to this HDL in computing labs doing exercises or small projects by ourselves. This would be great if accompanied by lectures to explain the theory involved, but not to learn how to write the code.

  The labs were really fun and I believe everyone would have enjoyed even more if we had more preparation time with Verilog beforehand. Especially because we really do not need the DE1 Board all the time and can do a lot by just writing and compiling code with Quartus.
- 1. I believe that there are much more presentations that there should be for the amount of the content given
  2. As almost all of the theoretical material given repeats itself from the last year, I think it would be great to have more examples of the code itself during lectures
  3. More code in the problem sheets
- One of the most engaging and best modules; however, there is much emphasis placed on the experiment and Verilog with little left to theory. Tutorials are great but sadly did not cover hard questions at the back of tutorial sheets/last few tutorials.
- Only one thing: the add 3 and shift algorithms could be a programming module in the compulsory task could be better.