E2.1 – Digital Electronics II

Problem Sheet 6 –Memory Interface

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1A. Explain why most memory integrated circuits have “tri-state” data output pins.

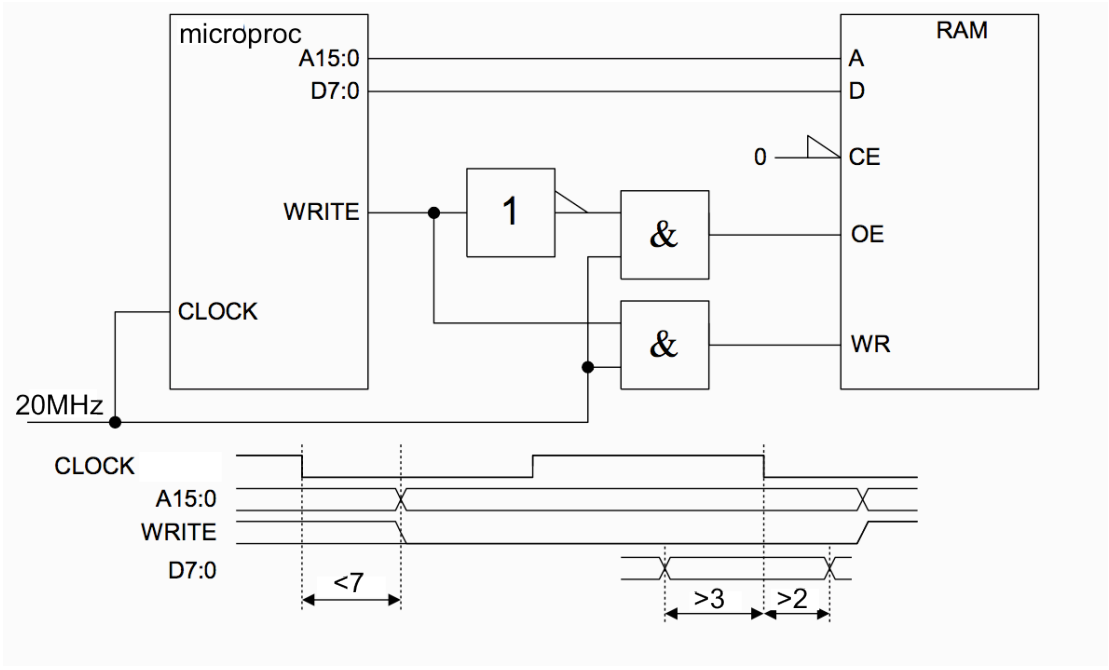
2B. In an 8-bit microprocessor system, addresses 0000 to 9FFF are occupied by RAM and addresses A000 to DFFF are occupied by ROM. The system also contains two peripheral devices: a serial port occupying addresses E100 to E107 and a parallel port occupying addresses E200 to E201. You have a supply of 8k×8 RAM integrated circuits and a supply of 16k×8 ROM integrated circuits.

a) State how many input address pins you would expect to find on each of the RAM integrated circuits, ecah of the ROM integrated circuits and on each of the peripheral device integrated circuits.

b) Derive Boolean expressions for the CE inputs of each memory and peripheral integrated circuit.

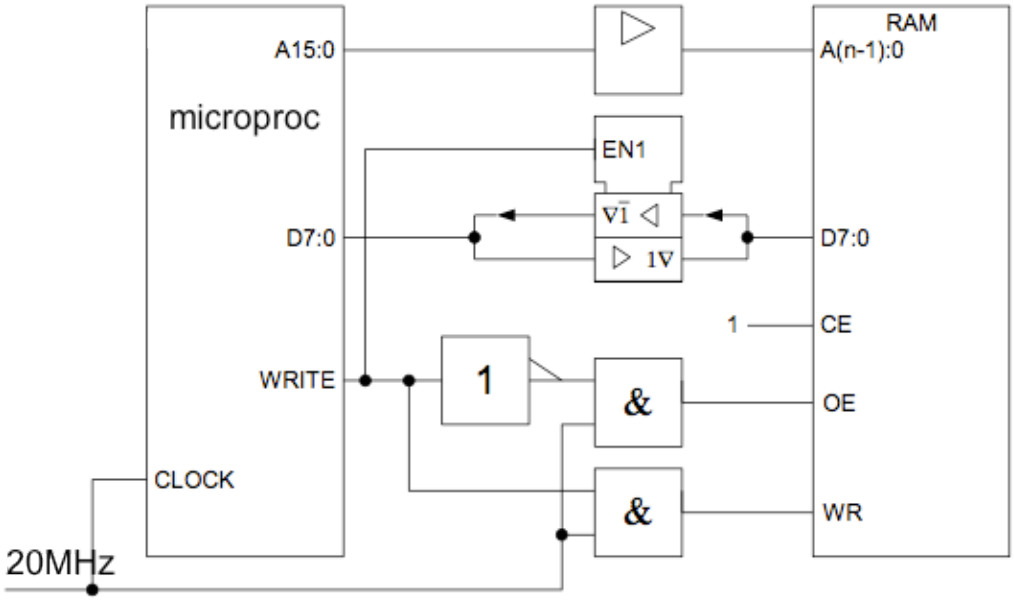
c) Say what is unusual about the byte ordering within the ROM.

3B. The diagram shows an 8-bit microprocessor connected to a memory circuit together with the timing diagram for a microprocessor read cycle..



Each logic gate has a propagation delay that may vary independently in the range 1 to 2 ns. Calculate the maximum permissible access times of the memory from (a) its address inputs, and (b) its OE input.

4C. The circuit of question 3B is altered by the introduction of buffers in the address lines and bi-directional buffers in the data lines.



The address line buffers have a propagation delay of <1 ns while the data line buffers have a propagation delay of <2 ns, an enable time of <1 ns and a disable time of <2ns. The enable time applies when an output changes from a high impedance state to a driven state, the disable time applies when an output changes from a driven state to a high impedance state.

Calculate the new values of the maximum permissible access times of the memory from (a) its address inputs, and (b) its OE input.

5A. Explain why a bi-directional buffer is normally designed to have a longer enable time than disable time.

6D. Buffers for address and data lines can be made faster if they have inverted outputs. Say how the operation of a microprocessor is affected if the address and data lines pass through inverting buffers between the microprocessor and (a) read-write RAM memory and (b) read-only ROM memory.