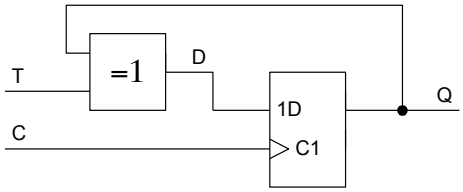
E2.1 – Digital Electronics II

Solution to Problem Sheet 4

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1B. As seen in problem sheet 1, an XOR gate can be used to invert a signal or pass it through unchanged according to whether a control input is high or low.



2C. We define t=0 as the falling edge of CA.

Setup requirement: $\max(DB\uparrow\downarrow)+12 < \min(CB\uparrow)$
$50+22+12 < (13 + \frac{1}{2}T)$
$\frac{1}{2}T > 71 \Rightarrow f < 7$ MHz

Hold requirement: $\max(CB\uparrow) + 27 > \min(T + DB\uparrow\downarrow)$
$\frac{1}{2}T+22 + 27 > T + 5+13$
$\frac{1}{2}T > 31$ (less severe restriction than above)

Note the extra T term in the hold requirement: this is because we want the *second* transition of DB to occur >27 ns after CB↑. The Hold requirement is so easily satisfied that it wouldn't normally be necessary to calculate it exactly.

3C.

µPA → flipflop CA↓=0	Setup:	$\max(DA\uparrow\downarrow)+5 < \min(CA\uparrow)$ $50+5 < \frac{1}{2}T$ $\frac{1}{2}T > 55 \Rightarrow$ **f < 9 MHz**	Hold:	$\max(CA\uparrow)+3 < \min(T+DA\uparrow\downarrow)$ $\frac{1}{2}T+3 < T + 5$ $\frac{1}{2}T > -2$ ☑
flipflop → flipflop CA↑=0	Setup:	$\max(DB\uparrow\downarrow)+5 < \min(CB\downarrow)$ $10+22+5 < \frac{1}{2}T+13$ $\frac{1}{2}T > 24 \Rightarrow f < 21$ MHz	Hold:	$\max(CB\downarrow)+3 < \min(T+DB\uparrow\downarrow)$ $\frac{1}{2}T+22+3 < T +2+13$ $\frac{1}{2}T > 10 \Rightarrow f < 50$ MHz
flipflop → µPB CB↓=0	Setup:	$\max(FB\uparrow\downarrow)+12 < \min(CB\uparrow)$ $10+12 < \frac{1}{2}T$ $\frac{1}{2}T > 22 \Rightarrow f < 23$ MHz	Hold:	$\max(CB\uparrow)+27 < \min(T +FB\uparrow\downarrow)$ $\frac{1}{2}T+27 < T + 2$ $\frac{1}{2}T > 25 \Rightarrow f < 20$ MHz

It can be seen that the critical figure is the setup time for the first flipflop: this is because the microprocessor takes such a long time (up to 50 ns) to output its data.

Question 4 (which doesn't work) and question 5 (which does) show how to relax this constraint. In the third row of the previous table, I have cancelled out the delay of the clock line driver/receiver from the two sides of the inequality. This is only valid if we can assume that the propagation delays for rising and falling edges are the same (not generally true).

4C. The first flipflop now responds to a falling clock edge: this means that µPA now has a full clock cycle to output its data rather than only a half cycle. We have therefore doubled maximum clock frequency of the circuit. (Note that the middle row of this table is unchanged from the previous question).

The problem is that the output from the second flipflop now changes on the rising clock edge and therefore fails to meet the hold time of µPB.

µPA → flipflop CA↓=0	Setup:	max(DA↑↓)+5<min(T+CA↓) 50+5<T T > 55 ⇒ **f < 18 MHz**	Hold:	max(CA↓)+3<min(DA↑↓) 0+3<5 ☑
flipflop → flipflop CA↓=0	Setup:	max(DC↑↓)+5<min(CB↑) 10+22+5 < ½T+13 ½T > 24 ⇒ f < 21 MHz	Hold:	max(CB↑)+3<min(T+DC↑↓) ½T+22+3<T + 2+13 ½T > 10 ⇒ f < 50 MHz
flipflop → µPB CB↑=0	Setup:	max(DD↑↓)+12<min(T+CB↑) 10+12<T T > 22 ⇒ f < 46 MHz	Hold:	max(CB↑)+27<min(DD↑↓) **2 > 27** ☒

5D. We can fix the hold problem by adding a third flipflop. The last row of the previous table is now replaced by the two rows below and the maximum frequency is now 18 MHz.

flipflop → flipflop CB↑=0	Setup:	max(DD↑↓)+5<min(CB↓) 10+5<½T ½T > 15 ⇒ f < 33 MHz	Hold:	max(CB↓)+3<min(T+DD↑↓) ½T+3<T + 2 ½T > 1 ⇒ f < 500 MHz
flipflop → µPB CB↓=0	Setup:	max(DE↑↓)+12<min(CB↑) 10+12<½T ½T > 22 ⇒ f < 23 MHz	Hold:	max(CB↑)+27<min(T+DE↑↓) ½T+27<T + 2 ½T > 25 ⇒ f < 20 MHz

The timing of this circuit with a clock period of about 60 ns (16.7 MHz) is shown below with setup/hold windows shaded: