E2.1 – Digital Electronics II2

Solution to Problem Sheet 6

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

1A. Two reasons. Firstly many memories, though not all, use the same pins for data input as for data output: the outputs must therefore be turned off (or "tristated") to allow new data to be written into a memory location. Secondly, a large memory system contains several memory integrated circuits which are enabled one at a time according to the address range selected. The use of tri-state outputs allows all memory data lines to be connected together without the need for an external multiplexer to switch between them.

2B. a) RAM has 13 address inputs, ROM has 14, Serial Port has 3 and Parallel Port has 1.

b) We need 5 RAM chips and one ROM, serial and parallel chips. The CE inputs are given in the following table:

Chip	Address Range	CE
RAM	0000 – 1FFF	$\overline{A15}\cdot\overline{A14}\cdot\overline{A13}$
	2000 – 3FFF	$\overline{A15}\cdot\overline{A14}\cdot A13$
	4000 – 5FFF	$\overline{A15}\cdot A14\cdot\overline{A13}$
	6000 – 7FFF	$\overline{A15}\cdot A14\cdot A13$
	8000 – 9FFF	$A15\cdot\overline{A14}\cdot\overline{A13}$
ROM	A000 – DFFF	$A15\cdot\left(\overline{A14}\cdot A13 + A14\cdot\overline{A13}\right)$
Serial	E100 – E107	$A15\cdot A14\cdot A13\cdot A8$
Parallel	E200 – E201	$A15\cdot A14\cdot A13\cdot A9$

Note that I have not included all the address lines needed to fully decode the Serial and Parallel port adress ranges. The microprocessor should never access the undefined memory locations in the range E000 to FFFF so it does not matter if the peripheral ports respond to several of them. As defined above, the following addresses will all refer to the serial port's lowest location: E100, E108, E110, E118, …, FFF8. Of the 16 address lines, 3 are direct inputs to the serial port, 4 are used in forming its CE and 9 are unused. The 9 unused lines can take on 512 possible values and so the serial port will appear 512 times in the memory map. If a PAL is being used to generate the CE signals, then the number of PAL inputs required may be reduced by not decoding peripheral address ranges fully.

c) The bytes are in the wrong order in the ROM. The ROM has 14 address inputs, namely A13:0. Addresses A000 to BFFF have A13=1 and will therefore be mapped to the second half of the ROM; addresses C000 to DFFF have A13=0 and will be mapped to the first half of the ROM. This situation could be corrected by inverting A13 before connecting it to the ROM but this would add delay: a neater solution is to use A14 as the most significant address bit rather than A13.

3B. Note that only the setup time matters for this question. Let A be the access time (or propagation delay) from the address inputs and E be the access time from the OE input. The clock period is 50 ns. P is the propagation delay of a gate (i.e. 1 to 2 ns)

$$\max(7+A)+3 < 50 \Rightarrow \underline{\mathbf{A < 40\ ns}}$$

$$\max(P+E)+3 < 25 \Rightarrow \underline{\mathbf{E < 20\ ns}} \text{ (taking P=2, its maximum value)}$$

4C. We now have three possible paths to consider:

A15:0→Mem→D7:0 max(7+1+A+2)+3<50 ⇒ **A < 37 ns**
CLOCK↑→Mem:OE→D7:0 max(P+E+2)+3<25 ⇒ **E < 18 ns**
WRITE→Buff:EN1→D7:0 max(7+2)+3<50 ⇒ **12 > 50** ☑

Note that in the symbol for the bidirectional buffer: the ∇ denotes tristate outputs: the output marked with a 1 is enabled when EN1 is high while the output marked with a $\bar{1}$ is enabled when EN1 is low. The ∇ always goes immediately next to the output pin. The symbol ▷ denotes a buffer: a gate with a higher than normal output current capability. Any signals that flow right to left instead of the more normal left to right must be marked with a ←.

5A. If the same wire is driven high by the output of one device and low by that of another, a high current will flow which will waste power and which may even damage the integrated circuits involved. To reduce the possibility of two devices trying to drive the same wire simultaneously, tristate outputs are almost always designed to turn off more quickly than they turn on.

6D. The effect of inverting the address lines is to subtract them from FFFF. Thus what were memory locations 0000, 0001 and 0002 now become FFFF, FFFE and FFFD. Providing the chip enables are generated correctly, this reversal does not matter at all for a RAM: as long as each distinct address refers to a unique memory location the microprocessor does not care where it is inside the chip. For a ROM, the contents must be pre-programmed in the correct locations: thus the program would need to be stored backwards.