§3 – Digital Systems Implementation
Programmable Logic Devices

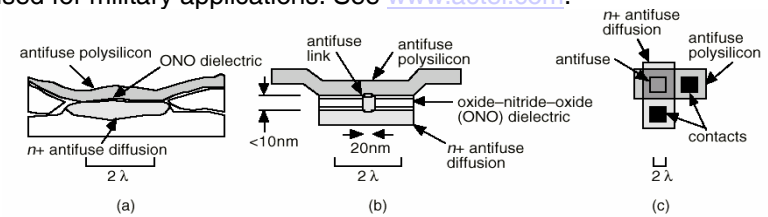
- Why Programmable Logic Devices (PLDs)?
  - Low cost, low risk way of implementing digital circuits as application specific ICs (ASICs).
  - Technology of choice for low to medium volume products (say hundreds to few 10's of thousands per year).
  - Good and low cost design software.
  - Latest high density devices are over 1 million gates!

Basic FPGA Architectures

- All FPGAs have the following key elements:
  - The Programming technology
  - The basic logic cells
  - The I/O logic cells
  - Programmable interconnect
  - Software to design and program the FPGA
- Currently the four main players in this field are:-
  - Actel
  - **Altera**
  - **Xilinx**
  - Atmel

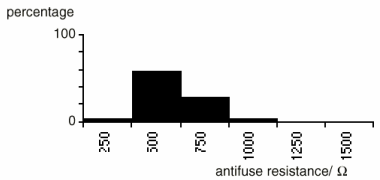
PLD Technologies: Antifuse

- Invented at Stanford and developed by Actel. Currently mainly used for military applications. See www.actel.com.



Number of antifuses on Actel FPGAs

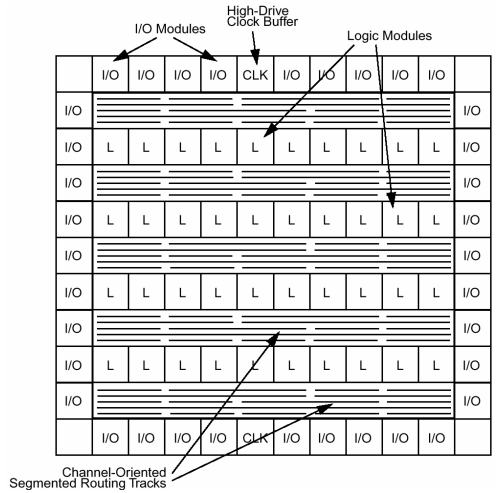
Device	Antifuses
A1010	112,000
A1020	186,000
A1225	250,000
A1240	400,000
A1280	750,000



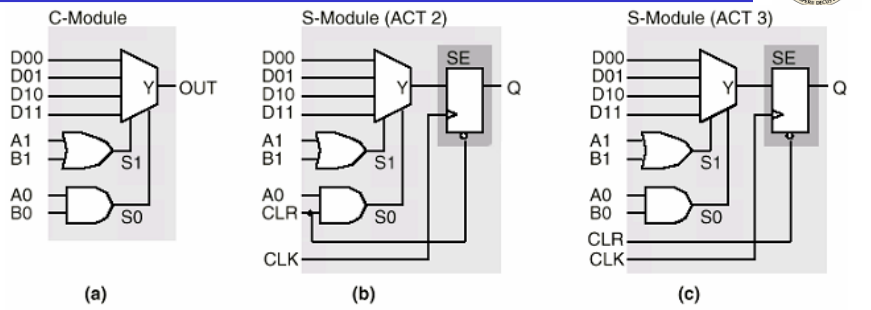
The resistance of blown Actel antifuses

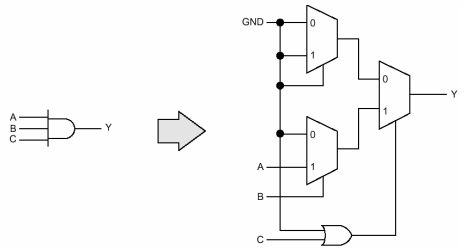
Actel FPGAs

- Uses antifuse technology
- Based on **channelled gate array** architecture as shown below
- Each logic element (labelled 'L') is a combination of multiplexers which can be configured as a multi-input gate



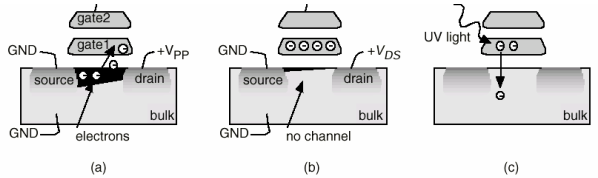
Actel Logic Element





PLD Technologies: EPROM & EEPROM

- Generally used in product-term type of PLDs.
- Non-volatile and reprogrammable.
- Good for FSM, less good for arithmetic circuits.



An EPROM transistor

(a) With a high (>12V) programming voltage, V_{PP}, applied to the drain, electrons gain enough energy to "jump" onto the floating gate (gate1)

(b) Electrons stuck on gate1 raise the threshold voltage so that the transistor is always for normal operating voltages

(c) UV light provides enough energy for the electrons stuck on gate1 to "jump" back to t bulk, allowing the transistor to operate normally

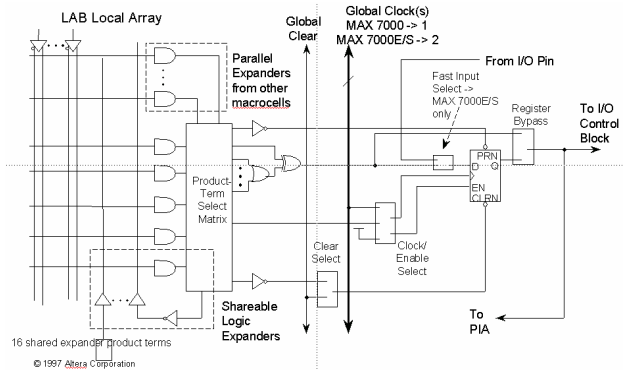
Facts and keywords: Altera MAX 5000 EPLDs and Xilinx EPLDs both use UV-erasable electrically programmable read-only memory (EPROM) • hot-electron injection or avalar injection • floating-gate avalanche MOS (FAMOS)

Altera MAX CPLDs

- CPLD = Complex Programmable Logic Devices
- FPGA = Field Programming Gate Arrays
- Altera has four different PLD families:
  - MAX family – product-term based macrocells CPLDs
  - FLEX family – SRAM based lookup tables (LUTs)
  - APEX family – mixture of product-term and LUT based devices
  - Stratix family – Advanced FPGAs with embedded blocks (Stratix-2 is currently the most advanced FPGA devices)

MAX7000 Logic Element

- **macrocell** implements a Boolean expression in the form of **sum-of-product (SOP)**.
- An example of such a sum-of-product is: a•!b•c•!d + a•c•e + !a•f
- Each product term could have many input variables ANDed together. A SOP could have a number of product terms ORed together.
- Each macrocell also contains a flip-flop – essential for implementing FSM.

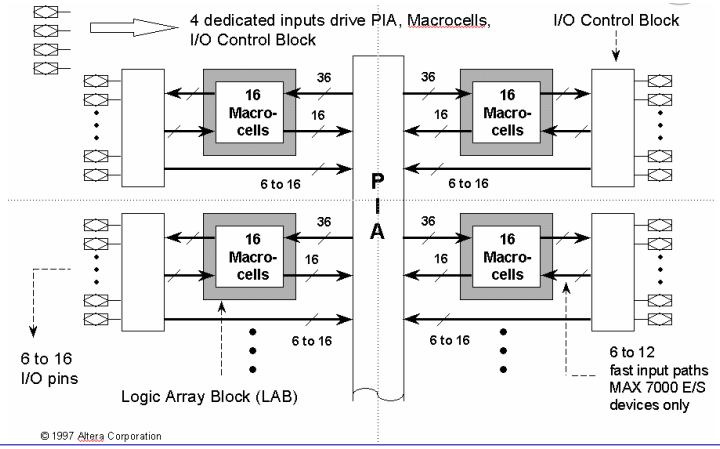


MAX7000 Logic Element

- Each horizontal line represent a product term.
- Inputs are presented to the product term as signal and its inverse.
- Each macrocell can normal OR 4 product terms together.
- Each LAB share an additional 16 shared product terms in order to cope with more complex Boolean equations.
- Output XOR gate allows either efficient implementation of XOR function or programmable logic inversion.
- The SOP output can drive the output directly or can be passed through a register.
- This architecture is particularly good for implementing finite state machine.
- Each register can store one state variable. This can be fed back to the logic array via the Programmable Interconnect Array (PIA).
- This is not efficient for adder or multiplier circuits or as buffer storage (such as register file or FIFO buffers) – waste the potential of the logic array.

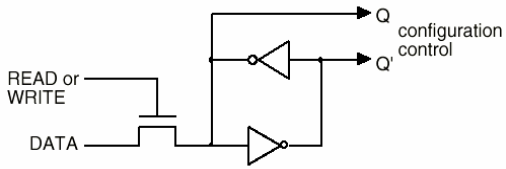
MAX7000 LABs

- Consists of Logic Array Blocks (LABs), each with 16 macro-cells
- PIA = Programmable Interconnect Array



PLD Technologies: Static RAM

- Almost all **Field Programmable Gate Arrays** (FPGAs) are based on static RAMs.
- Static RAM cells are used for three purposes:
  - As lookup tables (LUTs) for implementing logic (as truth-table).
  - As embedded block RAM blocks (for buffer storage etc.).
  - As control to routing and configuration switches.
- ***Advantages:***
  - Easily changeable (even dynamic reconfiguration)
  - Good density
  - Track latest SRAM technology (moving even faster than technology for logic)
  - Flexible – no only good for FSM, also good for arithmetic circuits
- ***Disadvantages:***
  - Volatile
  - Generally high power

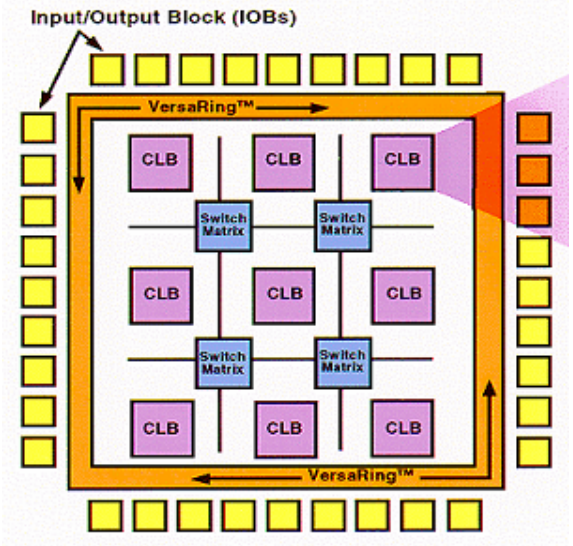


Xilinx FPGAs

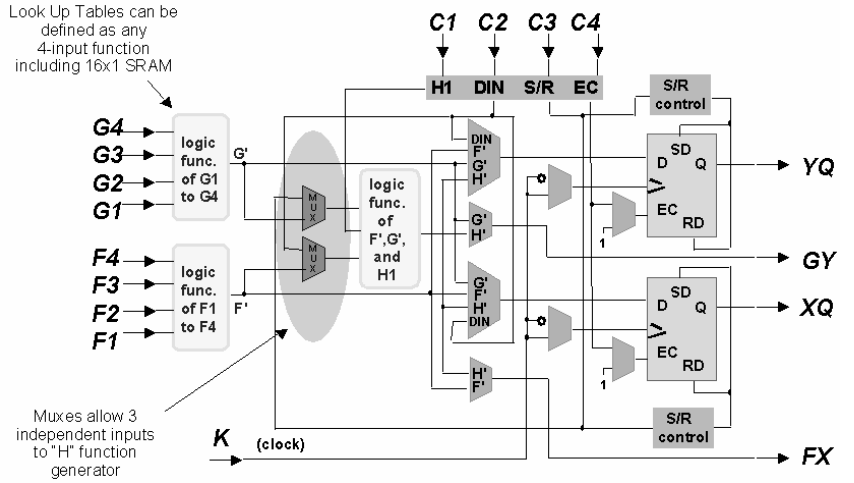
- Start with XC4000
- Virtex Family
- Virtex-II Family
- Virtex-II PRO (We use this for your coursework)
- Virtex-4 Families

Xilinx FPGA (XC4000)

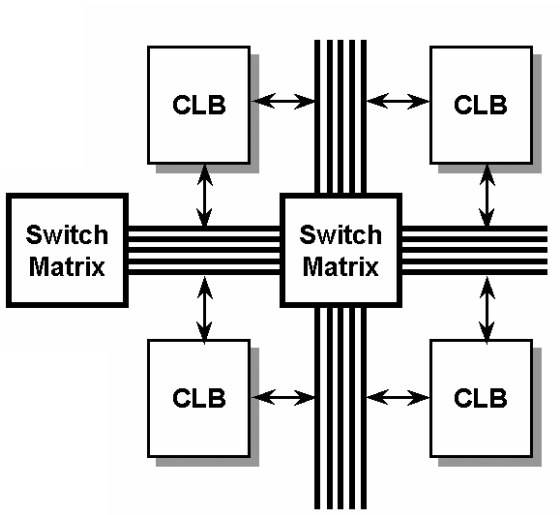
- Xilinx – first to introduce SRAM based FPGA using **Lookup Tables** (LUTs)
- Xilinx 4000 series contains four main building blocks:
- **Configurable Logic Block** (CLB)
- Switch Matrix
- VersaRing
- Input/Output Block



Xilinx FPGA (XC4000)



Xilinx FPGA Switch Matrix Routing

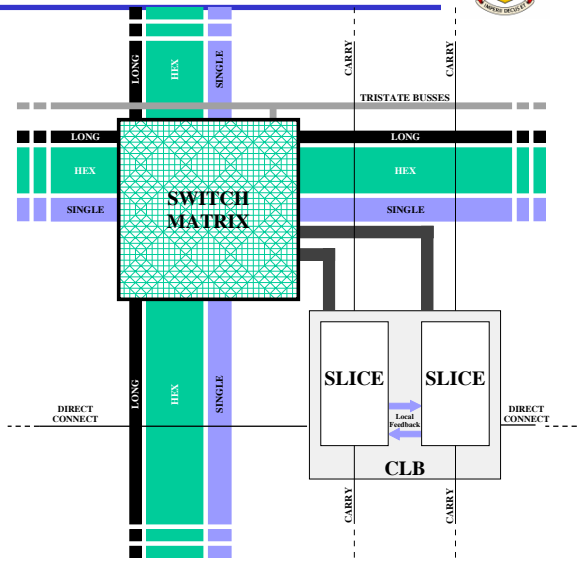


Xilinx FPGA (XC4000)

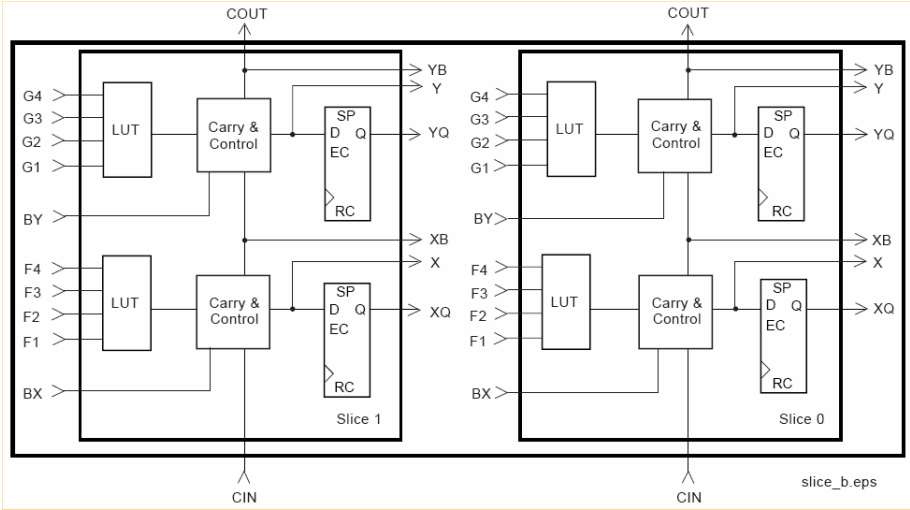
- Each CLB has two 4-input **Lookup Tables** (LUTs) and two reigsters.
- The two LUTs implement two independent logic functions F and G.
- The outputs F' and G' from the two LUTs inside each CLB can be combined to form a more complex function H.
- CLBs are linked together to form **carry** and **cascade chain** circuits (not shown in diagram)
- For the 4000E familiess, each CLB can be configured as synchronous RAM. Write address, data, and control are synchronized to write clock. This is called **distributed RAM**.
- Possible configurations are:
  - Two independent 16 x 1 RAMS
  - One 32 x 1 or 16 x 2 RAM
  - One 16 x 1 dual-port RAM (second port is read-only)

Xilinx new families: Virtex-2 CLB

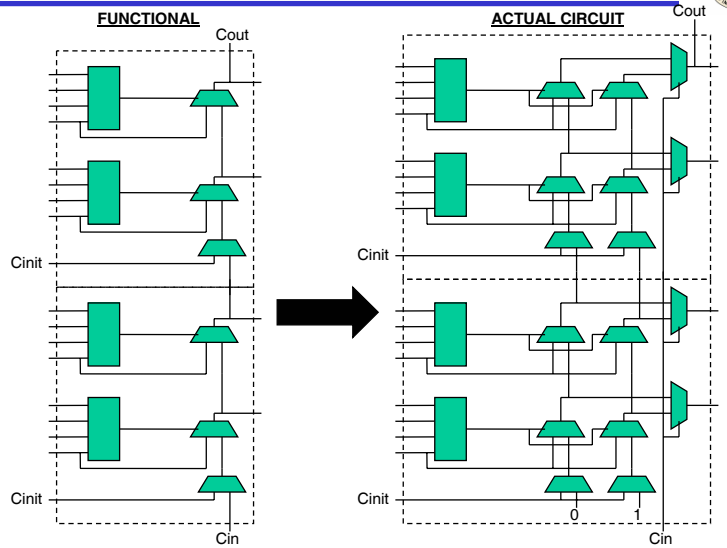
- All CLB inputs have access to interconnect on all four sides
- Two identical slices in each CLB
- Slices have bit pitch of 2
- Fast local feedback within CLB
- Direct connects to adjacent horizontal CLBs



Virtex Slice Model

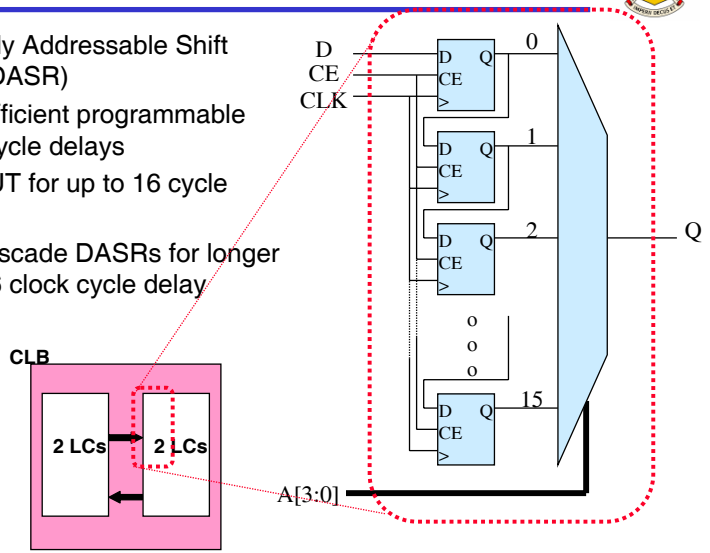


Virtex Carry Select

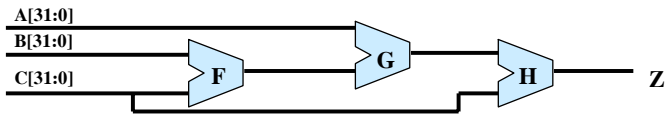


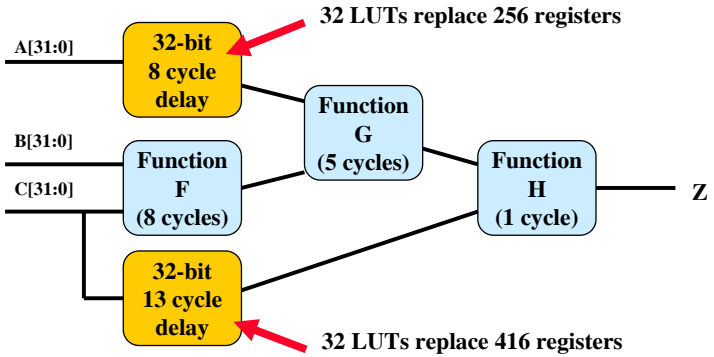
Virtex LUT as Pipeline Delay

- Dynamically Addressable Shift Register (DASR)
  - Ultra-efficient programmable clock cycle delays
  - One LUT for up to 16 cycle delay
  - Can cascade DASRs for longer than 16 clock cycle delay

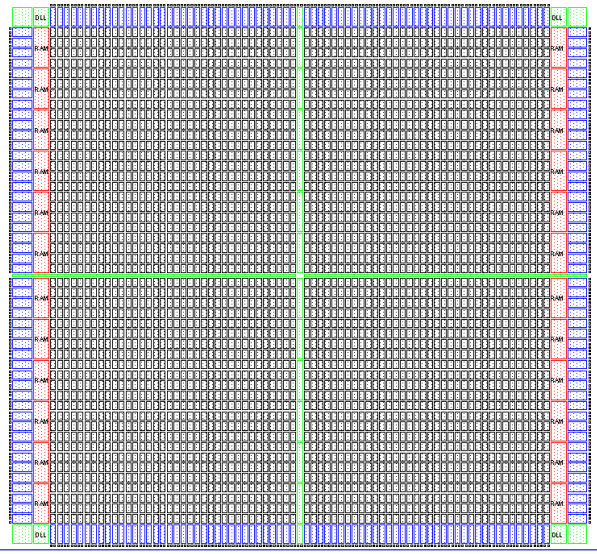


SelectShift Replaces Register Files



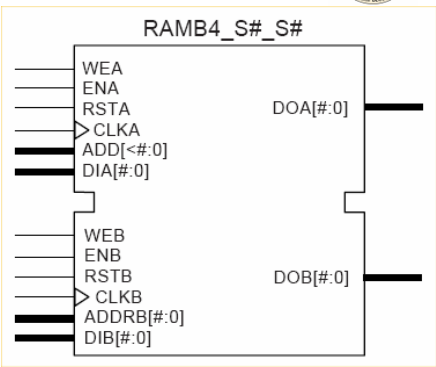


XCV600 (48x72) with Block RAMs



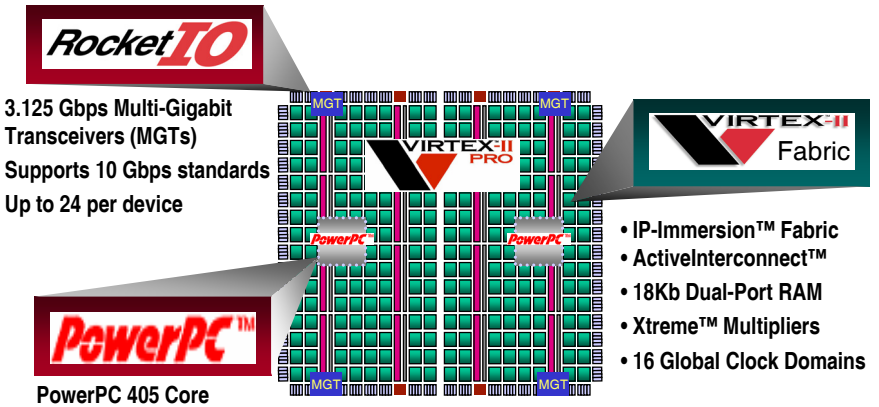
Virtex Block SelectRAM

- 2 Columns of Blocks on left and right
- 1 Block per 4 CLB rows.
- 4K bits of data
- Full Synchronous operation
  - No Asynchronous Read
- Ports can be configured to different widths
- Synchronous reset for Finite State Machine



ADDR	DATA	#/Width	Depth
(11:0)	(0:0)	1	4096
(10:0)	(1:0)	2	2048
(9:0)	(3:0)	4	1024
(8:0)	(7:0)	8	512
(7:0)	(15:0)	16	256

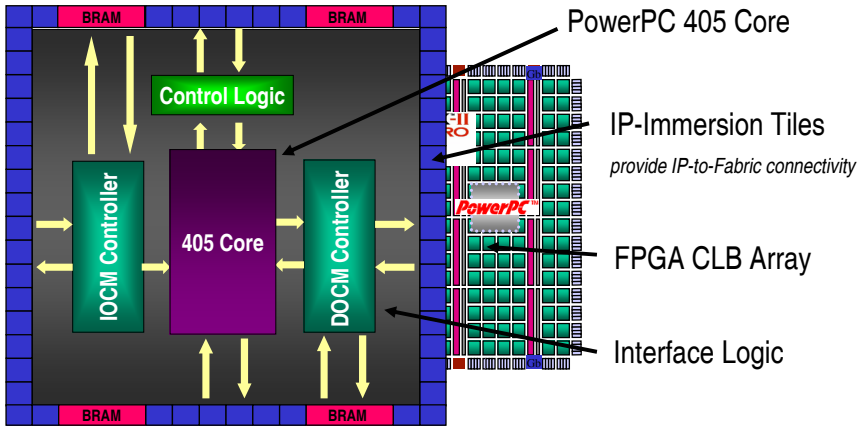
Virtex-II Pro Platform FPGA



Virtex-II PRO - Platform FPGA Technology

- Leading edge 130nm process technology
- Ultra-high performance 92nm gate length Transistors
- 1.5V Core
- 9 Metal layers - All Copper technology

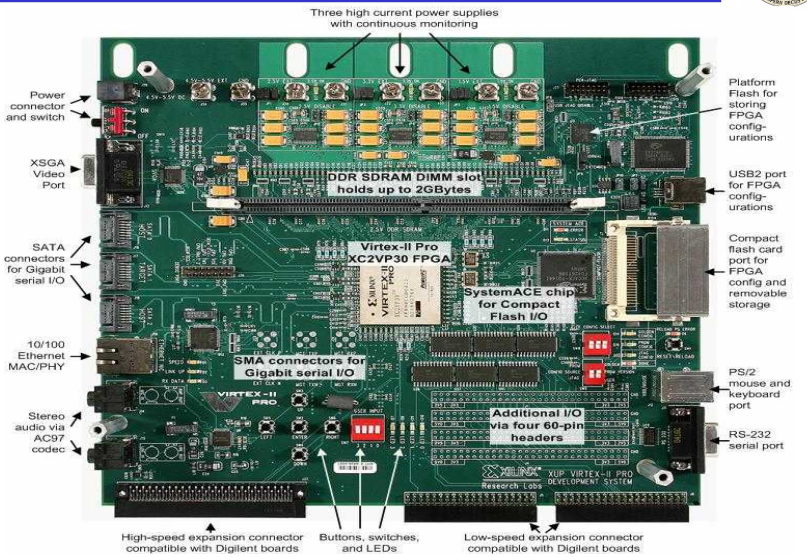
Processor Integration Technology



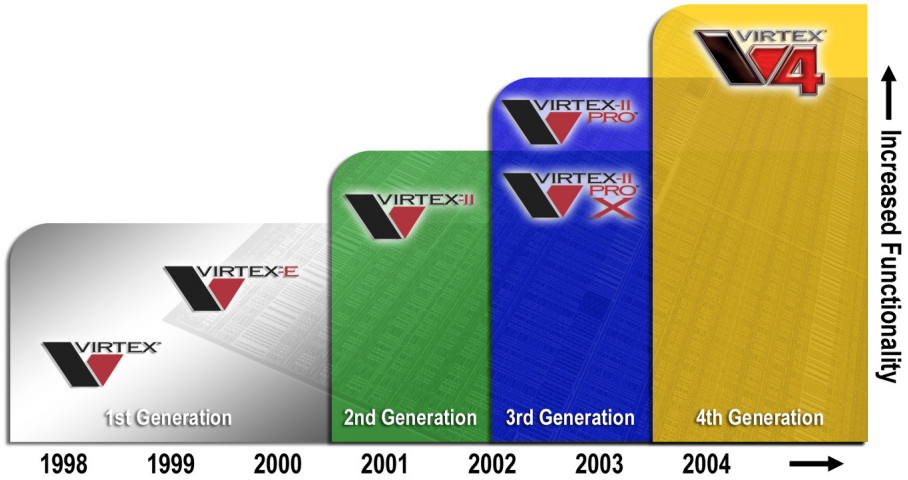
Virtex-II Pro & MicroBlaze

- RISC
  - 32-bit ALU, 32-bit data bus, 32-bit instruction word, 32 x 32 General Purpose Register file
- Harvard architecture (i.e. separate program and data memory space)
- 3 stage pipeline (IF, OF, EX)
- Proprietary instruction set has been created for MicroBlaze.

Virtex-2 PRO Board for coursework

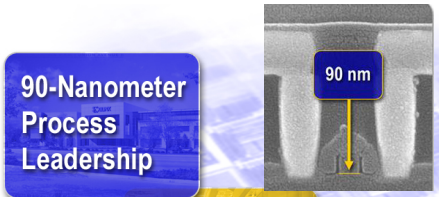


4th Generation Virtex – V4



Advanced 90nm Process Technology

- **Advanced 90-nm Process**
- **11-Layer Copper Metallization**
- **New Triple-Oxide Technology**
  - Enables Lower Quiescent Power Consumption
- **Exclusive Benefits:**
  - Best Cost
  - Greatest Performance
  - Lowest Power
  - Highest Density



90-Nanometer Process Leadership

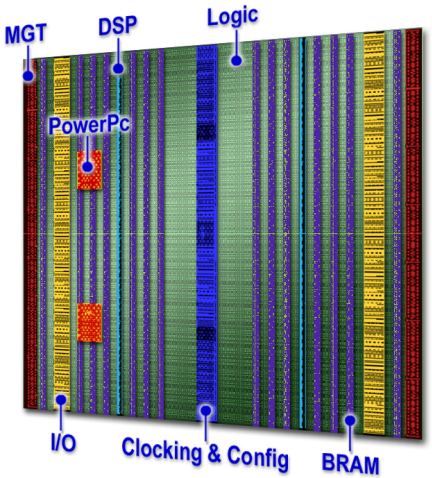
World Class Fab Partners

Shipping 90-Nanometer Today

Enables 2x Performance, 2x Capacity, ½ Power, ½ Cost

New ASMBL™ Columnar Architecture

- **Revolutionary Advance in FPGA Architecture**
- **Enables "Dial-In" Resource Allocation Mix**
  - Logic, DSP, BRAM, I/O, MGT, DCM, PowerPC
- **Enabled by Flip-Chip Packaging Technology**
  - I/O Columns Distributed Throughout the Device



Three Virtex-4 Platforms

Resource	LX	FX	SX
Logic	14K-200K LCs	12K-140K LCs	23K-55K LCs
Memory	0.9-6Mb	0.6-10Mb	2.3-5.7Mb
DCMs	4-12	4-20	4-8
DSP Slices	32-96	32-192	128-512
SelectIO	240-960	240-896	320-640
RocketIO	N/A	0-24 Channels	N/A
PowerPC	N/A	1 or 2 Cores	N/A
Ethernet MAC	N/A	2 or 4 Cores	N/A
System Monitor	0-1+ADC	0-1+ADC	0-1+ADC

Choose the Platform that Best Fits the Application