§8 – JTAG Boundary Scan

JTAG (IEEE 1149.1/P1149.4) Tutorial
Introductory

Based on TI Test Symposium (1997)

Background

Standard Approach To Test

- Developed by Joint Test Action Group (over 200 SC, test, and system vendors) starting in mid ’80s
- Sanctioned by IEEE as Std 1149.1 Test Access Port and Boundary-Scan Architecture in 1990
- Solution: Build test facilities/test points into chips
- Focus: Ensure compatibility between all compliant ICs

Standard Test Access Port (TAP)

- 4/5-Wire Interface at Chip-Level
- Serial Instruction/Serial Data Port
- Extensible to Include
  - user-defined instructions
  - user-defined data registers

Basic Boundary-Scan Architecture

- Scan effectively partitions digital logic to facilitate control and observation of its function
- Chip-Internal Scan: Partitions chips at storage cells (latches/ flip-flops) to effectively partition sequential logic into clusters of combinational logic
- Boundary-Scan: Partitions boards at chip I/Os for control and observation of board-level nodes
Why is JTAG necessary?

- Miniaturization results in loss of test access

Ever-Expanding Chip

- Increasing integration at chip level complicates controllability

Can't Afford Not To Test

Cost will increase by a factor of ten as fault finding moves from one level of complexity to the next. The result:

- Reduced Profit Margins
- Delayed Product Introduction
- Dissatisfied Customers

1. Device level 1 unit of cost
2. Board level 10 units of cost
3. System level 100 units of cost
4. Field level 1,000 units of cost

Conventional Methods of Board Test (in 90's)

Functional Test ('Edge-Connector' Test)

- Based on board function, rather than structure
- Test generation primarily manual
- Test access limited to primary I/O only
Conventional Methods of Board Test (in 90’s)

**In-Circuit Test**

*‘Bed-of-Nails’ Test*

- Based on board structure, but limited by chip complexity
- Expensive testers and fixtures required
- Test access limited by:
  - Fine pitch packages
  - Double-sided boards
  - Conformal coating
  - MCMs

The **Boundary Scan Idea**

- ‘In-Circuit’ test points moved onto the silicon, creating ‘Virtual Nails’
- Boundary scan cells bound each net, providing for continuity testing
- Observe/Control cells provide for test and normal function

The **Boundary Scan Idea**

- Scan provides a means to arbitrarily observe test results and source test stimulus
- Scan method requires minimal on chip/board resources (pins/nets)

Boundary Scan for Board Test

- Based on board structure; Not limited by chip function/complexity
- Test access is not limited by board physical factors
Boundary Scan for Board Test (con’t)

- Chip function need not be considered for board test (shorted/open nets)
- Test generation is highly automated; Simple ‘In-Circuit Library’ models (BSDL) are vendor-supplied or EDA-generated

Boundary Scan Cell

The Control Architecture

- Boundary scan and other test data registers operate under control of instruction register
- Data is scanned from TDI to TDO through selected test data register or instruction register under control of Test Access Port (TAP) controller
- TAP operates synchronously to TCK using TMS for state selection

The Test Logic Architecture

- The REQUIRED elements of the test logic architecture are:
  - Test Access Port (TAP)
  - TAP Controller
  - One Instruction Register
  - A Set of Data Registers
- All such elements are REQUIRED to be dedicated test logic (not used for any other purpose) with the exception of user-defined data registers
### The Test Access Port

- 4 wire TAP interface **REQUIRED**
- Either power-up reset or 5th wire, TRST*, is **REQUIRED**
- All TAP pins are **REQUIRED** to be dedicated (not used for any other purpose)
- Pullups **REQUIRED** at TDI and TMS (also, TRST*, if implemented)
- All inputs (e.g., TDI) are **REQUIRED** to be sampled on TCK rising; all outputs (e.g., TDO) are **REQUIRED** to be propagated on TCK falling.

### The TAP Controller

- The TAP controller is **REQUIRED** to conform exactly to this state diagram.
- The instruction scan sequence is **REQUIRED** to access only the single instruction register.
- The data scan sequence is **REQUIRED** to access only the data register selected by the current instruction.
- TDO is **REQUIRED** to be active only in the Shift-IR and Shift-DR states.

### The TAP Controller Outputs

- IR scan and update clocks and shift/capture select
- DR scan and update clocks and shift/capture select
- TDO edge and TDO instruction/data select

### Register Summary

<table>
<thead>
<tr>
<th>Register</th>
<th>Length</th>
<th>Capture Value</th>
<th>Selected by Instruction(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INSTRUCTION</td>
<td>at least two</td>
<td>X..01</td>
<td>n/a</td>
</tr>
<tr>
<td>BOUNDARY</td>
<td>user-specified</td>
<td>user-specified</td>
<td>Exttest Sample/Preload Inttest Clamp HighZ</td>
</tr>
<tr>
<td>BYPASS</td>
<td>exactly one</td>
<td>0</td>
<td>Bypass</td>
</tr>
<tr>
<td>Device ID</td>
<td>exactly 32</td>
<td>X..1</td>
<td>Idcode Usercode</td>
</tr>
<tr>
<td>User-defined</td>
<td>user-specified</td>
<td>user-specified</td>
<td>user-specified</td>
</tr>
</tbody>
</table>
The Instruction Register

- The instruction register is **REQUIRED** to be at least 2 bits in length.
- The instruction register is **REQUIRED** to capture the binary value 01 in its 2 least-significant bits on the rising edge of TCK in Capture-IR (other bits may capture user-specified data).
- The instruction register is **REQUIRED** to have a latched parallel output such that a new instruction only takes effect after shifting is complete (on falling edge of TCK in Update-IR).
- The instruction register is **REQUIRED** to reset to fidcode (if implemented), otherwise to Bypass.

The Test Data Registers

- Only 2 test data registers are **REQUIRED**:
  - The boundary-scan register - the serial concatenation of all boundary-scan cells, at least one for each digital signal pin
  - The bypass register
- These registers, and the device identification register, if implemented, are **REQUIRED** to be dedicated test logic (used for no other purpose).

The Boundary-Scan Register

- The boundary-scan register is **REQUIRED** to be a concatenation of all boundary-scan cells:
  - it is **REQUIRED** that there be at least one BSC for each digital input or output to the system logic (including on-chip outputs to analog circuitry)
  - it is **REQUIRED** that there NOT be BSCs at
    » TAP pins
    » compliance enables
    » non-digital signals

The Bypass Register

- The bypass register is **REQUIRED** to be one bit in length.
- The bypass register is **REQUIRED** to capture a logic 0 value in Capture-DR state.
- It is **REQUIRED** that any operation of the bypass register have no effect on the operation of the system logic.
Instruction Summary

<table>
<thead>
<tr>
<th>Instruction (REQUIRED/Optional)</th>
<th>Opcode</th>
<th>Mode</th>
<th>Selected Data Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST</td>
<td>0.0°</td>
<td>Test</td>
<td>Boundary</td>
</tr>
<tr>
<td>SAMPLE/PRELOAD</td>
<td>user-specified</td>
<td>Normal</td>
<td>Boundary</td>
</tr>
<tr>
<td>BYPASS</td>
<td>1.1</td>
<td>Normal</td>
<td>Bypass</td>
</tr>
<tr>
<td>Intest</td>
<td>user-specified</td>
<td>Test</td>
<td>Boundary</td>
</tr>
<tr>
<td>Runtist</td>
<td>user-specified</td>
<td>Test</td>
<td>User-specified</td>
</tr>
<tr>
<td>idcode</td>
<td>user-specified</td>
<td>Normal</td>
<td>Device ID</td>
</tr>
<tr>
<td>Usercode</td>
<td>user-specified</td>
<td>Normal</td>
<td>Device ID</td>
</tr>
<tr>
<td>Clamp</td>
<td>user-specified</td>
<td>Test</td>
<td>Bypass</td>
</tr>
<tr>
<td>HighZ</td>
<td>user-specified</td>
<td>Test</td>
<td>Bypass</td>
</tr>
<tr>
<td>user-defined</td>
<td>user-specified</td>
<td>user-specified</td>
<td>user-specified</td>
</tr>
</tbody>
</table>

- TMS transition in progress will switch the requirement for EXTEST opcode of all zero

The Extest Instruction

- Provides for test external to chip, such as interconnect test
- Output pins operate in test mode, driven from contents of BSC update latch
- Input data captured in BSC scan latches prior to shift operation
- Shift operation allows test response to be observed at TDO while next test stimulus inserted at TDI
- Following shift operation, new test stimulus transferred to BSC update latches

The Sample/Preload Instruction

- Provides means to preload boundary before entry to test mode
- Output and input pins operate in normal mode
- Input pin data and core logic output data captured in BSC scan latches
- Shift operation allows test response to be observed while next test stimulus inserted at TDI
- Following shift operation, new stimulus transferred to BSC update latches

The Bypass Instruction

- Provides for abbreviated scan path through chip
- Output and input pins operate in normal mode
- The one-bit bypass register is selected for scans
- Mandatory that an all-ones value updated into the IR decodes to Bypass, as well as any opcodes which are otherwise undefined
Interconnect Test with JTAG Board

- All nets bound by BSC’s and/or primary I/O requiring no physical access
- Parallel access reduced to card edge only
- Test generation and application fast and easy

Glue Logic Test

- Random-logic cluster is bound by boundary-scannable chips
- Deterministic test stimulus (ATPG-generated) can be driven to cluster from B/S outputs
- Test response can be captured at B/S inputs
- BIST methods (PRPG/PSA) can be used for increased test throughput and near “At-speed” performance

Partial Boundary Scan Board Test

- Not all nets are bound by boundary scan and/or primary I/O, perhaps requiring some ICT access
- Expense and complexity reduced for test generation and test application for chips/boards with B/S access
- Cluster testing may be used to access non-scan nets

Logic Cluster Test
Memory Test

- Memory array bound by boundary scan chips
- Automatic test patterns can be generated and driven from B/S outputs
- Test response can be captured at B/S inputs
- Transceivers can test for net shorts w/o memory R/W
- BIST methods (PRPG/PSA) can be used for increased test throughput

System-Level Test

- TAP-addressable interface unit extends JTAG access beyond board-level
- System-level test
- System design verification
- Sys integration (Mfg test)
- Sys self-test (Field Svc)
- Supports in place board test and board-to-board test
- Allows reuse of device/board test data

JTAG in Real Chips - FPGA

- Scan access to chips, boards, systems for:
  - Design verification/debug
  - Manufacturing test
  - Hardware/software integration
  - Field test/diagnostics
- Access built-in self-test (BIST)
- Access on-chip/in-circuit emulation (ONCE/ICE)
- Access in-system programming (ISP) of PLDs/EPPROMs
- Let your imagination run wild!!!

JTAG in Real Chips - FPGA

- Provides control and observation of system under test without need for physical access
  - Ease of set-up for test
- Can be used in standard system configuration (no need for card extenders, etc.)
- Can be used in environmental chambers
- Can access on-chip emulation for software/debug
- Can access ISP for code download/offload/changes
System Configuration Maintenance

- Provides low-level test access within configured systems for:
  - In-house system integration
  - Fielded-system test and diagnostics
  - Built-in self-test
  - In-field upgradability via ISP, etc.
  - Remote field test, diagnostic and upgrade

IEEE Standard 1149.1

  - The official document which specifies the international standard for a test access port and boundary-scan architecture. Informally known as the JTAG standard, it was officially ratified by the IEEE in February 1990. Since, it has been supplemented twice. The first supplement, ratified in June 1993, is included in the referenced document. The second supplement is currently a separate document, as referenced below.
  - The official document which specifies the international standard for a boundary-scan description language. This supplement to IEEE Std 1149.1-1990 was ratified in September 1994.

References

  - Edited by two principal chairs of the IEEE 1149.1 working group, this Computer Society tutorial compiles several of the seminal papers on boundary-scan along with several invited papers on various topics including applications, implementation, and others. It will primarily be of interest to the design and/or test engineers.
  - Authored by the principal force behind the Boundary-Scan Description Language (BSDL) and an IEEE 1149.1 working group principal as well as a long time manufacturing and design-for-test expert, this is truly considered THE indispensable handbook on boundary scan for the design and/or test engineers.
  - Authored by several JTAG and IEEE 1149.1 working group principals, this book is a ready reference to boundary-scan technology, its benefits, and considerations for design and test managers and engineers.

Abbreviations/Acronyms

- ASC Application-Specific Integrated Circuit
- ASP Addressable Scan Port
- ATE Automatic Test Equipment
- ATPG Automatic Test Pattern Generation
- BST Built-In Self-Test
- B/S Boundary-Scan
- BSC Boundary-Scan Cell
- BSDL Boundary-Scan Description Language
- BSR Boundary-Scan Register
- BST Boundary-Scan Test
- CAGE Computer-Aided Engineering
- DFT Design-for-Test
- DR Data Register
- DSP Digital Signal Processing/Processor
- EDA Electronic Design Automation
- eTBC Embedded Test Bus Controller
- FPGA Field-Programmable Gate Array
- HSDL Hierarchical Scan Description Language
- ICE In-Circuit Emulation
- ICT In-Circuit Test
- IEEE Institute of Electrical & Electronics Engineers IR Instruction Register
- ISP In-System Programming
- JTAG Joint Test Action Group
- MCM Multi-Chip Module
- Mfg Manufacturing
- PCB Printed Circuit Board
- PLD Programmable Logic Device
- PPG Pseudo-Random Pattern Generation
- PSA Parallel Signature Analysis
- PWB Printed Wiring Board
- SPL Scan Paths Linker
- SVF Serial Vector Format
- TAP Test Access Port
- TBC Test Bus Controller
- TCK Test Clock
- TDI Test Data Input
- TDO Test Data Output
- TM Test Mode Select
- TRST Test Reset
- UUT Unit Under Test