Topic 2

Programmable Logic Devices

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Programmable Logic Devices (PLDs)

- Supplied with no user programmable logic functions
- Require specialized computer software for design and programming – good quality and low cost
- Implementation of digital circuits with low cost and low risk
- Technology of choice for low to medium volume products (say hundreds to few 10's of thousands per year)
- Replacing application specific ICs (ASICs) fast!

Who makes PLDs?

XILINX
ALTERA
Actel
Lattice
CYPRESS
Connecting From Last Mile to First Mile.
QUICKLOGIC
ATMEL

PLD Technologies

- Floating Gate/ Flash Programming Technology
- SRAM Programming Technology
- Antifuse Programming Technology

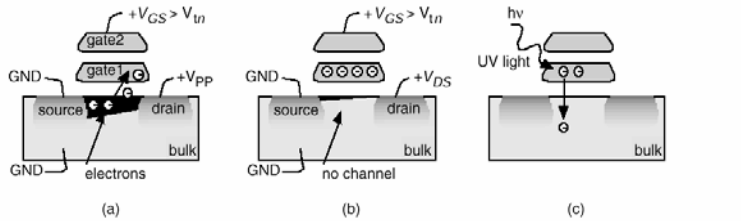
In-System Programming (ISP):
performing the programming while the chip is still attached to its circuit board

JTAG (Boundary Scan):
A port added to FPGAs for testing purposes, as a means of downloading the design in the programmable device via serial port of a PC

Floating Gates / Flash Technology

- Originally used in product-term type PLDs
- Non-volatile and reprogrammable
- Good for FSM and less good for arithmetic
- Now used by **Actel** for non product-term devices

Floating Gates / Flash Technology (2)



An EPROM transistor

(a) With a high (>12V) programming voltage, V_{PP}, applied to the drain, electrons gain enough energy to "jump" onto the floating gate (gate1)

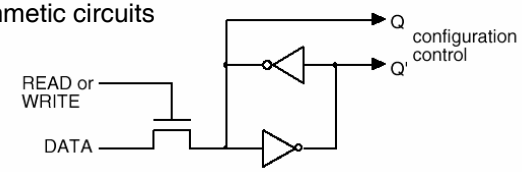
(b) Electrons stuck on gate1 raise the threshold voltage so that the transistor is always off for normal operating voltages

(c) UV light provides enough energy for the electrons stuck on gate1 to "jump" back to the bulk, allowing the transistor to operate normally

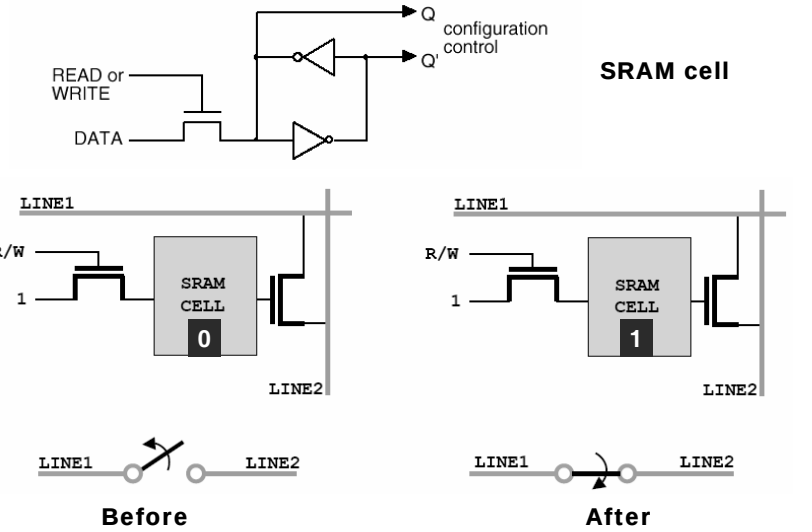
Facts and keywords: Altera MAX 5000 EPLDs and Xilinx EPLDs both use UV-erasable electrically programmable read-only memory (EPROM) • hot-electron injection or avalanche injection • floating-gate avalanche MOS (FAMOS)

SRAM Programming Technology

- Use in all **Field Programmable Gate Arrays** (FPGAs)
- Static RAM cells are used for three purposes:
  - As lookup tables (LUTs) for implementing logic (as truth-table).
  - As embedded block RAM blocks (for buffer storage etc.).
  - As control to routing and configuration switches.
- ***Advantages:***
  - Easily changeable (even dynamic reconfiguration)
  - Good density
  - Track latest SRAM technology (moving faster than logic technology)
  - Flexible –good for FSM & arithmetic circuits
- ***Disadvantages:***
  - Volatile
  - Generally high power

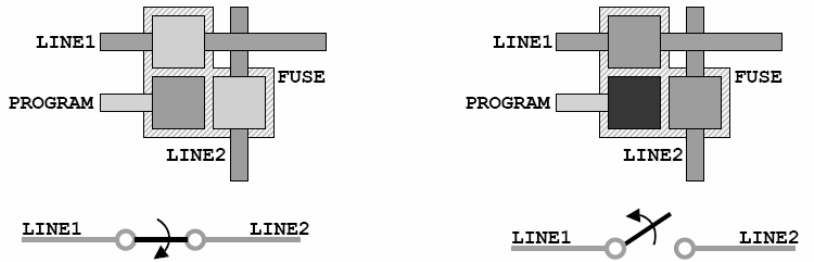


SRAM Programming Technology (2)



Antifuse Programming Technology

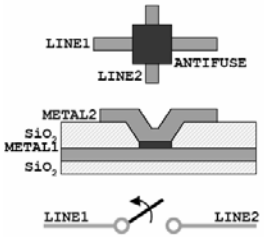
- Invented at Stanford and developed by Actel
- One-time programmable (OTP) only
- Non-volatile and mostly used for defense and space applications
- Normal fuse programming technology:



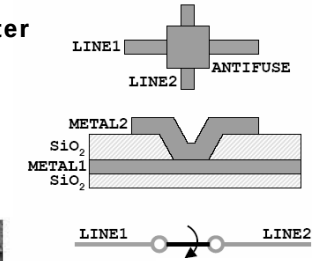
Before **After**

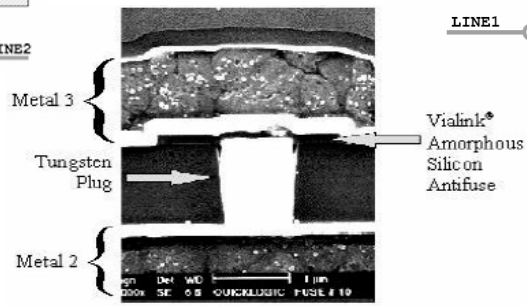
Antifuse Programming Technology (2)

Before



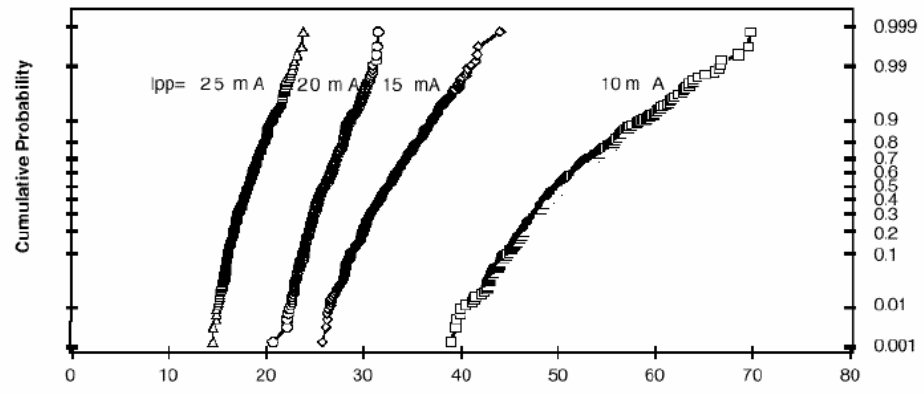
After



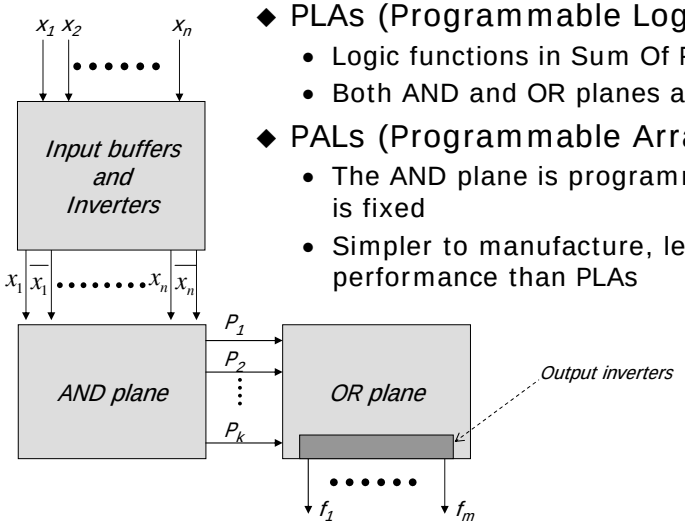


Antifuse Programming Technology (3)

- Typical antifuse resistance after programming: 20 – 100 ohms
- Program at ~10V
- Fuse thickness ~ 500 – 1000 Å

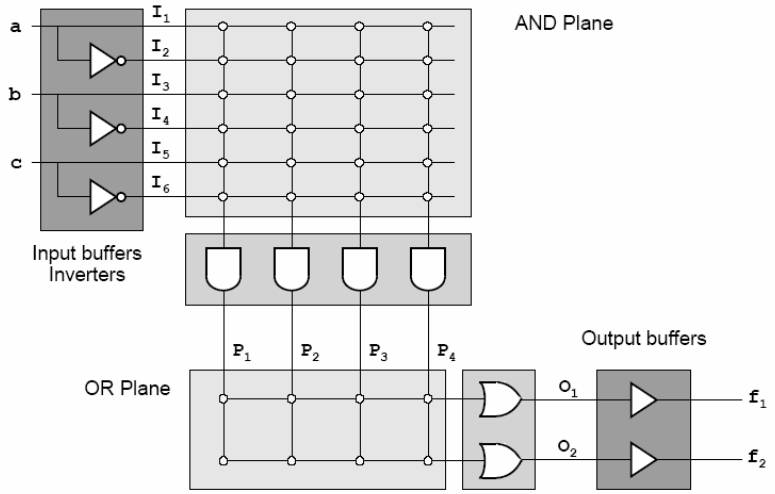


Basic Programmable Logic Devices

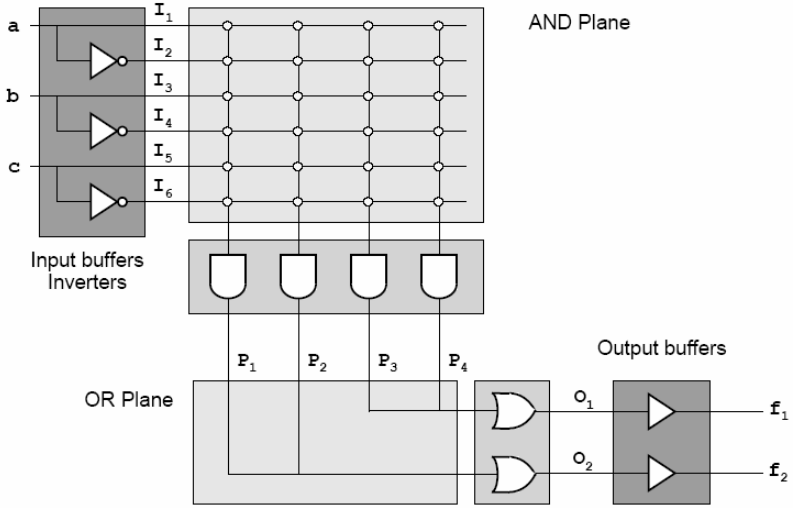


- PLAs (Programmable Logic Arrays)
  - Logic functions in Sum Of Product form
  - Both AND and OR planes are programmable
- PALs (Programmable Array Logics)
  - The AND plane is programmable; the OR plane is fixed
  - Simpler to manufacture, less expensive, better performance than PLAs

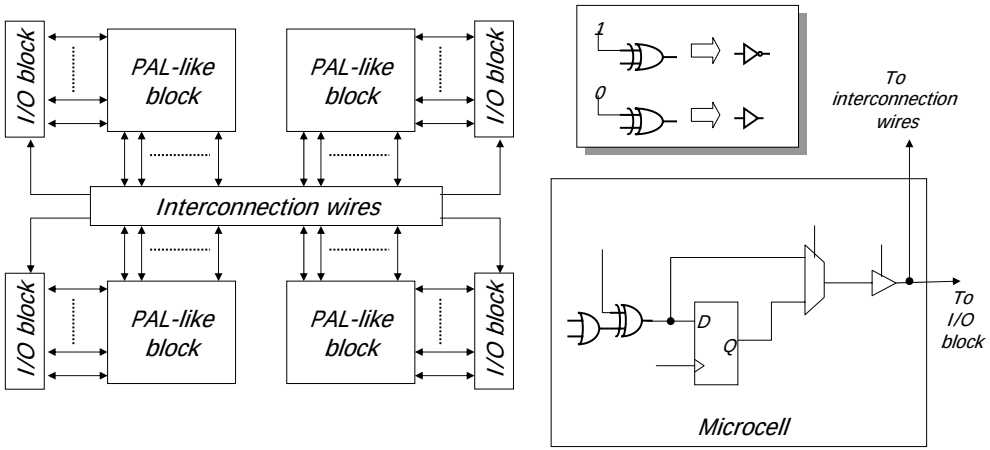
Generic PLA Structure



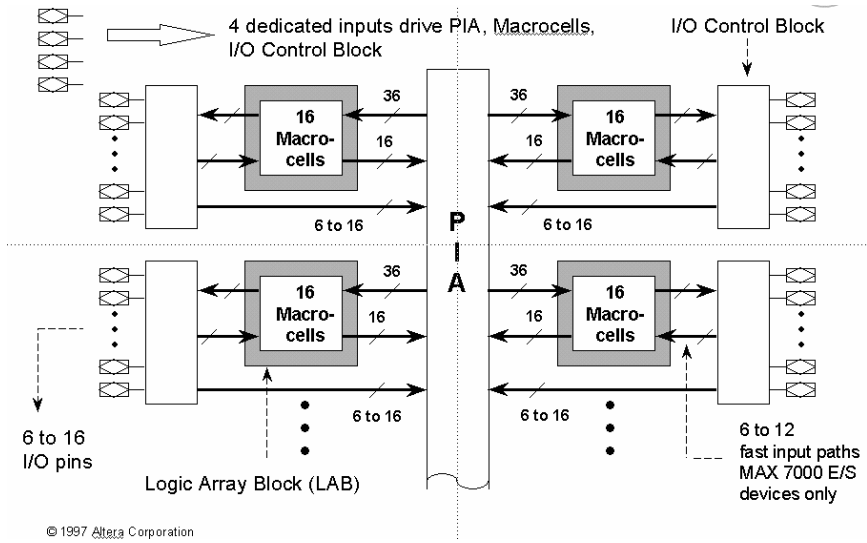
Generic PAL Structure



Complex Programmable Logic Devices (CPLDs)



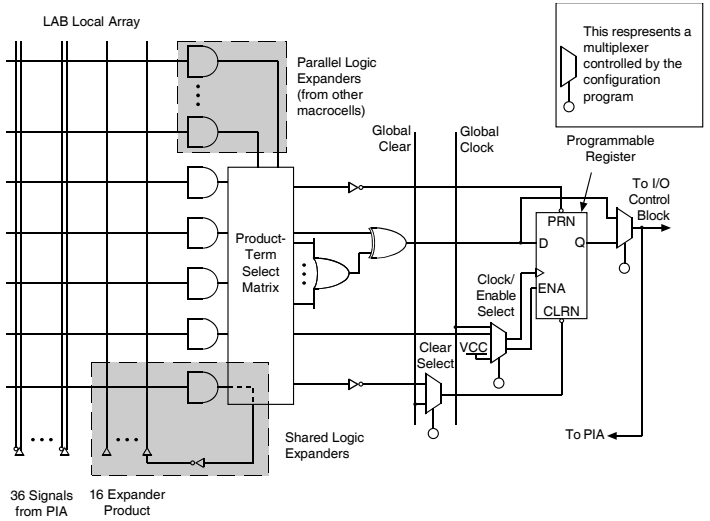
Altera's MAX 7000 Family CPLDs



Altera's MAX 7000 Family CPLDs (2)

- Basic logic element is a **macrocell** which can implement a Boolean expression in the form of **sum-of-product (SOP)**.
- An example of such a sum-of-product is: a•!b•c•!d + a•c•e + !a•f
- Each product term could have many input variables ANDed together. A SOP could have a number of product terms Ored together.
- Each macrocell also contains a flip-flop – essential for implementing FSM.
- 16 macrocells are grouped together to form a **Logic Array Block** (LAB).
- In the centre is a **Programmable Interconnect Array** (PIA) which allows interconnection between different part of the chip.
- Altera currently has:
  - MAX-II and MAX 3000A families low cost CPLDs
  - MAX 7000 family high performance CPLDs

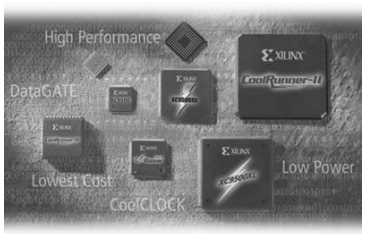
Altera's MAX 7000 Family CPLDs (3)



Altera's MAX 7000 Family CPLDs (4)

- Each horizontal line represents a product term
- Inputs are presented to the product term as signal and its inverse
- Each macrocell can normally OR 4 product terms together
- Each LAB share an additional 16 shared product terms in order to cope with more complex Boolean equations
- Output XOR gate allows either efficient implementation of XOR function or programmable logic inversion
- The SOP output can drive the output directly or can be passed through a register
- Particularly good for implementing finite state machine
- Each register can store one state variable. This can be fed back to the logic array via the Programmable Interconnect Array (PIA)
- Not efficient for adder or multiplier circuits or as buffer storage (such as register file or FIFOs) – waste the potential of the logic array

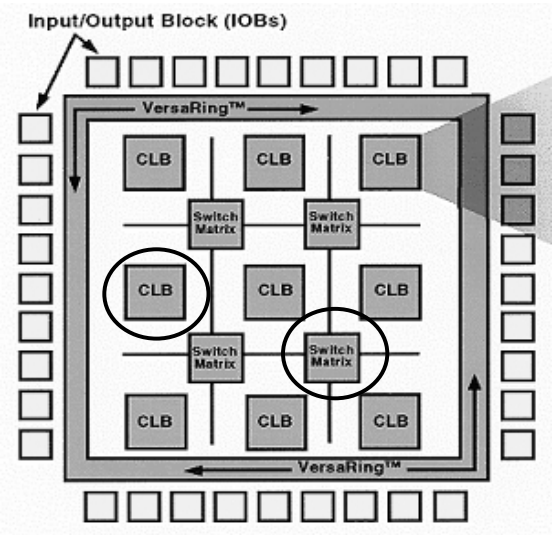
Xilinx CPLDs



Features	CoolRunner-II	XPLA3	XC9500XL/XV	XC9500
Core Voltage	1.8	3.3	3.3/2.5	5.0
Macrocells	32-512	32-512	36-288	36-288
I/Os	21-270	36-260	34-192	34-192
I/O Tolerance	1.5V, 1.8V, 2.5V, 3.3V	5.0V	5.0V (XL), 3.3V, 2.5V, 1.8V (XV)	5.0V, 3.3V
T_{PD} / f max (fastest)	3.8/323	4.5/213	5/222	5/100
Ultra Low Standby Power	28.8µW*	56.1µW	Low power mode	Low power mode
I/O Standards	LVTTL, LVCMOS, HSTL, SSTL	LVTTL, LVCMOS	LVTTL, LVCMOS	LVTTL, LVCMOS

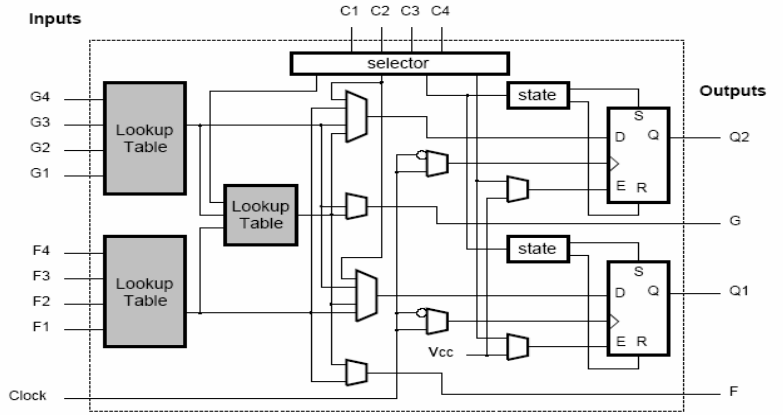
Field Programmable Gate Arrays (FPGAs)

- Xilinx – first to introduce SRAM based FPGA using Lookup Tables (LUTs)
- Xilinx 4000 series contains four main building blocks:
  - Configurable Logic Block (CLB)
  - Switch Matrix
  - VersaRing
  - Input/Output Block



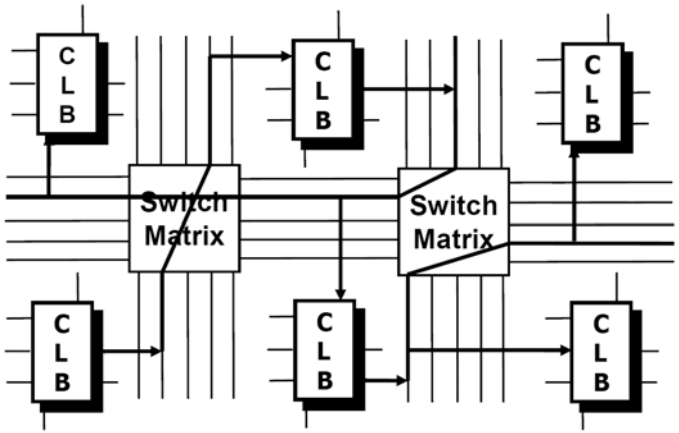
Field Programmable Gate Arrays (FPGAs)

- Each Configurable Logic Block (CLB) has 2 main Look-up Tables (LUTs) and 2 regsters.
- The two LUTs implement two independent logic functions F and G.
- Shown here is the CLB for XC4000 devices



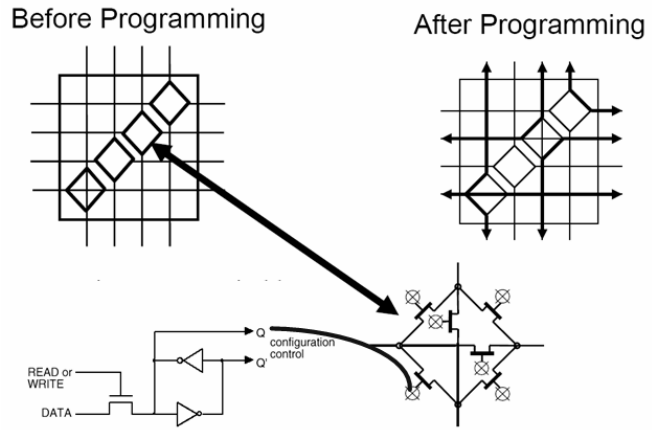
Programmable Interconnect

- Switch-box provides programmable interconnect
  - Local interconnects are fast and short
  - Horizontal and vertical interconnects are of various lengths



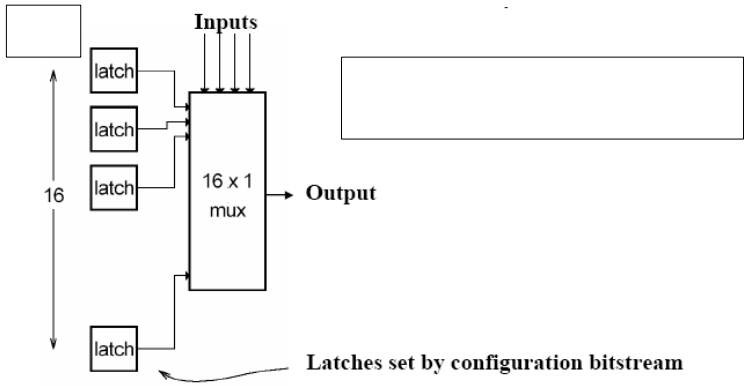
Switch-box circuit

- Here is an example how a switch-box works
  - Each switch-box interconnect point has 6 pass transistors
  - Pass transistors are driven by configuration memory celss



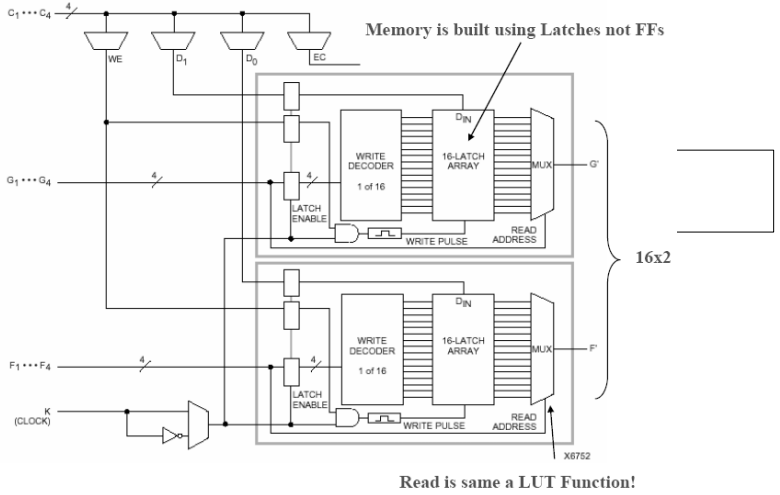
What is in a LUT?

- **L**ook**U**p **T**able (LUT) is implemented using latches:
  - 4-LUT (i.e. 4-input LUT) implements any truth table with 4 inputs
  - Requires 2^4 storage elements, each implemented with a latch (half the size of a register)
  - Multiplexer select one latch to output



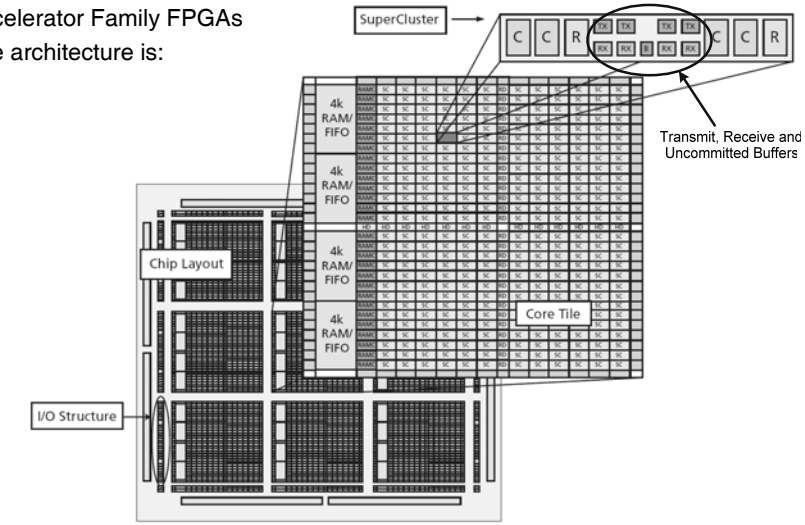
Using CLB as a RAM

- CLB easily changed to a 16 x 2 RAM (distributed RAM)



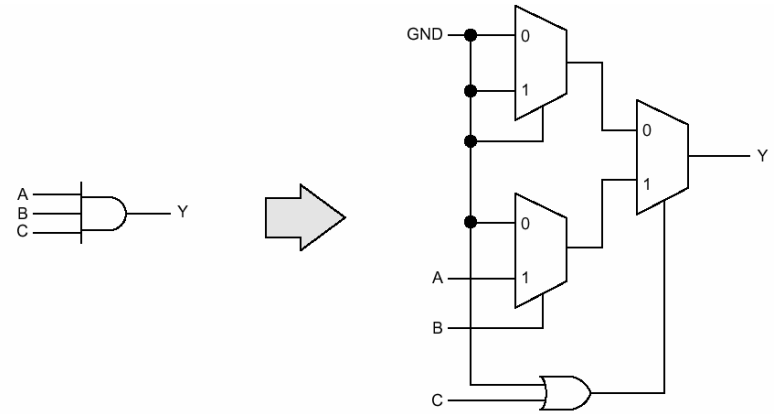
Antifuse FPGAs (Actel)

- Actel's Axcelerator Family FPGAs
- The device architecture is:



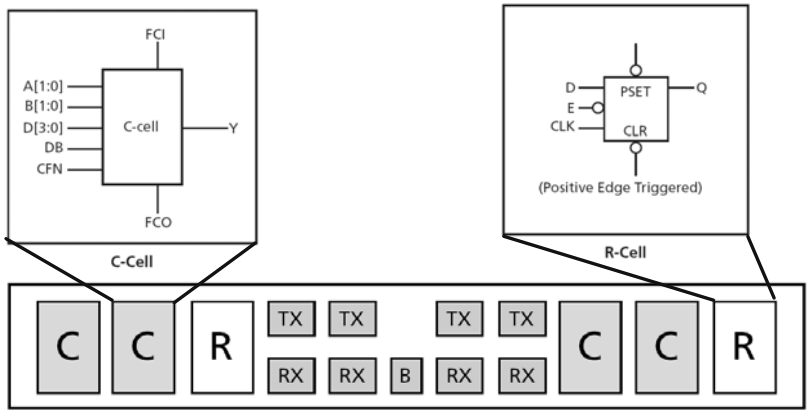
MUX based logic

- Each logic element (labelled 'L') is a combination of multiplexers which can be configured as a multi-input gate



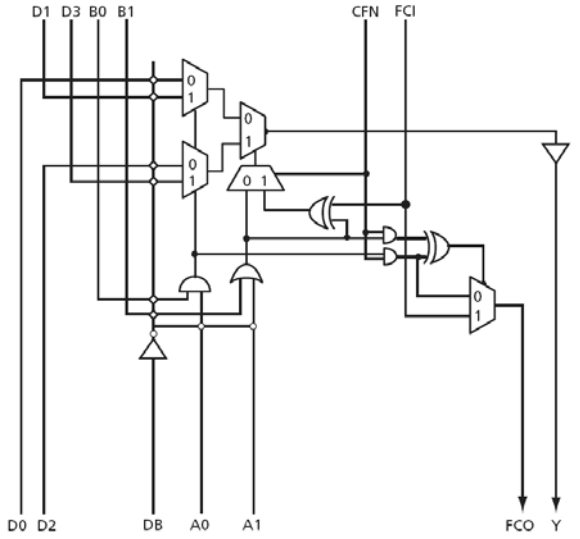
Architecture of a Supercluster

- It contains C cells which implement combinational logic
- R cells which implement reigsters
- Tx, Rx and B buffers



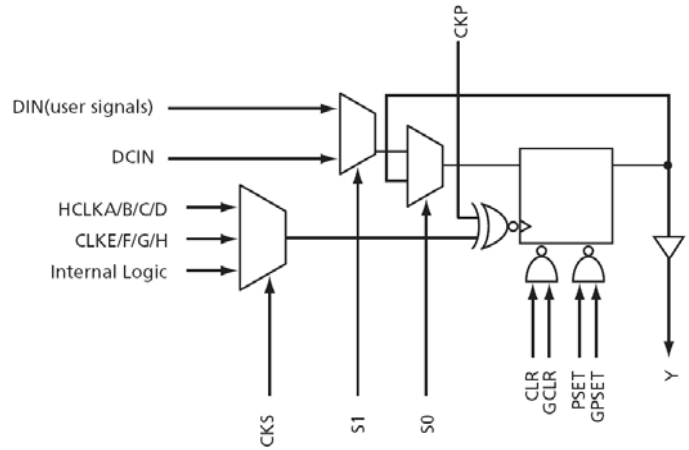
Actel C-Cell

- Contains 8-input MUX (data: D0-D3, select: A0, A1, B0, B1)
- Efficient carry chain for fast arithmetic circuits
- Each C-cell can implement over 4,000 5-input logic functions
- 2 C-cells implements 4-input XOR



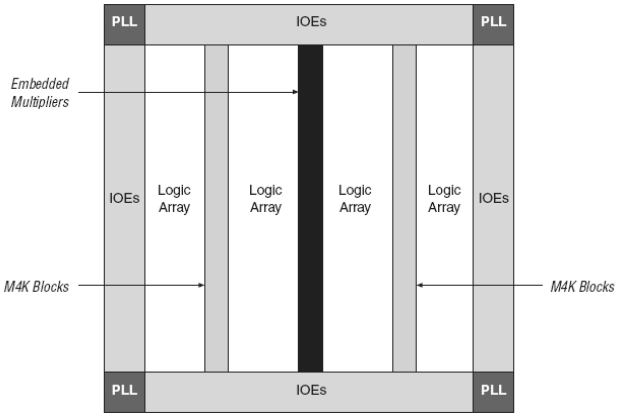
Actel R-Cell

- Flexible Flip-flop with MUX circuits
- Flexible reset/set and clocking connections



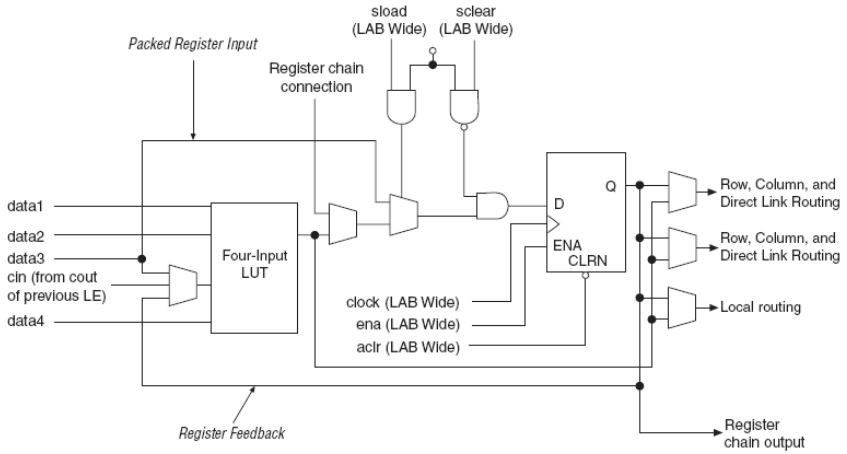
Altera FPGAs – Cyclone II

- This is the FPGA device used in DE2 Board for this course
- Block diagram of a Cyclone II
  - Logic Array containing LUTs
  - Block Memory (M4K Blocks)
  - Embedded Multipliers
  - Input/Output Modules (IOEs)
  - Phase-locked Loops (PLLs)



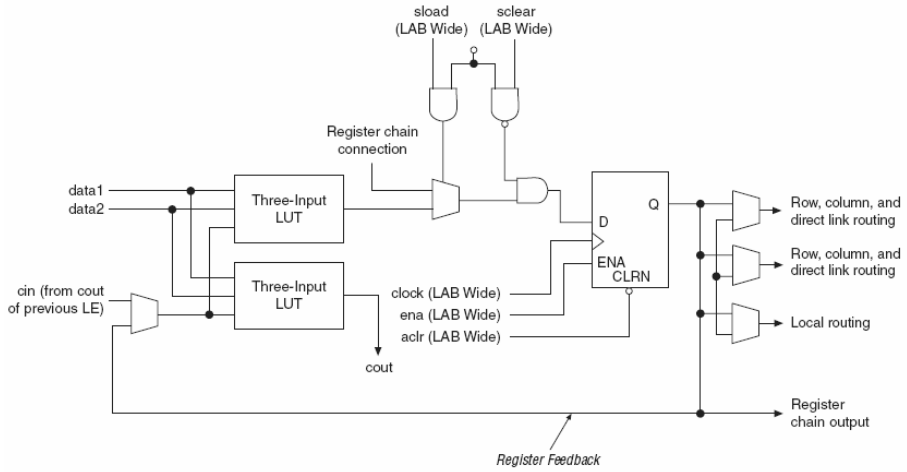
Cyclone II Logic Elements (1)

- The basic logic array contains many Logic Elements (LE) in normal mode
- 16 LEs forms a Logic Array Block (LAB)



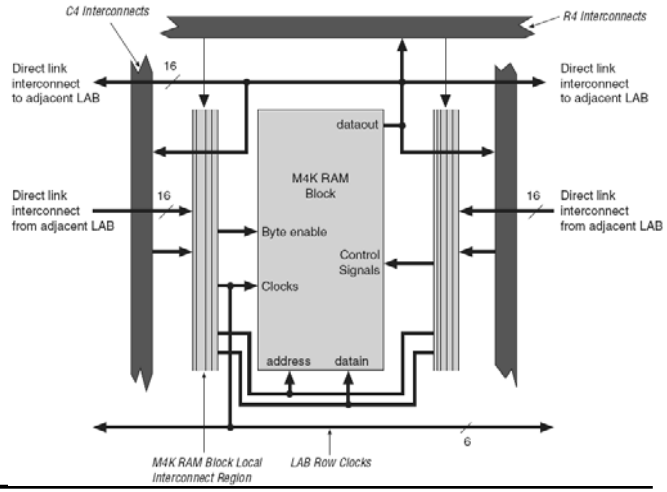
Cyclone II Logic Elements (2)

- An LE can be configured to perform arithmetic function (adder, counter, comparator)



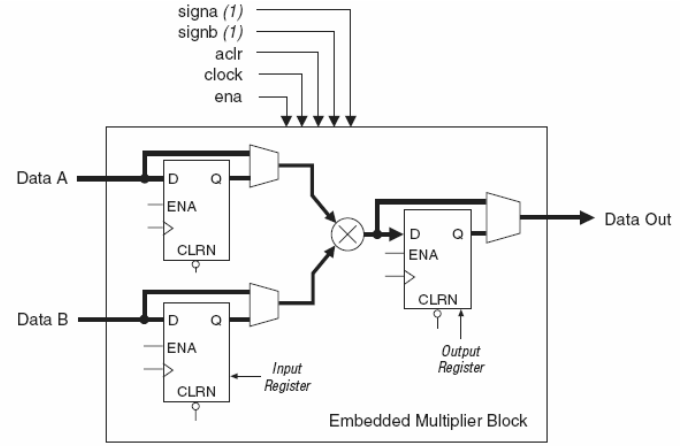
Cyclone II M4K RAM Blocks

- Cyclone II has many blocks of memories, each 4K bits in capacity
- Can be configurabed into 4K x1, 2K x 2 ….. 256 x 18
- Many modes of operations (we will consider in another lecture)



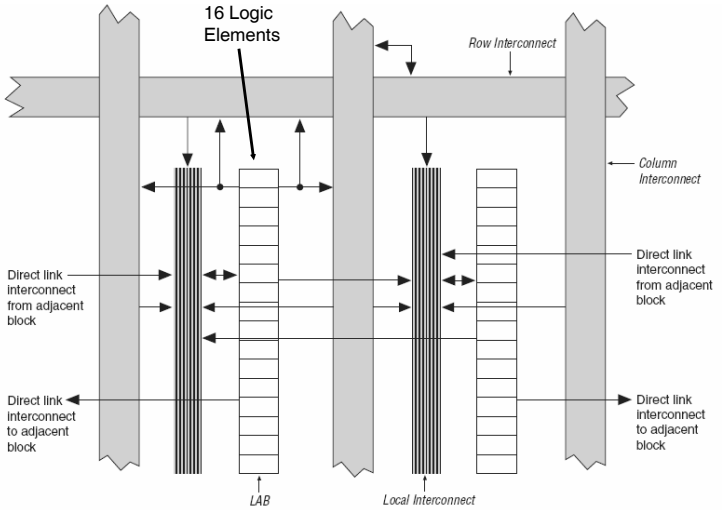
Cyclone II Multipler Blocks

- Cyclone II contain many multiplier blocks
- Can be configurabed into one 18 x 18 multiplier
- Or two 9 x 9 multipliers



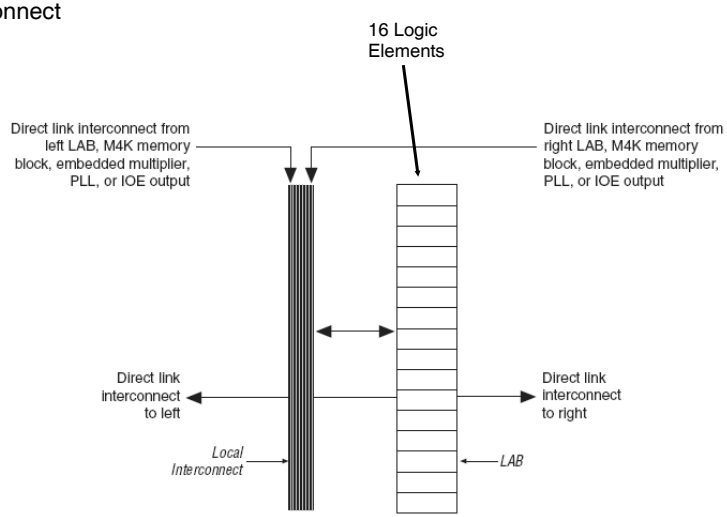
Cyclone II LABs

- 16 LEs are grouped together to form a Logic Array Block (LAB)
- Size of LAB = 1 M4K memory or 1 multiplier block
- Fast local interconnect to connect together LEs within a LAB
- Row and Column wires to connect between LABs



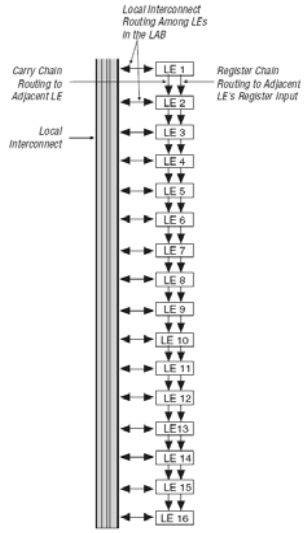
Cyclone II LAB Local interconnect

- Fast Local Interconnect



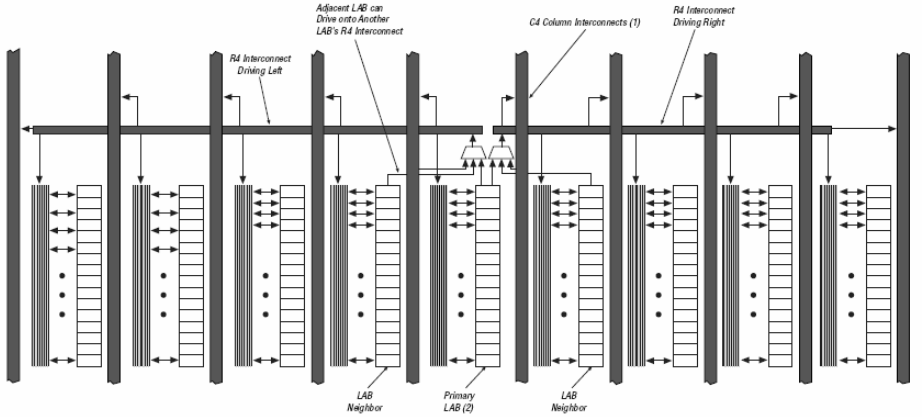
Cyclone II Chaining

- LEs can be chained together for implementing fast adder and counters



Cyclone II LAB Global interconnects

- Row interconnects : 1) direct link between LABs, 2) R4 spanning 4 LABs and 3) R24 traversing the chip
- Column interconnects: 1) Register chain between Les, 2) C4 spanning 4 rows and 3) C16 traversing the device



Cyclone II Family Summary

- DE2 uses EP2C35F672C6 FPGA (672 pins Ball Grid Array)

Table 1–1. Cyclone II FPGA Family Features

Feature	EP2C5	EP2C8 *(2)*	EP2C15 *(1)*	EP2C20 *(2)*	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	52	105	129	250
Total RAM bits	119,808	165,888	239,616	239,616	483,840	594,432	1,152,000
Embedded multipliers *(3)*	13	18	26	26	35	86	150
PLLs	2	2	4	4	4	4	4
Maximum user I/O pins	158	182	315	315	475	450	622

Cyclone II – What's not covered yet?

- Phase Locked Loops (PLLs) and clocking
- Input/Output Elements (IOEs) and interface I/O standards
- Routing and timing issues
- Configuring the chip
- JTAG Boundary Scan interface
- How to interface Cyclone II to other external components (such as memory)

- All these will be covered in later lectures

References & Addition Reading

- "FPGA and CPLD Architectures: A Tutorial", Stephen Brown, Jonathan Rose, IEEE Design & Test, Summer 1996 (Home reading)
- **Xilinx** "Programmable Logic Design – Quick Start Hand Book", 2nd edition, Jan 2002 (download from my course page)
- **Altera** Cyclone II information:
  - http://www.altera.com/products/devices/cyclone2/cy2-index.jsp
- **Actel** Axcelerator literature on the web:
  - http://www.actel.com/products/axcelerator/docs.aspx