**Programmable Logic Devices (PLDs)**

- Supplied with no user programmable logic functions
- Require specialized computer software for design and programming – good quality and low cost
- Implementation of digital circuits with low cost and low risk
- Technology of choice for low to medium volume products (say hundreds to few 10’s of thousands per year)
- Replacing application specific ICs (ASICs) fast!

**Who makes PLDs?**

- ALTERA
- XILINX
- Actel
- Lattice
- Cypress
- Qualcomm

**PLD Technologies**

- Floating Gate/ Flash Programming Technology
- SRAM Programming Technology
- Antifuse Programming Technology

**In-System Programming (ISP):**
performing the programming while the chip is still attached to its circuit board

**JTAG (Boundary Scan):**
A port added to FPGAs for testing purposes, as a means of downloading the design in the programmable device via serial port of a PC
Floating Gates/Flash Technology

- Originally used in product-term type PLDs
- Non-volatile and reprogrammable
- Good for FSM and less good for arithmetic
- Now used by Actel for non product-term devices

SRAM Programming Technology

- Use in all Field Programmable Gate Arrays (FPGAs)
- Static RAM cells are used for three purposes:
  - As lookup tables (LUTs) for implementing logic (as truth-table).
  - As embedded block RAM blocks (for buffer storage etc.).
  - As control to routing and configuration switches.

  Advantages:
  - Easily changeable (even dynamic reconfiguration)
  - Good density
  - Track latest SRAM technology (moving faster than logic technology)
  - Flexible –good for FSM & arithmetic circuits

Disadvantages:
- Volatile
- Generally high power
Antifuse Programming Technology

- Invented at Stanford and developed by Actel
- One-time programmable (OTP) only
- Non-volatile and mostly used for defense and space applications
- Normal fuse programming technology:

Before

After

Antifuse Programming Technology (2)

Antifuse Programming Technology (3)

- Typical antifuse resistance after programming: 20 – 100 ohms
- Program at ~10V
- Fuse thickness ~ 500 – 1000 Å

Basic Programmable Logic Devices

- PLAs (Programmable Logic Arrays)
  - Logic functions in Sum Of Product form
  - Both AND and OR planes are programmable
- PALs (Programmable Array Logics)
  - The AND plane is programmable; the OR plane is fixed
  - Simpler to manufacture, less expensive, better performance than PLAs
Generic PLA Structure

Input buffers

Inverters

AND Plane

OR Plane

Output buffers

I/O block

PAL-like block

Interconnection wires

Microcell

Complex Programmable Logic Devices (CPLDs)

ALTERA'S MAX 7000 FAMILY CPLDs
Altera’s MAX 7000 Family CPLDs (2)

- Basic logic element is a **macrocell** which can implement a Boolean expression in the form of **sum-of-product (SOP)**.
- An example of such a sum-of-product is: \( a \cdot \overline{b} \cdot c \cdot \overline{d} + a \cdot c \cdot e + \overline{a} \cdot f \)
- Each product term could have many input variables ANDed together. A SOP could have a number of product terms ORed together.
- Each macrocell also contains a flip-flop – essential for implementing FSM.
- 16 macrocells are grouped together to form a **Logic Array Block (LAB)**.
- In the centre is a **Programmable Interconnect Array (PIA)** which allows interconnection between different parts of the chip.
- Altera currently has:
  - MAX-II and MAX 3000A families low cost CPLDs
  - MAX 7000 family high performance CPLDs

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Altera’s MAX 7000 Family CPLDs (3)

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Altera’s MAX 7000 Family CPLDs (4)

- Each horizontal line represents a product term
- Inputs are presented to the product term as signal and its inverse
- Each macrocell can normally OR 4 product terms together
- Each LAB share an additional 16 shared product terms in order to cope with more complex Boolean equations
- Output XOR gate allows either efficient implementation of XOR function or programmable logic inversion
- The SOP output can drive the output directly or can be passed through a register
- Particularly good for implementing finite state machine
- Each register can store one state variable. This can be fed back to the logic array via the Programmable Interconnect Array (PIA)
- Not efficient for adder or multiplier circuits or as buffer storage (such as register file or FIFOs) – waste the potential of the logic array

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Xilinx CPLDs

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Field Programmable Gate Arrays (FPGAs)

- Xilinx – first to introduce SRAM based FPGA using Lookup Tables (LUTs)
- Xilinx 4000 series contains four main building blocks:
  - Configurable Logic Block (CLB)
  - Switch Matrix
  - VersaRing
  - Input/Output Block

Each Configurable Logic Block (CLB) has 2 main Look-up Tables (LUTs) and 2 registers.
The two LUTs implement two independent logic functions F and G.
- Shown here is the CLB for XC4000 devices

Programmable Interconnect

- Switch-box provides programmable interconnect
  - Local interconnects are fast and short
  - Horizontal and vertical interconnects are of various lengths

Switch-box circuit

- Here is an example how a switch-box works
  - Each switch-box interconnect point has 6 pass transistors
  - Pass transistors are driven by configuration memory cells
What is in a LUT?

- LookUp Table (LUT) is implemented using latches:
  - 4-LUT (i.e. 4-input LUT) implements any truth table with 4 inputs
  - Requires $2^n$ storage elements, each implemented with a latch (half the size of a register)
  - Multiplexer select one latch to output

Using CLB as a RAM

- CLB easily changed to a 16 x 2 RAM (distributed RAM)

Antifuse FPGAs (Actel)

- Actel’s Axcelerator Family FPGAs
- The device architecture is:

MUX based logic

- Each logic element (labelled ‘L’) is a combination of multiplexers which can be configured as a multi-input gate
Architecture of a Supercluster

- It contains C cells which implement combinational logic
- R cells which implement registers
- Tx, Rx and B buffers

Actel C-Cell

- Contains 8-input MUX (data: D0-D3, select: A0, A1, B0, B1)
- Efficient carry chain for fast arithmetic circuits
- Each C-cell can implement over 4,000 5-input logic functions
- 2 C-cells implements 4-input XOR

Actel R-Cell

- Flexible Flip-flop with MUX circuits
- Flexible reset/set and clocking connections

Altera FPGAs – Cyclone II

- This is the FPGA device used in DE2 Board for this course
- Block diagram of a Cyclone II
  - Logic Array containing LUTs
  - Block Memory (M4K Blocks)
  - Embedded Multipliers
  - Input/Output Modules (IOEs)
  - Phase-locked Loops (PLLs)
Cyclone II Logic Elements (1)

- The basic logic array contains many Logic Elements (LE) in normal mode
- 16 LEs forms a Logic Array Block (LAB)

Cyclone II Logic Elements (2)

- An LE can be configured to perform arithmetic function (adder, counter, comparator)

Cyclone II M4K RAM Blocks

- Cyclone II has many blocks of memories, each 4K bits in capacity
- Can be configurabed into 4K x 1, 2K x 2 ..... 256 x 18
- Many modes of operations (we will consider in another lecture)

Cyclone II Multiplier Blocks

- Cyclone II contain many multiplier blocks
- Can be configurabed into one 18 x 18 multiplier
- Or two 9 x 9 multipliers
Cyclone II LABs

- 16 LEs are grouped together to form a Logic Array Block (LAB)
- Size of LAB = 1 M4K memory or 1 multiplier block
- Fast local interconnect to connect together LEs within a LAB
- Row and Column wires to connect between LABs

Cyclone II LAB Local interconnect

- Fast Local Interconnect

Cyclone II Chaining

- LEs can be chained together for implementing fast adder and counters

Cyclone II LAB Global interconnects

- Row interconnects: 1) direct link between LABs, 2) R4 spanning 4 LABs and 3) R24 traversing the chip
- Column interconnects: 1) Register chain between LEs, 2) C4 spanning 4 rows and 3) C16 traversing the device
Cyclone II Family Summary

- DE2 uses EP2C35F672C6 FPGA (672 pins Ball Grid Array)

<table>
<thead>
<tr>
<th>Table 1–1. Cyclone II FPGA Family Features</th>
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<tbody>
<tr>
<td>----------------------------</td>
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<tr>
<td>LEs</td>
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<tr>
<td>M4K RAM blocks (4 Kbits plus 512 parity bits)</td>
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<tr>
<td>Total RAM bits</td>
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<td>Embedded multipliers (3)</td>
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<td>PLLs</td>
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<td>Maximum user I/O pins</td>
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</tbody>
</table>

Cyclone II – What’s not covered yet?

- Phase Locked Loops (PLLs) and clocking
- Input/Output Elements (IOEs) and interface I/O standards
- Routing and timing issues
- Configuring the chip
- JTAG Boundary Scan interface
- How to interface Cyclone II to other external components (such as memory)
- All these will be covered in later lectures

References & Addition Reading

- Xilinx “Programmable Logic Design – Quick Start Hand Book”, 2nd edition, Jan 2002 (download from my course page)
- Altera Cyclone II information:
- Actel Accelerator literature on the web: