Topic 7

Practical Digital Design: I/O interfacing

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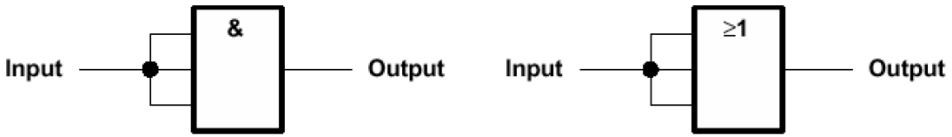
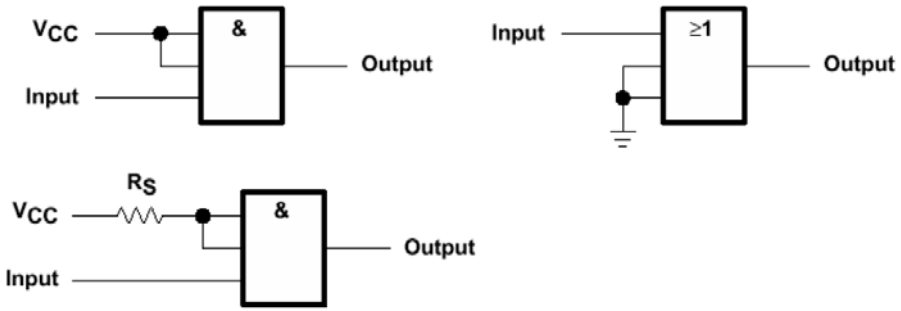
Unused inputs (1)

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that should be applied to any particular unused input depends on the function of the device.
- One solution is to connect unused inputs to an input of the same gate that is in use. Connecting the inputs together increases the capacitive load on the driver stage and, with bipolar circuits, also increases the dc current drain.



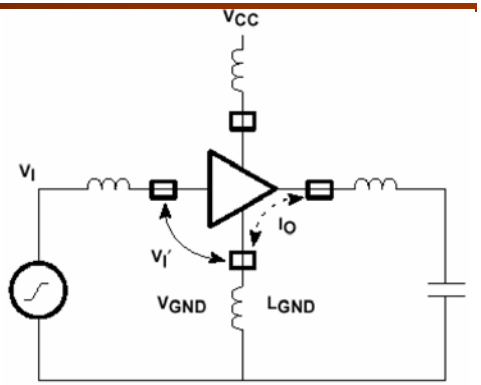
Unused inputs (2)

- A better solution is to apply a fixed logic level to the unused inputs. If a low level is required, the input should be directly connected to GND; if a high level is required, it should be connected to the positive supply voltage Vcc directly of via a series resistor.



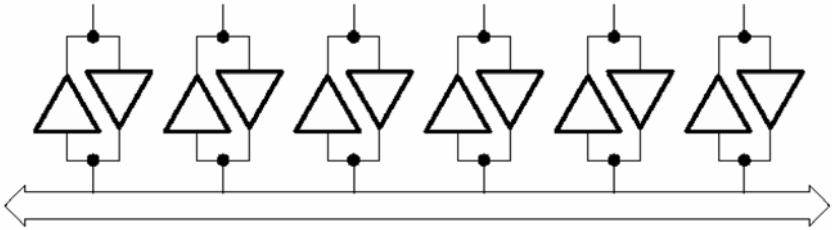
Slow Input Edge Rate

- A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations.
- Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.
- These functional problems are due to voltage transients induced on the device's power system.
- In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction.
- If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate.



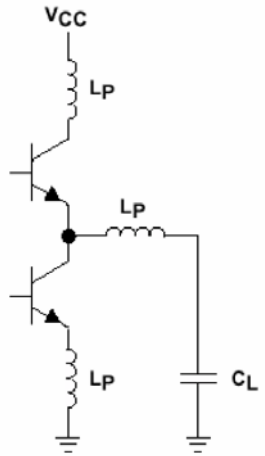
Avoid floating inputs

- This is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined.
- When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*.
- The result is a considerable increase in power consumption and a risk of damaging all components on the bus.
- Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.



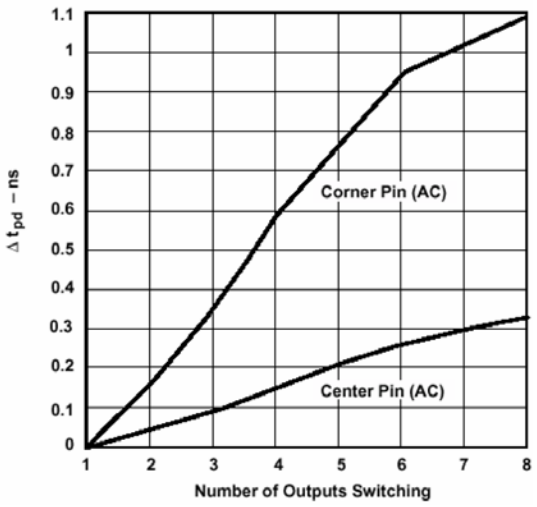
Simultaneous Switching Outputs (1)

- The propagation delay times of circuits given in data sheets apply when only **one output switches at a time**. The reason for this is that the production equipment used to test circuits can test only one transmission channel at a time.
- If several outputs switch simultaneously, beware of datasheet!. The reason for this is that the **package inductances** (L_P) of the supply-voltage lines, as well the output lines (see figure below), have a significant influence on the circuits and, thus, on the delay times.
- These inductances have the effect that the current in the power supply lines, and consequently in the output of the device, has a limited rate of rise.
- When several outputs switch simultaneously, only a limited output current is available.



Simultaneous Switching Outputs (2)

- This figure shows the influence on the delay time of the number of outputs that are switched simultaneously.
- An increase of the delay time of 150 ps to 200 ps for each additional output that is simultaneously switched can be expected.
- With an octal bus driver, such as an SN74xx240, the delay time is increased by 1 ns to 1.4 ns when all eight outputs switch simultaneously.

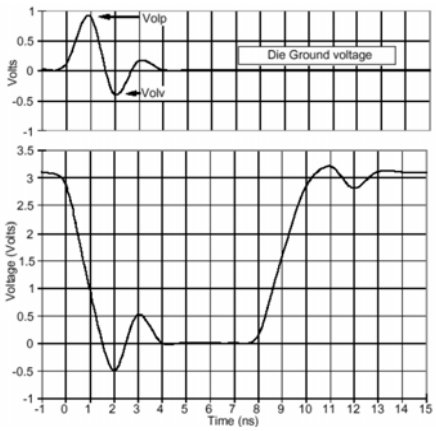


Ground Bounce (1)

- Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die.
- Ground Bounce is one of the **primary causes of false switching in high speed components** and is a major cause of poor signal quality.
- Essentially it is caused by a current surge passing through the lead inductance of the package.
- The effect is most pronounced when all outputs switch simultaneously, (hence the alternate name, Simultaneous Switching Noise).

Ground Bounce (2)

- While the inductance is the combined effect of the package lead, the package lead frame, the bond wire and the inductance in the die pad, most of the inductance is caused by the bond wire.
- This figure shows a typical waveform for a high speed CMOS component with TTL level outputs. Shown directly above the signal waveform on the same time scale is the voltage seen on the ground of the die relative to the external ground.

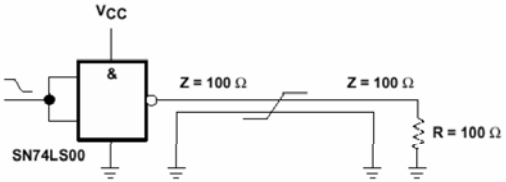


Ground Bounce (3)

- Ground Bounce levels are typically more pronounced than Vcc Bounce levels because of the HIGH to LOW transition is trying to quickly bring a HIGH signal down to a narrow window of <400mV for a logic LOW. A low output impedance is required to complete the transition quickly.
- In the LOW to HIGH, the only requirement is that the output be above 2.4V. 5V is available as a driving voltage. A much lower pull up impedance is required to make the transition quickly.
- Ground Bounce effect can be reduced by:
  1. Using more Vcc/Gnd pins (offered by manufacturers)
  2. Avoid pullup/pulldown resistors (i.e. use bus hold circuit)
  3. Possibly use series damping resistors (see later)
  4. Control output slew rate
  5. Extra care in holding clock signals to solid voltage level (Vh) and fast clock transistions

Capacitive Loads or Transmission Line (1)

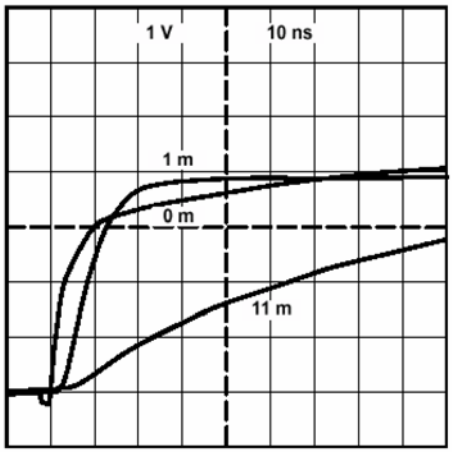
- In data sheets, propagation delay times are specified with a capacitive load of 50 pF.
- This value is also the capacitive load when the output drives five inputs of other circuits and this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards (PCBs).
- With such short lines, the first assumption is that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly.



- However, with long lines, this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wavefront along the line.
- In fact, the propagation delay time of the device is determined by the loading of the output, that is, by the characteristic impedance of the line to which it is connected, not by its length or capacitance.

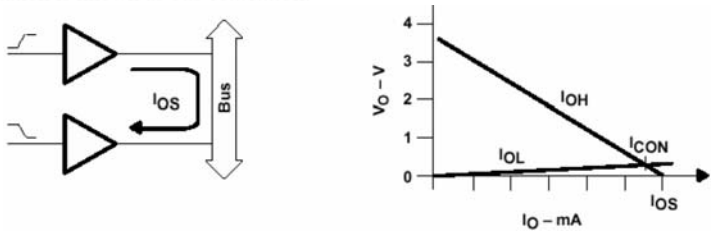
Capacitive Loads or Transmission Line (2)

- When driving a line terminated at its end with a resistance of 100Ω, and lengths of 0 (resistor connected directly to the output), 1 m, and 11 m (see below), an SN74LS00 device has the output waveforms shown in this figure.
- The length of the line and the resulting signal propagation time (5 ns/m) influence the delay time of the system. The propagation time of the wave along an 11-m transmission line is 55 ns. Add the propagation delay time of the SN74LS00 of about 10 ns for a total delay of 65 ns.



Bus Contention

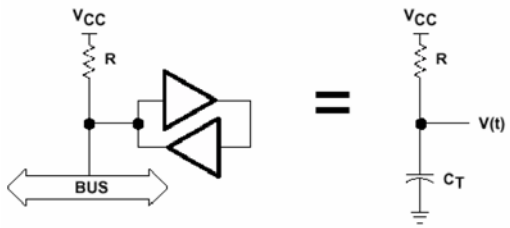
- For this short time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation is known as *bus contention*.



- Bus contention during power-on - bus contention that can last several 100 ms
- Even if no defect is detected after such bus contention, a dramatic degradation of the device is likely, which leads to a final destruction of the component some time later.
- Preventing bus contention is not easy.
- One method is to connect a pullup resistor between the enable inputs (assuming low active) of the bus-interface circuits and the positive supply rail.
- A reliable solution is to disable all bus-interface circuits in question during the critical time with additional control logic

Pullup or Pulldown resistors

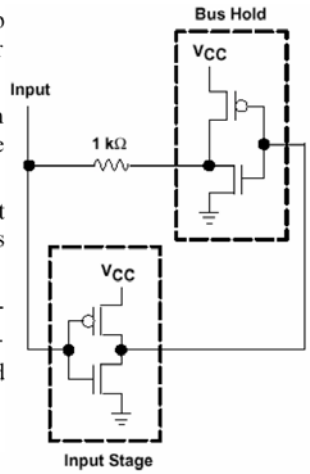
- When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components being damaged or overheated.
- A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem occur.



- Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated selecting pullup or pulldown resistors. Otherwise, components may oscillate, or device reliability may affected.
- This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical.
- Instead, use the **bus-hold** feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

Bus Hold Circuit

- Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors.
- Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 4.17).
- To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit.
- Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor.
- The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit.
- The same condition applies when the bus is in the low state and then goes inactive.



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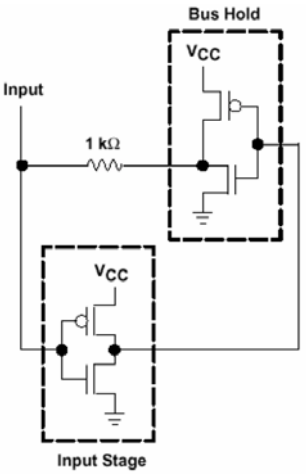
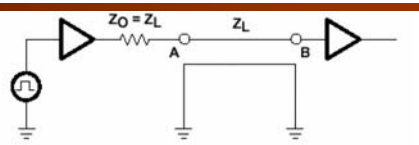
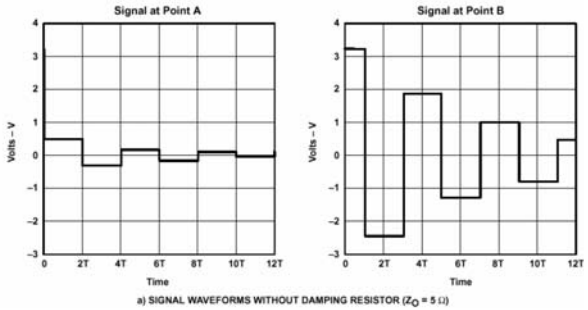


Series Damping Resistor (1)

- The purpose of integrating output-damping resistors in line buffers and drivers is to suppress signal undershoots and overshoots on the transmission line through what is usually referred to as line-impedance matching (see Figure 1).



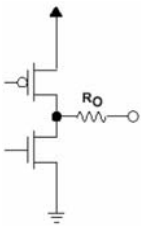
- The effective output impedance of the line driver (Z_O) is matched with the line impedance (Z_L) . Thus, no signal reflection occurs at the line start.
- The input impedance of the receiving device (Z_I) is assumed to be several orders of magnitude higher than the line impedance. This is valid for CMOS and BiCMOS devices. In this case, the reflection coefficient at point B is approximately 1, such that almost all of the wave energy is reflected at the end of the line.

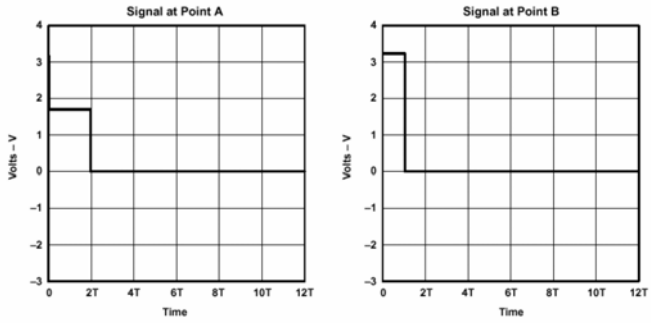


a) SIGNAL WAVEFORMS WITHOUT DAMPING RESISTOR (Z_O = 5 Ω)

Series Damping Resistor (2)

- To reduce this ringing effect, output damping resistors can be added:
- The effect of this resistor (typically 25-33Ω) is to eliminate most of the ringing effect:

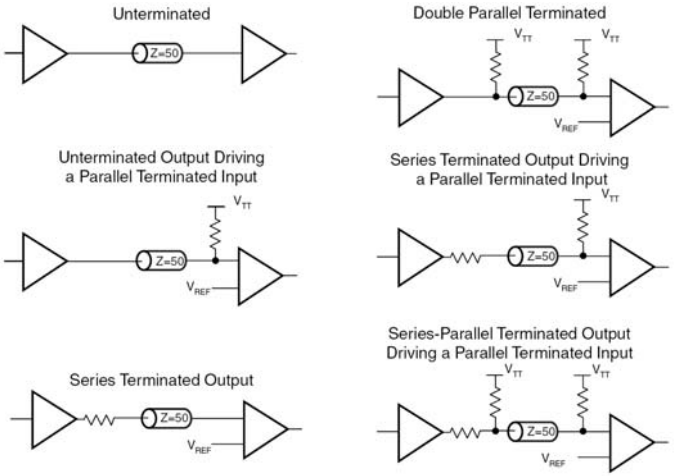




b) SIGNAL WAVEFORMS WITH DAMPING RESISTOR ($Z_O = Z_L$ = 33 Ω)

FPGAs provides many of these functions (1)

- Here is a summary of different terminations that may be programme on a typical FPGA I/O block (example taken from Xilinx).

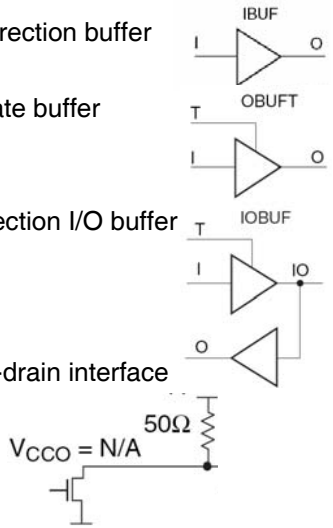


Modern Electronics I/O Standards

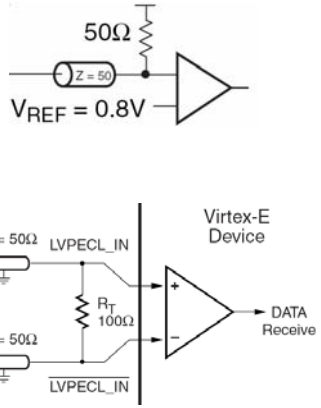
- Modern digital electronics use many different I/O standards.
- Here is an incomplete list:
  - LVTTL – Low-voltage TTL
  - LVCMOS2 – Low-voltage CMOS for 2.5v
  - PCI – Peripheral Component Interface
  - GTL – Gunning Transceiver Logic (Terminated)
  - GTL+ - Gunning Transceiver Logic Plus
  - HSTL – High-Speed Transceiver Logic
  - SSTL2 – Stub Series Terminated Logic for 2.5v
  - SSTL3 – Stub Series Terminated Logic for 3.3v
  - LVDS – Low Voltage Differential Signals
  - AGP – Advanced Graphics Port
- The following specifications of these standards refer to those used by Xilinx in their Virtex family of FPGAs.

Types of I/O

- Uni-direction buffer
- Tri-state buffer
- Bi-direction I/O buffer
- Open-drain interface

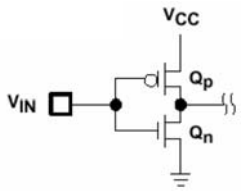


- Differential interfaces



LVTTL — Low-Voltage TTL

- The LVTTL standard is a general purpose EIA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer.
- The input and output buffers are both 5V-tolerant. This standard requires a 3.3V output source voltage (VCCO), but does not require the use of a reference voltage (VREF) or a termination voltage (VTT).



Parameter		Min	Typ	Max
V_{CCO}		3.0	3.3	3.6
V_{REF}		-	-	-
V_{TT}		-	-	-
V_{IH}	Virtex	2.0	-	5.5
	Virtex-E & Virtex-EM	2.0	-	3.6
V_{IL}		–0.5	-	0.8
V_{OH}	Virtex	2.4	-	-
	Virtex-E & Virtex-EM	2.4	-	-
V_{OL}		-	-	0.4
I_{OH} at V_{OH} (mA)		–24	-	-
I_{OL} at V_{OL} (mA)		24	-	-

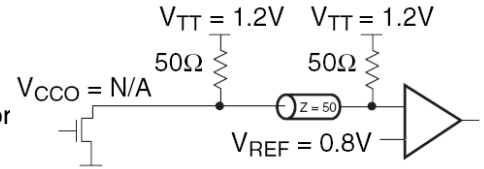
LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

- The LVCMOS2 standard is an extension of the LVCMOS standard used for general purpose 2.5V applications.
- It uses a 5V tolerant CMOS input buffer and a Push-Pull output buffer. This standard requires a 2.5V output source voltage (VCCO), but does not require the use of a reference voltage (VREF) or a board termination voltage (VTT).

Parameter		Min	Typ	Max
V_{CCO}		2.3	2.5	2.7
V_{REF}		-	-	-
V_{TT}		-	-	-
V_{IH}	Virtex	1.7	-	5.5
	Virtex-E & Virtex-EM	1.7	-	3.6
V_{IL}		–0.5	-	0.7
V_{OH}		1.9	-	-
V_{OL}		-	-	0.4
I_{OH} at V_{OH} (mA)		–12	-	-
I_{OL} at V_{OL} (mA)		12	-	-

GTL — Gunning Transceiver Logic Terminated

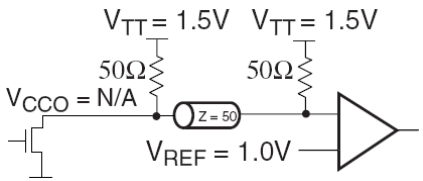
- The GTL standard is a high-speed bus standard invented by Xerox.
- Many FPGA companies have implemented the terminated variation for this standard, requiring a differential amplifier input buffer and a Open Drain output buffer.



Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$[1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} \geq V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} \leq V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL} at V_{OL}(mA) at 0.4V	32	-	-
I_{OL} at V_{OL}(mA) at 0.2V	-	-	40

GTL+ — Gunning Transceiver Logic Plus

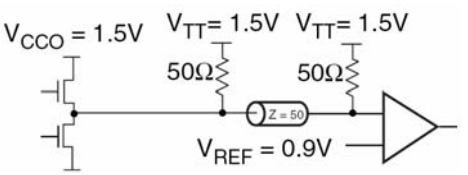
- The GTL+ standard is a high-speed bus standard derived from GTL, first used by the Pentium Pro processor.



Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$[1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} \geq V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} \leq V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

HSTL — High-Speed Transceiver Logic

- The HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM and has four variations or classes.
- This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

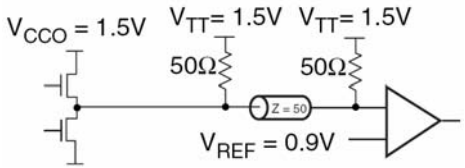


HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}		0.90	
V_{TT}		V_{CCO}	
V_{IH}	V_{REF} + 0.1		
V_{IL}			V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4		
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

SSTL3 — Stub Series Terminated Logic for 3.3V

- A general purpose 3.3V memory bus standard sponsored by Hitachi and IBM.
- This standard has two classes, I and II.
- This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.



HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}		0.90	
V_{TT}		V_{CCO}	
V_{IH}	V_{REF} + 0.1		
V_{IL}			V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4		
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

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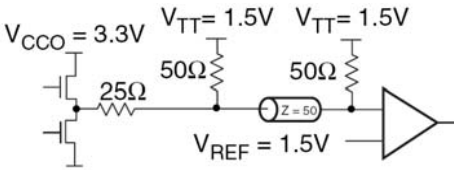
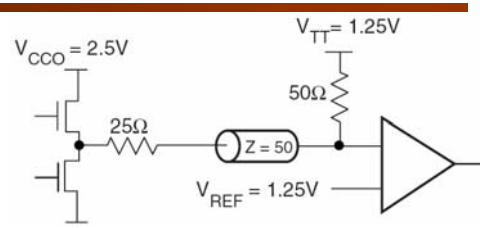


SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	2.3	-
$V_{OL} \leq V_{REF} - 0.8$	-	0.7	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

SSTL2 — Stub Series Terminated Logic for 2.5V

- The SSTL2 standard is the same as SSTL3, but for 2.5V.
- There are also two classes: I & II.

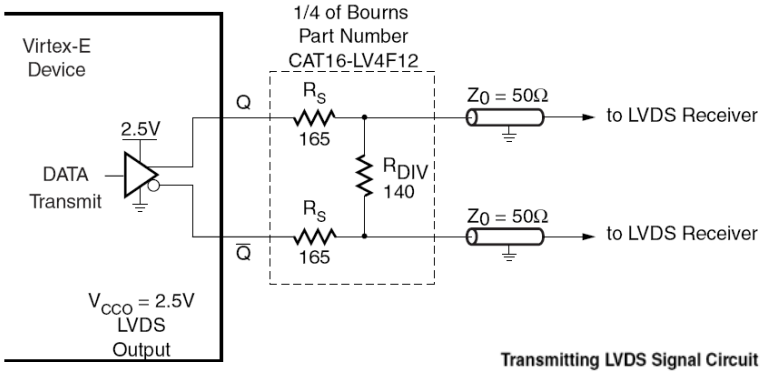


Terminated SSTL2 Class I

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	3.0[2]
$V_{IL} \leq V_{REF} - 0.18$	–0.3[3]	1.07	1.17
$V_{OH} \geq V_{REF} + 0.61$	1.76	1.82	1.96
$V_{OL} \leq V_{REF} - 0.61$	0.54	0.64	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

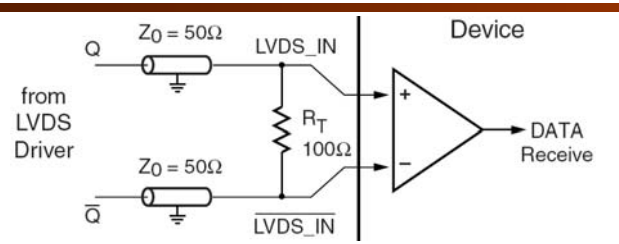
LVDS – Low voltage differential signal (1)

- This is a fully differential signals often used for very high speed network connections.
- The transmit and receive circuits are different.



Transmitting LVDS Signal Circuit

LVDS – Low voltage differential signal (2)



Receiving LVDS Signal Circuit

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
$V_{ICM}^{(2)}$	0.2	1.25	2.2
$V_{OCM}^{(1)}$	1.125	1.25	1.375
V_{IDIFF} (mV)[1]	100	350	-
V_{ODIFF} (mV)[1]	250	350	450
$V_{OH}^{(1)}$	1.25	-	-
$V_{OL}^{(1)}$	-	-	1.25

FPGAs provides many of these functions (2)

- Other programmable features (in addition to termination) are:
  - Input Reference Voltage (Vref)
  - Output Source Voltage (Vcco)
  - Board Termination Voltage (Vtt)
  - Output Slew Rate
  - Output Drive Strength
  - Synchronous/Asynchronous I/O
  - Programmable Output Delay (called ChipSynch in Xilinx)

Xilinx Virtex 5 I/O capability

- Each pin can be input and (3-state-able) output
- Each pin can be individually configured for:
  - ChipSync, XCITE termination, drive strength, input threshold, weak pull-up or -down
- Each input can be 3.3-V tolerant, limited by its Vcco
  - No 5-V tolerance, unless current-limiting R is used
- Each I/O can have the same performance
  - Up to 700 Mbps single-ended & 1.25 Gbps differential LVDS
- Each I/O supports 40+ voltage and protocol standards including:

- LVCMOS (***3.3v***, 2.5v, 1.8v, 1.5v, and ***1.2v***)
- LVDS, Bus LVDS, Extended LVDS
- LCPECL
- PCI, PCI-X
- HyperTranport (LDT)

- HSTL (1.8v, 1.5v, Classes I, II, III, IV)
- ***HSTL_I_12 (unidirectional only)***
- ***DIFF_HSTL_I_18, DIFF_HSTL_I_18_DCI***
- ***DIFF_HSTL_I, DIFF_HSTL_I_DCI***
- ***RSDS_25 (point-to-point)***

- SSTL (2.5v, 1.8v, Classes I, II)
- ***DIFF_SSTL_I***
- ***DIFF_SSTL2_I_DCI***
- ***DIFF_SSTL18_I, DIFF_SSTL18_I_DCI***
- GTL, GTL+

Altera Cyclone-II I/O Features

I/O Structure & Features

IOEs support many features, including:

- Differential and single-ended I/O standards
- 3.3-V, 64- and 32-bit, 66- and 33-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Output drive strength control
- Weak pull-up resistors during configuration
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- V_{REF} pins

All I/O Banks Support

- *3.3-V LVTTL/LVCMOS*
- *2.5-V LVTTL/LVCMOS*
- *1.8-V LVTTL/LVCMOS*
- *1.5-V LVCMOS*
- *LVDS*
- *RSDS*
- *mini-LVDS*
- *LVPECL (3)*
- *SSTL-2 Class I and II*
- *SSTL-18 Class I*
- *HSTL-18 Class I*
- *HSTL-15 Class I*
- *Differential SSTL-2 (4)*
- *Differential SSTL-18 (4)*
- *Differential HSTL-18 (5)*
- *Differential HSTL-15 (5)*

Useful References

- Application Notes SDYA009C, “Designing with Logic”, Texas Instrument, June 1997.
- XAPP133, “Using the Virtex Select I/O Resource”, Xilinx.
- Cyclone II Device Handbook, Vol. 1, p. 2-37 to 2-61.