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TMS320 DSP Product Family

Glossary

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Product Family

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Preface

Read This First

About This Manual

This glossary lists and explains terms used to describe the functions of all devices in the TMS320 family. Some entries pertain only to a specific device. The device is indicated at the end of each entry in italicized text.

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DSP Glossary

A

A0–A*n*: External address pins for data/program memory or I/O devices.

absolute address: An address that is permanently assigned to a memory location. See also *symbolic address*.

absolute lister: A debugging tool that accepts linked files as input and creates .abs files as output. These .abs files can be assembled to produce a listing that shows the absolute addresses of object code. Without the tool, an absolute listing can be prepared with the use of many manual operations.

ABU: See a*utobuffering unit*.

ACC: See *accumulator.*

ACCB: See *accumulator buffer*.

access stage: The optional third stage of the master processor's fetch, execute, access (FEA) pipeline, during which memory accesses (load or store operations) occur. (*TMS320C8x*)

ACCH: See *accumulator high byte*.

ACCL: See *accumulator low byte.*

accumulator (ACC): A register that temporarily stores the results of an arithmetic logic unit (ALU) operation and provides an input for subsequent ALU operations. The ACC is accessible in two halves: accumulator high (ACCH) and accumulator low (ACCL).

accumulator buffer (ACCB): A register that temporarily stores the contents of the accumulator (ACC). The ACCB has a direct path back to the arithmetic logic unit (ALU) and can be arithmetically or logically acted upon with the ACC.

accumulator high byte (ACCH): The most significant bits stored in the accumulator (ACC). See also *accumulator*.

accumulator low byte (ACCL): The least significant bits stored in the accumulator (ACC). See also *accumulator*.

active time: The time intervals of a display frame that are not in blanking. The time intervals in which pixels are displayed. See also *blanking*. (*TMS320C8x)*

active window: The window that is currently selected for moving, sizing, editing, closing, or some other function.

A/D: See *analog-to-digital.*

ADC: See *analog-to-digital converter*.

ADC bit: See *detect complete bit*.

address: The logical location of program code or data stored in memory.

addressing mode: The method by which an instruction interprets its operands to acquire the data it needs.

address stage: The second stage of the parallel processor's fetch, address, execute (FAE) pipeline during which addresses are calculated and supplied to the crossbar. (*TMS320C8x*)

address unit: Hardware on the parallel processor that computes a bit address during each cycle. Each parallel processor has two address units: a global address unit and a local address unit. (*TMS320C8x*)

address unit arithmetic: The parallel processor's use of the local and global address units to perform general-purpose arithmetics in parallel with the data unit. The computed address is not used for memory access, but is stored in the destination register. (*TMS320C8x*)

address visibility (AVIS) bit: A bit field that allows the internal program address to appear at the external address pins. This enables the internal program address to be traced and the interrupt vector to be decoded in conjunction with the interrupt acknowledge ($\overline{\text{IACK}}$) signal when the interrupt vectors reside in on-chip memory. At reset, AVIS = 0. (*TMS320C5x, TMS320C54x, TMS320C2xx*)

administrative privileges: Authority to set software and hardware access; includes access and privileges to install, manage, and maintain system and application software and directories on a network server or individual computer systems.

ADTR: *Asynchronous data transmit and receive register*. See also *receive (ADTR) register*.

AFB: See *auxiliary register file bus*.

aggregate type: A C data type, such as a structure or an array, in which a variable is composed of multiple other variables, called members.

AIC: See *analog interface circuit.*

A-Law companding: See *companded*.

alias disambiguation: A technique that determines when two pointer expressions cannot point to the same location, allowing the compiler to freely optimize such expressions. (*TMS320C6200*)

aliasing: 1) A method of customizing debugger commands; aliasing provides a shorthand method for entering often-used command strings. 2) A method of accessing a single data object in more than one way, as when a pointer points to a named object. The optimizer has logic to detect aliasing, but aliasing can cause problems for the optimizer. 3) Aliasing occurs when a single object can be accessed in more than one way, such as when two pointers point to a single object. It can disrupt optimization, because any indirect reference could refer to any other object.

alignment: A process in which the linker places an output section at an address that falls on an *n*-byte boundary, where *n* is a power of 2. You can specify alignment with the SECTIONS linker directive.

allocation: A process in which the linker calculates the final memory addresses of output sections.

allocation node: The processor node into which an internode message is allocated.

ALU: See *arithmetic logic unit.*

ALU function: For the parallel processor, an action performed on the three inputs to the arithmetic logic unit (ALU), which includes any arithmetic or Boolean combination of the three inputs, as well as mixed arithmetic and Boolean functions. (*TMS320C8x*)

ALU function modifier: For the parallel processor, a 4-bit code that specifies modifications to the functions performed by the arithmetic logic unit (ALU) data path (such as carry-in or multiple arithmetic). These function modifiers are specified in the opcode or in the D0 register, depending on the application. (*TMS320C8x*)

ALU operation: For the parallel processor, an action performed by the arithmetic logic unit (ALU) data path (that is, the result of the ALU function, the operation class, and any function modifiers). (*TMS320C8x*)

analog interface circuit (AIC): Integrated circuit that performs serial analog-to-digital (A/D) and digital-to-analog (D/A) conversions.

analog mixing: The mixing together of two analog signals; the multiplexing of two analog signals into one.

analog-to-digital (A/D): Conversion of continuously variable electrical signals to discrete or discontinuous electrical signals.

analog-to-digital (A/D) converter: A converter with internal sample-and-hold circuitry used to translate an analog signal to a digital signal.

ANSI: *American National Standards Institute*. An organization that establishes standards voluntarily followed by industries.

ANSI C: A version of the C programming language that conforms to the C standards defined by the American National Standards Institute (ANSI).

annul: Any instruction that is annulled does not complete its pipeline stages.

API: See *application programming interface*.

application programming interface (API): Used for proprietary application programs to interact with communications software or to conform to protocols from another vendor's product. (*TMS320C8x*)

AR0–AR7: *Auxiliary Registers 0–7*. Eight registers that are used as pointers to an address within the data space address range. The registers are operated on by the auxiliary register arithmetic unit (ARAU) and are selected by the auxiliary register pointer (ARP).

AR: See *auxiliary register*.

ARAU: See *auxiliary register arithmetic unit.*

ARB: See *auxiliary register pointer buffer*.

architecture: The software or hardware structure of all or part of a computer system; includes all the detailed components of the system.

archive library: A collection of individual files grouped into a single file by the archiver.

archiver: A software program that collects several individual files into a single file called an archive library. With the archiver, you can add, delete, extract, or replace members of the archive library.

ARCR: See *auxiliary register compare register*.

argument buffer: A memory block into which argument values are placed that accompany a command to a server parallel processor.

arithmetic logic unit (ALU): The section of the computer that carries out all arithmetic operations (addition, subtraction, multiplication, division, or comparison) and logic functions.

ARP: See *auxiliary register pointer.*

ARR: See *BSP address receive register*.

ARSR: *See asynchronous serial port receive shift register*.

ASCII: *American Standard Code for Information Interchange*, 1968. The standard set of 7-bit coded characters (8-bit including parity check) used for information interchange among data processing systems, communications systems, and associated equipment. The ASCII set consists of control characters and graphics characters.

ASIC: *Application-specific integrated circuit.*

ASPCR: See *asynchronous serial port control register*.

assemble: To prepare a machine-language program from a symbolic language program by substituting absolute operation codes for symbolic operation codes and absolute or relocatable addresses for symbolic addresses.

assembler: A software program that creates a machine-language program from a source file that contains assembly language instructions and directives. The assembler substitutes absolute operation codes for symbolic operation codes, and absolute or relocatable addresses for symbolic addresses.

assembly language: A low-level symbolic programming language, closely resembling machine code language and composed of groups of letters — each group representing a single instruction; allows a computer user to write a program using mnemonics instead of numeric instructions.

assembly language instructions: The language in which computer operations are represented by mnemonics.

assembly mode: A debugging mode that shows assembly language code in the DISASSEMBLY window and does not show the FILE window, no matter what type of code is currently running.

assembly optimizer: A software program that optimizes linear assembly code, which is assembly code that has not been register-allocated or scheduled. The assembly optimizer is automatically invoked with the shell program, cl6x, when one of the input files has a .sa extension. (*TMS320C6x*)

assembly-time constant: A symbol whose full definition is assigned at assembly time.

assert: To make a digital logic device pin active. If the pin is active low, then a low voltage on the pin asserts it. If the pin is active high, then a high voltage asserts it.

assignment statement: A statement that initializes a value to a variable.

asynchronous data transmit and receive register (ADTR): A register used by the on-chip asynchronous serial port. Data to transmit is written to the 8 least significant bits (LSBs) of the ADTR, and received data is read from the 8 LSBs of the ADTR. See also *asynchronous serial port receive shift register.* (*TMS320C2xx*)

asynchronous serial port control register (ASPCR): A 16-bit register used to control the on-chip asynchronous serial port; contains bits for setting port modes, enabling or disabling the automatic baud-rate detection logic, selecting the number of stop bits, enabling or disabling interrupts, setting the default level on the TX pin, configuring pins IO3–IO0, and resetting the port. (*TMS320C2xx*)

asynchronous serial port receive shift register (ARSR): A register in the on-chip asynchronous serial port that receives data from the RX pin one bit at a time. When full, ARSR transfers its data to the asynchronous data transmit and receive register (ADTR).

asynchronous serial port transmit shift register (AXSR): A 16-bit register in the asynchronous serial port that receives data from the asynchronous data transmit and receive (ADTR) register and transfers it one bit at a time to the asynchronous transmit (TX) pin. (*TMS320C2xx*)

asynchronous transmit (TX) pin: The pin on which data is transmitted serially from the asynchronous serial port; accepts a character one bit at a time from the asynchronous serial port transmit shift register (AXSR). (*TMS320C2xx*)

attribute: A parameter specifying some characteristic or feature to be applied to subsequent pictorial information.

audio breakout cable: A cable that connects the software development board (SDB) to audio input and output peripherals. It contains standard RCA jacks for stereo line-out, line-in, and auxiliary-in. (*TMS320C8x*)

autobuffering receiver enable (BRE) bit: A bit field that enables/disables the autobuffering receiver. At reset, BRE = 0. This bit is stored in the buffered serial port (BSP) control extension register (SPCE).

autobuffering receiver halt (HALTR) bit: A bit field that halts the autobuffering unit (ABU) when the boundaries of the buffer are crossed. At reset, HALTR = 0. This bit is stored in the buffered serial port (BSP) control extension register (SPCE).

autobuffering transmitter enable (BXE) bit: A bit field that enables/disables the autobuffering transmitter. At reset, BXE = 0. This bit is stored in the buffered serial port (BSP) control extension register (SPCE).

autobuffering transmitter halt (HALTX) bit: A bit field that halts the autobuffering unit (ABU) when the boundaries of the buffer are crossed. At reset, HALTX = 0. This bit is stored in the buffered serial port (BSP) control extension register (SPCE).

autobuffering unit (ABU): An on-chip module that allows the buffered serial port interface to read or write directly to internal memory independently of the central processing unit (CPU). Autobuffering capability can be separately enabled for transmit and receive sections. When autobuffering is disabled, the operation is similar to that of the standard serial port.

autocalibration: Automatic adjustment of a device so that the output is within a specific range for particular values of the input.

autoexec.bat: A batch file that contains DOS commands for initializing a PC.

autoinitialization: The process of initializing global C variables (contained in the .cinit section) before program execution begins.

autoinitialization at load time: An autoinitialization method used by the linker when linking C code. The linker uses this method when you invoke the linker with the –cr option. This method initializes variables at load time instead of runtime.

autoinitialization at runtime: An autoinitialization method used by the linker when linking C code. The linker uses this method when you invoke the linker with the –c option. The linker loads the .cinit section of data tables into memory, and variables are initialized at runtime.

auto mode: A context-sensitive debugging mode that automatically switches between showing assembly language code in the DISASSEMBLY window and C code in the FILE window, depending on what type of code is currently running.

auxiliary entry: The extra entry that a symbol may have in the symbol table which contains additional information about the symbol (whether it is a filename, a section name, a function name, etc.).

auxiliary register: A register that is used as a pointer to an address within the data-space address range. The register is operated on by the auxiliary register arithmetic unit (ARAU) and is selected by the auxiliary register pointer (ARP).

auxiliary register arithmetic unit (ARAU): An arithmetic unit used to increment, decrement, or compare the contents of the auxiliary registers. Its primary function is manipulating auxiliary register values for indirect addressing.

auxiliary register buffer (ARB) bits: A field that holds the previous value contained in the auxiliary register pointer (ARP). These bits are stored in status register 1.

auxiliary register compare register (ARCR): A memory-mapped register used as a limit to compare indirect addresses.

auxiliary register file bus (AFB): The bus on which the currently selected auxiliary register (AR) addresses the data memory location.

auxiliary register pointer (ARP): A field that selects the auxiliary register (AR) to use in indirect addressing. When the ARP is loaded, the previous ARP value is copied to the auxiliary register buffer (ARB). The ARP can be modified by memory-reference instructions when using indirect addressing, and by the MAR and LST instructions. These bits are stored in status register 0. *(TMS320C5x, TMS320C54x)*

auxiliary register pointer buffer (ARB): A field in the status register that holds the previous value of the auxiliary register pointer (ARP).

AVIS: See *address visibility (AVIS) bit*.

AXR: See *BSP address transmit register*.

AXSR: See *asynchronous serial port transmit shift register.*

B

B0: An on-chip block of dual-access RAM that can be configured as either data memory or program memory, depending on the value of the configuration control (CNF) bit in status register.

B1: An on-chip block of dual-access RAM available for data memory.

B2: An on-chip block of dual-access RAM available for data memory.

back porch: The interval of the video waveform between the end of synchronization and the corresponding blanking pulse. The horizontal back porch is specified as an integral number of frame clock (FCLK) periods; the vertical back porch is specified as an integral number of lines (half-lines for interlaced mode). See also *front porch*.

barrel rotator: A device that rotates the position of bits within a data word. It is similar to a barrel shifter except that bits shifted out are wrapped around to the vacated bits.

barrel shifter: A unit that rotates bits in a word. See also *POSTSCALER* and *PRESCALER*.

base: 1) A reference value. 2) A number that is multiplied by itself as many times as indicated by an exponent.

base set ALUs: The parallel processor's fundamental set of arithmetic logic unit (ALU) operations, which includes Boolean as well as mixed arithmetic and Boolean functions.

base set arithmetics: The fundamental set of parallel processor instructions that specify an arithmetic logic unit (ALU) arithmetic operation in the opcode. This set of instructions includes eleven class-independent arithmetic operations and six class-specific arithmetic operations.

base set Booleans: The fundamental set of parallel processor instructions that specify an arithmetic logic unit (ALU) Boolean operation in the opcode. This set of instructions includes the 256 possible Boolean functions.

batch file: One of two different types of files. One type contains DOS commands for the PC to execute. A second type of batch file contains debugger commands for the debugger to execute. The PC does not execute debugger batch files, and the debugger does not execute PC batch files.

baud-rate divisor register (BRD): A register for the asynchronous serial port that is used to set the serial port's baud rate. (*TMS320C2xx*)

BBS: *Bulletin board system.* A computer program which may be accessed by remote users through a modem, allowing them to post questions, view responses, and download files.

benchmarking: A type of program execution that allows you to track the number of CPU cycles consumed by a specific section of code.

BI bit: See *break interrupt (BI) bit*.

BIG bit: A field that specifies how the input/output (I/O) port wait-state register is mapped. This bit is stored in the wait-state control register (CWSR). At reset, BIG = 0.

big-endian: An addressing protocol in which bytes are numbered from left to right within a word. More significant bytes in a word have lower numbered addresses. Endian ordering is specific to hardware and is determined at reset. See also *little endian.*

binding: Associating or linking together two complementary software objects.

$\overline{\text{BIO}}$ pin: A general-purpose input pin that can be tested by conditional instructions that cause a branch when an external device drives $\overline{\text{BIO}}$ low.

bitBLT: *Bit-aligned block transfer*. Transfer of a block of pixels from one location in a bitmap to another.

bit detection: The special logic that supports leftmost-one, rightmost-one, leftmost-bit-change, and rightmost-bit-change detection.

bitmap: 1) A digital representation of an image in which bits are mapped to pixels. 2) A block of memory used to hold raster images in a device-specific format.

bit plane: A bit storage array (plane) used to store a particular bit of each pixel of an image. The 0 bit of each pixel is stored in bit plane 0, the first bit of each pixel is stored in bit plane 1, and so on. (*TMS320C8x*)

bit-reversed addressing: Addressing in which bits of an address are reversed in order to speed the processing of algorithms, such as Fourier transform algorithms.

bit-reversed indexed addressing: A method of indirect addressing that allows efficient I/O operations by resequencing the data points in a radix-2 fast Fourier transform (FFT) program. The direction of carry propagation in the auxiliary register arithmetic unit (ARAU) is reversed.

bits per pixel (BPP): The number of bits used to represent the color value of each pixel in a digitized image. (*TMS320C8x*)

BK: See *block-size register*.

BKR: See *BSP receive buffer size register*.

BKX: See *BSP transmit buffer size register*.

blanking: The process of extinguishing the scanning beam during horizontal and vertical retrace periods. See also *active time*; *blanking area*.

blanking area: The area of a display that is not active but rather blanked. No pixels are displayed in the blanking area. Vertical and horizontal retrace occur during blanking. See also *blanking pulse*.

blanking pulse: A positive or negative pulse developed during retrace, appearing at the end of each field; used to blank out scanning lines during the vertical or horizontal retrace interval. See also *blanking*.

blocked: The state of a task that is not ready to execute. A task can be blocked either by being suspended or by voluntarily choosing to wait for an event such as the arrival of a message or signal.

block miss: A cache miss in which the addressed block is not resident in the cache. The least recently used (LRU) algorithm determines which existing cache block is discarded. If the cache contains any modified data (master processor (MP) data cache only), then any modified subblocks are written back to external memory before the requested subblock is brought into cache.

block move address register (BMAR): A memory-mapped register that holds an address value for use with block moves or multiply/accumulates. *(TMS320C5x)*

block repeat active flag (BRAF) bit: A field that indicates a block repeat is currently active. This bit is normally set when the repeat block (RPTB) instruction is executed and is cleared when the block repeat counter register (BRCR) decrements below 0. Writing a 0 to this bit deactivates block repeat. At reset, BRAF = 0. This bit is stored in the processor mode status register for the TMS320C5x. (*TMS320C5x*)

block repeat counter register (BRC, BRCR): A register that specifies the number of times a block of code is to be repeated when a block repeat is performed.

block repeat program address end register (PAER, REA): A memory-mapped register that contains the end address of the segment of code being repeated.

block repeat program address start register (PASR, RSA): A memory-mapped register that contains the start address of the segment of code being repeated.

block-size register (BK): A register used for defining the length of a program block to be repeated in repeat mode.

block write: A nonstandard packet transfer that allows the transfer controller (TC) to perform multicolumn write operations.

BMAR: See *block move address register*.

BOB: See *byte ordering bit*.

boot: The process of loading a program into program memory.

boot loader: An on-chip program that loads and executes programs received from a host processor through standard memory devices (including EPROM), with and without handshake, or through the serial port to RAM at power up.

$\overline{\text{BOOT}}$ pin: The pin that enables the on-chip boot loader. When $\overline{\text{BOOT}}$ is held low, the processor executes the boot loader program after a hardware reset. When $\overline{\text{BOOT}}$ is held high, the processor skips execution of the boot loader and accesses off-chip program-memory at reset. (*TMS320C2xx, TMS320C24x*)

boundary scan: The use of scan registers on the border of a chip or section of logic to capture the pin states. By scanning these registers, all pin states can be transmitted through the JTAG port for analysis.

BPP: See *bits per pixel*.

$\overline{\text{BR}}$: See *bus request ($\overline{BR}$) pin*.

BRAF: See *block repeat active flag (BRAF) bit*.

branch: A switching of program control to a nonsequential program-memory address.

BRC: See *block repeat counter register*.

BRCR: See *block repeat counter register*.

BRD: See *baud-rate divisor register.*

BRE: See *autobuffering receiver enable (BRE) bit*.

break interrupt (BI) bit: A bit within the I/O status register (IOSR) that indicates when a break is detected on the asynchronous receive (RX) pin. (*TMS320C2xx*)

breakpoint: A place in a routine specified by an instruction, instruction digit, or other condition, where the routine may be interrupted by external intervention or by a monitor routine.

BRI: Basic rate service of Integrated Services Digital Network (ISDN), providing two B channels and one 16-Kbps D channel.

BSP: See *buffered serial port*.

BSP address receive register (ARR): A memory-mapped register that stores the address for writing a word to be transferred from the data receive register (DRR) to internal memory. When autobuffering is enabled (BRE = 1), the ARR is no longer available for software access as a memory-mapped register.

BSP address transmit register (AXR): A memory-mapped register that stores the address for reading a word to be transferred from internal memory to the data transmit register (DXR). When autobuffering is enabled (BXE = 1), the AXR is no longer available for software access as a memory-mapped register.

BSP control extension register (SPCE): A memory-mapped register that contains status and control bits for the buffered serial port (BSP) interface. The 10 least significant bits (LSBs) of the SPCE are dedicated to serial port interface control, whereas the 6 most significant bits (MSBs) are used for autobuffering unit (ABU) control.

BSP receive buffer size register (BKR): A memory-mapped register that stores the address block size for writing a word to be transferred from the data receive register (DRR) to internal memory. When autobuffering is enabled (BRE = 1), the BKR is no longer available for software access as a memory-mapped register.

BSP transmit buffer size register (BKX): A memory-mapped register that stores the address block size for reading a word to be transferred from internal memory to the data transmit register (DXR). When autobuffering is enabled (BXE = 1), the BKX is no longer available for software access as a memory-mapped register.

.bss section: One of the default common object file format (COFF) sections. Use the .bss directive to reserve a specified amount of space in the memory map that you can use later for storing data. The .bss section is uninitialized.

BTT: *Breakpoint/trace/timing*.

bubble: A pipeline cycle during which the transfer controller (TC) performs no operation. Bubbles occur because of contention, an insufficient amount of data for the next access, or simply an absence of requests for activity.

buffered serial port (BSP): An on-chip module that consists of a full-duplex, double-buffered serial port interface and an autobuffering unit (ABU). The double-buffered serial port of the BSP is an enhanced version of the standard serial port interface. The double-buffered serial port allows transfer of a continuous communication stream (8-,10-,12- or 16-bit data packets). Status and control of the BSP is specified in the BSP control extension register (SPCE).

buffer pool: See *message buffer pool*.

burst mode: A synchronous serial port mode in which a single word is transmitted following a frame synchronization pulse (FSX and FSR).

bus request ($\overline{BR}$) pin: The $\overline{BR}$ pin is tied to the $\overline{BR}$ signal, which is asserted when a global data memory access is initiated.

bus watching: The processor's ability to calculate and adjust for changes in address bus usage.

butterfly: A kernel function that computes an *n*-point fast Fourier transform (FFT), where *n* is a power of 2. The combinational pattern of inputs resembles butterfly wings.

BXE: See *autobuffering transmitter enable (BXE) bit*.

byte: Traditionally, a byte is a sequence of 8 adjacent bits operated upon as a unit. However, the TMS320C2x/C2xx/C5x byte is 16 bits.

By ANSI C definition, the *sizeof* operator yields the number of bytes required to store an object. ANSI further stipulates that when *sizeof* is applied to char, the result is 1. Since the TMS320C2x/C2xx/C5x char is 16 bits (to make it separately addressable), a byte is also 16 bits. This can yield unexpected results; for example, sizeof (int) = = 1 (not 2). TMS320C2x/C2xx/C5x bytes and words are equivalent (16 bits).

A byte is 32 bits for the TMS320C3x/C4x. On a parallel processor and the 'C6x, where the smallest addressable unit is 8 bits in length, the C definition corresponds to the traditional notion of an 8-bit byte.

byte ordering bit (BOB): A field that affects host processor data and address transfers when using the host port interface. Only the host processor can toggle this bit. The BOB must be initialized before the first data or address register access. This bit is stored in the host port interface control (HPIC) register.

C

C: A high-level, general-purpose programming language useful for writing compilers and operating systems and for programming microprocessors.

cache: A fast memory into which frequently used data or instructions from slower memory are copied for fast access. Fast access is facilitated by the cache's high speed and its on-chip proximity to the CPU.

cache block: A section of cache memory. Each block has an associated tag register and is divided into four subblocks. Cache memory is allocated in block-size portions, but cache servicing is performed at the subblock level, with subblocks brought in as needed.

cache clean: A master processor (MP) operation that updates external memory by writing modified (dirty) data-cache subblocks back to memory, thus resetting that subblock's dirty bit to 0. (*TMS320C8x*)

cache coherency: The state or condition in which the contents of one or more cache memories consistently and accurately represent the corresponding contents of the external memory.

cache flush: A master processor (MP) operation that updates external memory by writing modified (dirty) data-cache subblocks back to memory, thus resetting that subblock's present and dirty bits to 0.

cache hit: The state or condition in which the cache memory contains the requested instruction or data word.

cache miss: The state or condition in which the cache does not contain the requested instruction or data word.

cache subblock: One of four partitions of a cache block. Cache subblocks are the unit of memory brought into a cache on a subblock miss. Each subblock has a present bit (and a dirty bit for master processor (MP) data cache only) in the tag register for that block.

cache tag register: A register containing the address of the block whose subblock(s) have been copied into cache. It also contains a present bit for each subblock indicating whether or not the subblock is present in the cache. For master processor (MP) data cache, there is also a dirty bit for each subblock.

CAD: *Computer-aided design*.

CAD bit: See *calibrate A detect (CAD) bit*.

calibrate A detect (CAD) bit: A bit within the asynchronous serial port control register (ASPCR) that enables and disables the automatic baud-rate detection logic of the on-chip asynchronous serial port. (*TMS320C2xx*)

CALLS window: A window that lists the functions called by your program. (This window is part of the graphical user interface for all TI debuggers.)

CALU: See *central arithmetic logic unit*.

CAM: *Computer-aided manufacturing*.

capture mode: 1) A serial-register-transfer (SRT) mode during which an image is captured and stored into memory. Memory locations not corresponding to the captured image may be overwritten. See also *display mode; merge mode*. 2) A mode of the audio subsystem in which direct memory access (DMA) transfers read audio data that has been captured by the audio codec.

CAR1: See *circular buffer 1 auxiliary register (CAR1) bits*.

CAR2: See *circular buffer 2 auxiliary register (CAR2) bits*.

CAREA: See *composite area.*

carry bit: A bit in the status register used by the arithmetic logic unit (ALU) for extended arithmetic operations and accumulator shifts and rotates. The carry bit can be tested by conditional instructions.

carry flag: See *carry bit*.

$\overline{\text{CAS}}$: *Column address strobe*. A memory interface signal that drives the column address strobe inputs of DRAMs/VRAMs.

casting: A feature of C expressions that allows you to use one type of data as if it were a different type of data.

CBCR: See *circular buffer control register (CBCR)*.

CBER1: See *circular buffer 1 end register (CBER1)*.

CBER2: See *circular buffer 2 end register (CBER2)*.

C bit: See *carry bit.*

$\overline{\text{CBLNK}}$: See *composite blanking.*

CBSR1: See *circular buffer 1 start register*.

CBSR2: See *circular buffer 2 start register*.

CC: *Chip carrier*.

CCITT: *Consultative Committee for International Telephony and Telegraphy*.

C compiler: A software program that translates C source statements into assembly language source statements.

cDSP: *Configurable digital signal processor* or *customizable digital signal processor.*

CIO0–CIO3 bits: Bits within the asynchronous serial port control register (ASPCR) that individually configure pins IO0–IO3 as either inputs or outputs. For example, CIO0 configures the IO0 pin. See also *DIO0–DIO3 bits*; *IO0–IO3 bits*. (*TMS320C2xx)*

CE: *Chip enable*.

CENB1: See *circular buffer 1 enable (CENB1) bit*.

CENB2: See *circular buffer 2 enable (CENB2) bit*.

central arithmetic logic unit (CALU): The main arithmetic logic unit for the CPU that performs arithmetic and logic operations. It accepts a value for operations, and its output is held in the accumulator. (*TMS320C24x*)

central processing unit (CPU): The CPU is the portion of the processor involved in arithmetic, shifting, and Boolean logic operations, as well as the generation of data- and program-memory addresses. The CPU includes the central arithmetic logic unit (CALU), the multiplier, and the auxiliary register arithmetic unit (ARAU).

children: Additional windows opened for aggregate types that are members of a parent aggregate type displayed in an existing DISP window. (These windows are part of the standard graphical user interface for all TI debuggers.) See also *DISP window*.

chrominance: The National Television Standards Committee (NTSC) or phase alternation line (PAL) video signal contains two pieces that make up what you see on the screen: the black and white part (luminance) and the color part (chrominance). See also *luminance*. (*TMS320C8x*)

circular addressing: An addressing mode in which an auxiliary register is used to cycle through a range of addresses to create a circular buffer in memory. Also called modulo addressing.

circular buffer 1 auxiliary register (CAR1) bits: A field that identifies which auxiliary register (AR) is assigned to circular buffer 1. These bits are stored in the circular buffer control register (CBCR).

circular buffer 1 enable (CENB1) bit: A field that enables/disables circular buffer 1. At reset, CENB1 = 0. This bit is stored in the circular buffer control register (CBCR).

circular buffer 1 end register (CBER1): A memory-mapped register that indicates the circular buffer 1 end address.

circular buffer 1 start register (CBSR1): A memory-mapped register that indicates the circular buffer 1 start address.

circular buffer 2 auxiliary register (CAR2) bits: A field that identifies which auxiliary register (AR) is assigned to circular buffer 2. These bits are stored in the circular buffer control register (CBCR).

circular buffer 2 enable (CENB2) bit: A field that enables/disables circular buffer 2. At reset, CENB2 = 0. This bit is stored in the circular buffer control register (CBCR).

circular buffer 2 end register (CBER2): A memory-mapped register that indicates the circular buffer 2 end address.

circular buffer 2 start register (CBSR2): A memory-mapped register that indicates the circular buffer 2 start address.

circular buffer control register (CBCR): A memory-mapped register that enables/disables the circular buffers (CENB1 and CENB2 bits) and defines which auxiliary registers (CAR1 and CAR2 bits) are mapped to the circular buffers.

class: See *operation class*.

class-independent arithmetics: The parallel processor's eleven arithmetic logic unit (ALU) arithmetic functions in the base set of ALU operations that are available with any of the eight operation classes.

class-specific arithmetics: The parallel processor's arithmetic functions in the base set of arithmetic logic unit (ALU) operations that are available only for a subset of the eight operation classes.

client: A program or task that requests services from a server program or task.

CLK: A pseudoregister in the debugger that shows the number of CPU cycles consumed during benchmarking.

CLKDV: See *internal transmit clock division factor (CLKDV) bits*.

CLKIN: See *input clock signal*.

CLKMOD bit: See *clock mode (MCM) bit*.

CLKMOD pin: Determines whether the on-chip clock generator is running in the divide-by-two or multiply-by-two mode. See also *clock mode*. (*TMS320C209*)

CLKOUT1: See *master clock output signal*.

CLKOUT1 cycle: See *CPU cycle*.

CLKOUT1-pin control register: See *CLK register*.

CLKP: See *clock polarity (CLKP) bit*.

CLKR: See *receive clock input (CLKR) pin.*

CLK register: *CLKOUT1-pin control register.* A bit within this register determines whether the CLKOUT1 signal is available at the CLKOUT1 pin. (*TMS320C2xx, TMS320C24x*)

CLKX: See *transmit clock input/output (CLKX) pin*.

clock cycle: A cycle based on the input from the external clock.

clock mode (clock generator): One of the modes which sets the internal CPU clock frequency to a fraction or multiple of the frequency of the input clock signal CLKIN.

clock mode (MCM) bit: 1) A field that specifies the source of the clock for the transmit clock input/output (CLKX) pin. At reset, MCM = 0. This bit is stored in the serial port control register (SPC) and the time-division multiplexed (TDM) serial port control register (TSPC). 2) A bit within the synchronous serial port control register (SSPCR) that determines whether the source signal for clocking synchronous serial port transfers is external or internal. (*TMS320C2xx*)

clock mode (synchronous serial port): See *clock mode (MCM) bit*.

clock modes: Options used by the clock generator to change the internal CPU clock frequency to a fraction or multiple of the frequency of the input clock signal.

clock polarity (CLKP) bit: A field that indicates when the data is sampled by the receiver and sent by the transmitter. At reset, CLKP = 0. This bit is stored in the buffer serial port control extension register (SPCE).

CMOS: *Complementary metal oxide semiconductor.* A form of digital logic that is characterized by low power consumption, wide power supply range, and high noise immunity.

CNF bit: See *configuration control (CNF) bit*.

code: A set of instructions written to perform a task; a computer program or part of a program.

codec: *Coder-decoder*, or *compression/decompression*. A device that codes in one direction of transmission and decodes in another direction of transmission.

code-display windows: Windows that show code, text files, or code-specific information. This category includes the DISASSEMBLY, FILES, and CALLS windows. (These windows are part of the standard graphical user interface for all TI debuggers.)

code generator: A compiler tool that takes the file produced by the parser or the optimizer and produces an assembly language source file.

COFF: *Common object file format*. A binary object file format that promotes modular programming by supporting the concept of sections.

COFF magic number: A common object file format (COFF) file header entry that identifies the version of the common object file format or identifies the processor on which the module can be executed.

coherency: See *cache coherency*.

cold boot: The process of loading a program into program memory at power up.

COLMASK: *Column mask.* A control mask used by the serial register transfer (SRT) controller for address calculation.

command: A character string you provide to a system, such as an assembler, that represents a request for system action.

command descriptor block (CDB): A command block that is used to pass requests from an initiator to a target.

command file: A file created by the user which names initialization options and input files for the linker or the debugger.

command interpreter: A software routine that accepts commands from a client program or task and dispatches each command to the appropriate subroutine for execution.

command line: The portion of the COMMAND window where you can enter commands.

command-line cursor: An on-screen marker that identifies the current character position on the command line.

command-line interface: A method of communicating with a computer's operating system in which you type commands from a defined set into a specific location on the monitor display. Command-based systems are usually programmable.

COMMAND window: A window that provides an area for you to enter commands and for the debugger to echo command entry, show command output, and list progress or error messages.

comment: A source statement (or portion of a source statement) that documents or improves the readability of a source file. Comments are not compiled, assembled, or linked; they have no effect on the object file.

companded: *Compressed and expanded*. A quantization scheme for audio signals in which the input signal is compressed and then, after processing, is reconstructed at the output by expansion. There are two distinct companding schemes—A-law, used in Europe, and μ-law, used in the United States.

compiler: A translation program that converts a high-level language set of instructions into a target machine's assembly language.

composite area (CAREA): The signal generated by the frame timers that can be used to define a special area, such as an overscan boundary. This signal acts identically in both interlaced and noninterlaced modes, defining a purely rectangular region.

composite blanking ($\overline{\text{CBLNK}}$): A signal that combines information about the horizontal and vertical timing intervals into one signal that is more complex than either horizontal blanking ($\overline{\text{HBLNK}}$) or vertical blanking ($\overline{\text{VBLNK}}$). $\overline{\text{CBLNK}}$ can be used to disable pixel capture or display during horizontal and vertical retrace. See also *blanking pulse*.

composite synchronization ($\overline{\text{CSYNC}}$): A signal that combines information about the horizontal and vertical timing intervals into one signal that is more complex than either horizontal synchronization ($\overline{\text{HSYNC}}$) or vertical synchronization ($\overline{\text{VSYNC}}$). $\overline{\text{CSYNC}}$ can be used to enable retrace of the electron beam of a display screen that supports composite video.

composite video (CVBS): A signal that carries video picture information for color, brightness, and synchronization signals for both horizontal and vertical scans. (*TMS320C8x*)

composite video display: A display that receives all encoded video information in one signal. This information can include color, horizontal synchronization, vertical synchronization, or other information normally required by the National Television Standards Committee (NTSC) for television and video tape recording.

conditional processing: A method of processing one block of source code or an alternate block of source code, according to the evaluation of a specified expression.

conditional source: A source operand; either the odd or even register in a D register pair, depending on the negative status bit.

config.sys: A batch file that contains commands for initializing your PC.

configuration control (CNF) bit: A bit in the status register used to determine whether the on-chip RAM block is mapped to program space or data space. (*TMS320C24x, TMS320C5x*)

configured memory: Memory that is specified within the MEMORY directive of a linker command file and used by the linker for allocation of program code and data. (*TMS320C2x*, *TMS320C2xx*, *TMS320C5x*)

connect: A function used by an initiator to select a target to initiate an action.

connector: A hardware coupler that joins or connects a cable to a peripheral device for electronic communication. The software development board (SDB) has four connectors that connect cables from input/output peripherals to the board.

constant: A fixed or invariable value or data item that can be used as an operand.

contention: A situation where two or more devices or units attempt simultaneous accesses to the same resource.

context save/restore: A save and/or restore of system status (status registers, accumulator, product register, temporary register, hardware stack, auxiliary registers, etc.) when the device enters and/or exits a subroutine such as an interrupt service routine.

continuous mode: A synchronous serial port mode in which only one frame synchronization pulse is necessary to transmit or receive several consecutive packets at maximum frequency. See also *burst mode*.

control register: A mechanism for controlling and monitoring the operation of a device.

convolution: A time domain reference for digital filtering that makes extensive use of sum-of-products.

C optimizer: See *optimizer*.

counting semaphore: See *semaphore*.

CPU: See *central processing unit*.

CPU cycle: The period during which a particular execute packet is in a particular pipeline stage. CPU cycle boundaries always occur on clock cycle boundaries; however, memory stalls can cause CPU cycles to extend over multiple clock cycles.

CPU window: A window that displays the contents of on-chip registers, including the program counter, status register, and other registers. (This window is part of the standard graphical user interface for all TI debuggers.)

crossbar: A generally configurable, high-speed bus switching network for a multiprocessor system, permitting any of several processors to connect to any of several memory modules.

cross-reference lister: A debugging tool that accepts linked object files as input and produces cross-reference listings as output.

cross-reference listing: An output file created by the assembler that lists the symbols it defined, what line they were defined on, which lines referenced them, and their final values.

$\overline{\text{CSYNC}}$: See *composite synchronization*.

current AR: See *current auxiliary register*.

current auxiliary register (AR): The auxiliary register pointed to by the auxiliary register pointer (ARP). The auxiliary registers are AR0 (ARP = 0) through AR7 (ARP = 7). See also *auxiliary register*; *next auxiliary register*.

current data page: The data page indicated by the content of the data memory page pointer (DP). See also *data page*.

current-field cursor: A screen icon that identifies the current field in the active window.

CVBS: See *composite video*.

CWSR: See *wait-state control register*.

cycle: See CPU cycle.

D

D0–D*n*: External data bus pins that transfer data between the processor and external data/program memory or I/O devices.

D/A: See *digital-to-analog.*

DAB: See *direct-address bus*.

DAC: See *digital-to-analog converter*.

DARAM: *Dual-access RAM*. RAM that can be accessed twice in a single CPU clock cycle. For example, your code can read from and write to DARAM in the same clock cycle.

DARAM configuration (CNF) bit: See *configuration control (CNF) bit*.

.data section: One of the default common object file format (COFF) sections. The .data section is an initialized section that contains initialized data. You can use the .data directive to assemble code into the .data section.

data-address generation logic: Logic circuitry that generates the addresses for data memory reads and writes. This circuitry, which includes the auxiliary registers and the auxiliary register arithmetic unit (ARAU), can generate one address per machine cycle.

data bus: A group of connections used to route data.

data cache: The master processor's (MP) two SRAM banks that hold cached data needed by the MP. Data RAMs for the parallel processors are not cached. See also *SRAM banks*.

data cache reset (DCR): A command you send with the master processor cmnd instruction that resets all data cache tag registers and the data least recently used (DLRU) register.

data-display windows: Windows for observing and modifying various types of data. This category includes the MEMORY, CPU, DISP, and WATCH windows. (These windows are part of the standard graphical user interface for all TI debuggers.)

data memory: A memory region used for storing and manipulating data.

data memory address (dma) bits: The 7 least significant bits (LSBs) of a direct addressed instruction that contains the immediate relative address within a 128-word data page. The 7 LSBs are concatenated with the data memory page pointer (DP) to form the direct memory address of 16 bits. See also *data memory page pointer (DP) bits*.

data memory page pointer (DP) bits: A bit field that specifies the current data memory page address. The DP bits are concatenated with the least significant bits (LSBs) of the instruction word to form the direct memory address. These bits are stored in status register 0 (ST0). (*TMS320C3x*, *TMS320C4x*, *TMS320C5x*)

data memory page 0: The first page in data memory space where the memory-mapped registers and the scratch-pad RAM block (B2) reside.

data page: A contiguous block in data memory. Fixed-point devices contain a block of 128 words in data memory. Data memory contains 512 data pages. Data page 0 is the first page of data memory (addresses 0000h–007Fh); data page 511 is the last page (addresses FF80h–FFFFh). In floating-point devices, data pages are 64K words long. The ’C3x has a total of 256 pages; the ’C4x has a total of 64K (65,536) pages. See also *direct addressing*.

data RAM: On-chip RAM that is available for the general-purpose storage of data by the master processor or parallel processors. (*TMS320C8x*)

data-read address bus (DRAB): An internal bus that carries the address for each read from data memory. *(TMS320C24x*)

data read bus (DRDB): An internal bus that carries data from data memory to the central arithmetic logic unit (CALU) and the auxiliary register arithmetic unit (ARAU). (*TMS320C24x*)

data receive register (DRR): A memory-mapped register that holds serial data copied from the receive shift register (RSR). When autobuffering is enabled (BRE = 1), the DRR is no longer available for software access as a memory-mapped register. See also *data receive shift register (RSR)*.

data receive shift register (RSR): A register that holds serial data received from the serial data receive (DR) pin. See also *data receive register (DRR)*.

data size: The number of bits (8, 16, 24, 32, or 40) used to represent a particular number.

data-space wait-state (DSWS) bit(s): A value in the wait-state generator control register (WSGR) that determines the number of wait states applied to reads from and writes to off-chip data space. (*TMS320C24x*)

data terminal ready (DTR): A signal defined by the IEEE RS-232 serial standard that allows a data source, such as a computer or terminal, to indicate that it is ready for transmission.

data transmit register (DXR): A memory-mapped register that holds serial data to be copied to the data transmit shift register (XSR). When autobuffering is enabled (BXE = 1), the DXR is no longer available for software access as a memory-mapped register. See also *data transmit shift register (XSR)*.

data transmit shift register (XSR): A register that holds serial data to be transmitted from the serial data transmit (DX) pin (or from the time-division multiplexed data transmit (TDX) pin when TDM = 1). See also *data transmit register (DXR)* and *TDM data transmit register (TDXR)*.

data unit: The parallel processor's data manipulation hardware unit that includes the arithmetic logic unit (ALU), the multiplier, the mf expander, and the barrel rotator.

data unit operation: For the parallel processor, the operations performed by the hardware in the data unit. The data unit allows both a multiply and an arithmetic logic unit (ALU) data path operation to be performed in a single cycle.

data write bus (DWEB): An internal bus that carries data to both program memory and data memory.

dba: The assembler keyword for the parallel processor-relative base address to local RAM0 (LRAM0) (0x#000 where # is the parallel processor identification number). The dba keyword is used to generate addresses in parallel processor-independent code.

DBMR: See *dynamic bit manipulation register*.

dcache: See *data cache*.

DCR: See *data-cache reset*.

DCT: See *discrete cosine transform.*

D_DIR: An environment variable that identifies the directory containing the commands and files necessary for running the debugger.

DEA: See *direct external access.*

deassert: To make a digital logic device pin inactive. If the pin is active low, then a high voltage on the pin deasserts it. If the pin is active high, then a low voltage deasserts it.

debugger: A software interface used to identify and eliminate mistakes in a program.

decode phase: The phase of the pipeline in which the instruction is decoded. See also *pipeline*.

default task: The task that runs when no other task is ready to run.

delay slot: A CPU cycle that occurs after the first execution phase (E1) of an instruction in which results from the instruction are not available. (*TMS320C62xx*)

delta-guided transfer: A type of guided packet transfer in which the guide table consists of delta values to be added to the starting address of the previous two-dimensional patch to form the starting address of the new patch. See also *guided transfer*.

delta interrupt: An asynchronous serial port interrupt (TXRXINT) that is generated if a change takes place on one of the general-purpose I/O pins (IO0, IO1, IO2, or IO3).

delta-interrupt mask (DIM) bit: A bit within the asynchronous serial port control register (ASPCR) which enables and disables delta-detect. The delta-detect function allows or prevents interrupts from being generated by changes on the I/O pins.

denormal: A floating-point number with a zero exponent and a nonzero mantissa.

destination controller: One of two independent controllers within the transfer controller (TC) that handle packet transfers. The destination controller generates the addresses needed to write packet data into the destination memory area.

destination port: The message port to which a message is sent. See also *port ID*.

detect complete (ADC) bit: A bit within the I/O status register (IOSR); a flag bit used in the implementation of automatic baud-rate detection in the asynchronous serial port. (*TMS320C2xx*)

device driver: Software that enables computer hardware to communicate with a device. A device driver may also translate data and call other drivers to actually send data to a device. The software development board (SDB) uses a device driver for Windows NT to ensure communication between the host and the SDB.

Dhrystones: An algorithm used to benchmark processor performance.

DIE: See *DMA interrupt enable register*.

digital loopback (DLB) mode: A synchronous serial port test mode in which the receive pins are connected internally to the transmit pins on the same device. This mode, enabled or disabled by the DLB bit, allows you to test whether the port is operating correctly.

digital loopback (DLB) bit: A field that puts the serial port in digital loopback mode. At reset, DLB = 0. This bit is stored in the serial port control (SPC) register and the time-division multiplexed (TDM) serial port control (TSPC) register.

digital mixing: The mixing together of two digital signals into one; the algebraic sum of two digital signals. *(TMS320C8x*)

digital signal processor (DSP): A semiconductor that turns analog signals—such as sound or light—into digital signals, which are discrete or discontinuous electrical impulses, so that they can be manipulated.

digital-to-analog (D/A): Conversion of discrete or discontinuous electrical signals to continuously variable signals. See also *digital-to-analog converter*.

digital-to-analog converter (DAC): A device that converts a signal represented by a series of numbers (digital) to a continuously varying signal (analog). See also *digital-to-analog*.

digitizer: The part of the video capture front end that converts the analog video signal into a digital signal to be decoded.

DIM: See *delta-interrupt mask (DIM) bit*.

dimensioned transfer: A transfer consisting of sources and/or destinations that can be a simple contiguous linear sequence of data bytes or can consist of a number of such regions. See also *guided transfer*.

DIN: *Deutsch Industrie Norm.* Germany's national standards organization that controls the specifications for a system of plugs, cables, and sockets used for audio signaling equipment.

DIN connector: A type of connector that is in accordance with the German national standard organization (Deutsch Industrie Norm - DIN) and is sometimes used in computer and audio connections. The most common is the PC keyboard connector. See also *mini-DIN connector*.

DIO0–DIO3 bits: Bits within the I/O status register (IOSR). These bits are used to track a change from a previous known or unknown signal value at the corresponding I/O pin (IO0–IO3) when the asynchronous serial port is enabled (that is, when the reset asynchronous serial port (URST) bit of the asynchronous serial port control register (ASPCR) is 1). For example, DIO0 indicates a change on the IO0 pin. See also *CIO0–CIO3 bits*; *IO0–IO3 bits*. (*TMS320C2xx*)

DIP: See *dual in-line package*.

direct address bus (DAB): A bus that provides the data address used by the central processing unit (CPU).

direct addressing: One of the methods used by an instruction to address data-memory. In direct addressing, the data-page pointer (DP) holds the 9 most significant bits (MSBs) of the address (the current data page), and the instruction word provides the 7 least significant bits (LSBs) of the address (the offset). See also *indirect addressing*.

direct call: A function call where one function calls another using the function's name.

direct external access (DEA): A method of accessing off-chip (external) memory without having to issue a packet transfer request to the tranfer controller (TC).

directive: A special-purpose command that controls the actions and functions of a software tool.

direct memory access (DMA): A mechanism whereby a device other than the host processor contends for, and receives, mastery of the memory bus so that data transfers can take place independent of the host.

dirty flag: A storage bit associated with each subblock of master processor data-cache memory that indicates whether the subblock contains modified data that needs to be written back to main memory.

disambiguation: See *alias disambiguation*.

disassembly: The process of translating the contents of memory from machine language to assembly language (also known as reverse assembly).

DISASSEMBLY window: A window that displays the disassembly of memory contents.

disconnect: A function to cause a target to release the SCSI bus control (the SCSI bus is placed into the BUS FREE phase).

discontinuity: A state in which the addresses fetched by the debugger become nonsequential as a result of instructions that load the PC with new values, such as branches, calls, and returns.

discrete cosine transform (DCT): A fast Fourier transform used in manipulating compressed still and moving picture data. See also *fast Fourier transform; JPEG standard*.

display area: The portion of the COMMAND window or parallel debug manager (PDM) window where the debugger/PDM echoes command entry, shows command output, and lists progress or error messages.

display mode: A serial-register-transfer (SRT) mode during which information is transferred from the frame memory to the display device. See also *capture mode; merge mode*.

DISP window: A window that displays the members of an aggregate data type. (This window is part of the standard graphical user interface for all TI debuggers.)

DIV2/DIV1: Two pins used together to determine the clock mode of the ’C2xx/’C24x clock generator (÷2, ×1, ×2, or ×4). (The ’C209 uses the CLKMOD pin and has only two clock modes, ÷2 and ×2.) (*TMS320C2xx, TMS320C24x*)

divide-down value: The value in the timer divide-down register (TDDR). This value is the prescale count for the on-chip timer. The larger the divide-down value, the slower the timer interrupt rate.

DLB: See *digital loopback mode (DLB) bit*.

DLRU: *Data least recently used*.

DMA: See *direct memory access (DMA)* or *data memory address*.

DMA controller: See *DMA coprocessor.*

DMA coprocessor: A peripheral that transfers the contents of memory locations independently of the processor (except for initialization). (*TMS320C4x*)

DMA interrupt enable (DIE) register: A register (in the CPU register file) that controls which interrupts the DMA coprocessor responds to.

DMA mode: *Direct memory access mode*. A mode of the audio subsystem in which a DMA transfer reads audio data that has been captured by the audio codec or in which a DMA transfer supplies audio data for playback. Simultaneous DMA capture and playback is not possible.

D_OPTIONS: An environment variable that you can use for identifying often-used debugger options.

DOS/4GW: A memory extender that is bound with the MS-DOS version of the fixed-point and floating-point DSP tools. You may see this term when invoking the code generation tools.

DOS/16M: The executable filename for a tool that is embedded in the TMS320C3x/C4x code generation tools. You may occasionally see this term in an error message.

dot clock: The clock that cycles the rate at which video data is output to a display monitor. *(TMS320C8x*)

double buffering: A method of using dual buffers to achieve efficient one-way data transmission between two processors or between a processor and a peripheral device. Each buffer is a block of storage through which data is transmitted from one processor (or device) to the other. The receiving processor reads the transmitted data from one buffer while the sending processor simultaneously prepares the data for the next transmission in the alternate buffer.

double-precision floating-point: A floating-point number with 64 bits plus an additional hidden bit.

doubleword: A 64-bit value.

DP: See *data memory page pointer (DP).*

DRAB: See *data-read address bus*.

DRAM: See *dynamic random-access memory*.

DR bit: *Data ready indicator for the receiver.* A bit that is automatically reset to 0 when the receive register is read or when the device is reset.

DRDB: See *data read bus (DRDB).*

DR pin: See *serial data receive (DR) pin.*

driver: See *device driver*.

DRR: See *data receive register (DRR)*.

$\overline{\text{DS}}$: *Data memory select pin*. The DSP asserts $\overline{\text{DS}}$ to indicate an access to external data memory (local or global).

DSK: *Digital signal processor (DSP) starter kit.* Tools and documentation provided to new DSP users to enable rapid use of the product.

DSP: See *digital signal processor.*

DSPINT: See *DSP interrupt (DSPINT) bit*.

DSP interrupt (DSPINT) bit: A field that enables and/or disables an interrupt from a host processor to the DSP. The DSPINT bit is written from the host processor; a DSP write has no effect on the DSPINT bit. When DSPINT = 1, a DSP interrupt is generated. The host must write a 0 to the DSPINT bit while writing to the byte ordering bit (BOB) or DSP-to-host processor interrupt (HINT) bit, so that the host does not provoke an unwanted DSP interrupt. This bit is stored in the host port interface control (HPIC) register.

D_SRC: An environment variable that identifies directories containing program source files. (This is a standard part of the TI debugger environment.)

DSWS: See *data-space wait-state (DSWS) bit(s).*

DTR: See *data terminal ready*.

dual in-line package (DIP): A common rectangular chip housing with leads (pins) on both long sides.

dummy cycle: A CPU cycle in which the CPU reloads the program counter with the same address.

DWAB: See *data-write address bus*.

DWEB: See *data write bus*.

DX pin: See *serial data transmit (DX) pin*.

DXR: See *data transmit register*.

dynamic bit manipulation register (DBMR): A memory-mapped register that masks the input to the parallel logic unit (PLU) in the absence of a long immediate value.

dynamic memory allocation: A technique used by several functions (such as malloc, calloc, and realloc) to dynamically allocate memory for variables at runtime. This is accomplished by defining a large memory pool (heap) and using the functions to allocate memory from the heap.

dynamic random-access memory (DRAM): Memory typically used for external memory. A special memory circuit that is dynamic in nature; it requires each bit of information to be refreshed, or restored to its programmed state, on a periodic basis to maintain valid data.

E

EALU: See *extended arithmetic logic unit*.

EALU||ROTATE: The parallel processor's extended arithmetic logic unit (EALU) variation that allows you to save the result of the barrel rotation to an additional destination register. (*TMS320C8x*)

EGA: *Enhanced Graphics Adaptor.* An industry standard for video cards.

EISA: *Extended Industry Standard Architecture.* An industry standard for PC buses.

EMI: *Electromagnetic interference*.

EMIF: *External memory interface*.

EMIF CE space: One of the four memory spaces defined by a chip enable on the EMIF.

emulator: A debugging tool that is external to the target system and provides direct control over the TMS320 processor that is on the target system.

emurst: A debugger utility that resets the emulator.

enable extra index register (NDX) bit: A field that determines if a modification or write to auxiliary register 0 (AR0) also modifies or writes to the index register (INDX) and the auxiliary register compare register (ARCR) to maintain compatibility with the TMS320C2x. This bit is stored in the processor mode status register (PMST).

enable multiple TREGs (TRM) bit: A field that indicates if a load TREG0 (LT/A/D/P/S) instruction loads only temporary register 0 (TREG0) or loads all three of the temporary registers (TREG0, TREG1, and TREG2) to maintain compatibility with the TMS320C2x. The TRM bit allows the TMS320C5x to operate in either 'C2x-compatible mode (TRM = 0) or 'C5x-enhanced mode (TRM = 1) in conjunction with the use of TREG0, TREG1, and TREG2. The TRM bit affects the operation of all 'C2x-compatible instructions that modify TREG0. This bit is stored in the processor mode status register (PMST). (*TMS320C5x*)

entry point: A point in target memory where the program begins execution.

environment variable: 1) A special system symbol that the debugger uses for finding directories or obtaining debugger options. 2) A system symbol that can be used to modify command-line input for the assembler or linker, or to modify the environment. 3) System symbols that you define and assign to a string. They are often included in batch files, for example, .cshrc.

epilog: The portion of code in a function that restores the stack and returns. See also *pipelined-loop epilog*.

EPROM: See *erasable programmable read-only memory*.

erasable programmable read-only memory (EPROM): A read-only memory in which stored data can be erased by ultraviolet light or other means. It is reprogrammed bit by bit with appropriate voltage pulses.

event: A stimulus that can cause a task to begin executing.

event flag: A bit in memory that is bound to either a port or a semaphore and that indicates whether a specific event has taken place.

event pin: A pin on the software development board (SDB) interrupt controller that triggers an event when asserted. (*TMS320C8x*)

event register: A field in a task descriptor that contains the associated task's 32 event flags.

EVM: *Evaluation module*.

EVRC: *Enhanced variable-rate voice coder*.

exception: A condition that is handled outside the normal program flow of a task. An exception in a task is the software equivalent of a hardware interrupt in a processor.

exception flag: A bit in a task's exception register that indicates the status of a particular type of exception.

exception handler: A function associated with a task that handles exceptions raised in that task. The manner in which an exception handler responds to an exception in a task is analogous to the way an interrupt service routine (ISR) responds to a hardware interrupt in a processor.

exception register: A field in a task descriptor that contains the associated task's 32 exception flags.

executable module: A linked object file that can be executed in a target system.

execute packet: A block of instructions that execute in parallel.

execute phase: The final phase of a multi-phase processor pipeline; the phase in which an instruction is executed. See also *pipeline*.

execute stage: The second stage of the master processor's fetch, execute, access (FEA) pipeline and the third stage of the parallel processor's fetch, address, execute (FAE) pipeline. These stages operate differently for the master processor and the parallel processors. For the master processor's execute stage, the instruction is decoded, source operands are read from the registers, the operation is performed, and the results are written into the destination register. For the parallel processor, all data unit operations occur, as well as memory accesses (loads and stores) and register-to-register moves. (*TMS320C8x*)

executive: The portion of a multitasking software system that is responsible for executing application tasks, providing communications among tasks, and managing shared resources.

exit-list: A list of functions that are executed by the kernel each time a task exits.

expander: For the parallel processor, the arithmetic logic unit (ALU) data path hardware that expands 1-, 2-, or 4-bit values by respectively duplicating each bit by 32, 16, or 8 times to expand the bit(s) out to a 32-bit word. The value to be expanded can be contained in the multiple flags (mf) register, the only register connected to the parallel processor's expander.

expression: One or more operations in assembler programming represented by a combination of symbols, constants, and paired parentheses separated by arithmetic operators.

extended arithmetic logic unit (EALU): The parallel processor's set of operations that extend the normal arithmetic logic unit (ALU) functions by specifying the ALU operation and/or multiplier features in the D0 register instead of in the opcode.

extended-precision floating-point format: A 40-bit representation of a floating-point number with a 32-bit mantissa and an 8-bit exponent.

extended-precision register: A 40-bit register used primarily for extended-precision floating-point calculations. Floating-point operations use bits 39–0 of an extended-precision register. Integer operations, however, use only bits 31–0.

external access active strobe ($\overline{\text{STRB}}$): $\overline{\text{STRB}}$ is asserted during accesses to external program, data, or I/O space.

external address: See *off-chip address.*

external flag (XF) pin: A general-purpose output pin whose status can be read or changed by way of the XF bit in status register ST1. (*TMS320C2xx*, *TMS320C24x, TMS320C5x, TMS320C54x*)

external flag (XF) pin status bit: 1) A field that drives the level of the external flag (XF) pin. At reset, XF = 1. This bit is stored in status register 1. (*TMS320C2xx, TMS320C24x, TMS320C5x, TMS320C54x*)

external interrupt: A hardware interrupt triggered by a specific value on a pin.

externally initiated packet transfer (XPT): A packet transfer initiated by an external device through the ’C8x’s $\overline{\text{XPT}}$ [2:0] inputs. (*TMS320C8x*)

external symbol: A symbol that is either 1) defined in the current module and accessed in another, or 2) accessed in the current module but defined in another.

F

FAE pipeline sequence: *Fetch, address, execute pipeline sequence.* The instruction-execution unit pipeline for the parallel processor. The fetch stage includes instruction and operand fetch; the address stage includes address computation and possible crossbar access; and the execute stage includes data unit operations, memory accesses, and register-to-register moves. (*TMS320C8x*)

fast Fourier transform (FFT): An efficient method of computing the discrete Fourier transform algorithm, which transforms functions between the time domain and frequency domain. The time-to-frequency domain is called the forward transform, and the frequency-to-time domain is called the inverse transformation.

fast mode: A master processor (MP) floating-point unit mode in which MP floating-point instructions are executed with all denormals treated as 0 for both input operands and the output result.

fault: Any condition that causes a system to fail.

FCLK: *Frame clock*. The clock that controls the internal video logic of the video controller's frame timers. (*TMS320C8x*)

FE: See *format extension (FE) bit*.

FEA pipeline sequence: *Fetch, execute, access pipeline sequence.* The instruction-execution integer unit pipeline for the master processor. The fetch stage includes instruction and operand fetch; the execute stage includes operations and register-to-register moves; and the optional access stage includes memory accesses (loads and stores).

FE bit: *Framing error indicator bit*. A bit within the I/O status register (IOSR) that indicates whether a valid stop bit has been detected during the reception of a character into the asynchronous serial port. (*TMS320C2xx)*

fetch: That portion of a computer cycle during which the next instruction is retrieved from memory.

fetch packet: A block of program data containing up to 8 instructions.

fetch stage: The first stage of the master processor's fetch, execute, access (FEA) pipeline and the parallel processor's fetch, address, execute (FAE) pipeline, during which instructions and their operands are fetched. See also *FEA pipeline sequence* or *FAE pipeline sequence*.

FFT: See *fast Fourier transform*.

field: A software-configurable data type which can be programmed to be from 1 to 8 bits long.

field extract move: A parallel processor's register-to-register move that right-justifies a specified byte or halfword from the source register and writes the result with a 0 or sign extension to the destination register. The source register must be a D register, while the destination register can be any parallel processor register.

field replicate move: A parallel processor's register-to-register move that replicates the lower byte or halfword in the source register to fill 32 bits and writes the result to the destination register. The source register must be a D register, while the destination register can be any register.

FIFO: *First in, first out*. A queue; a data structure or hardware buffer from which items are taken out in the same order they were put in. A FIFO is useful for buffering a stream of data between a sender and receiver which are not synchronized; that is, the sender and receiver are not sending and receiving at exactly the same rate. If the rates differ by too much in one direction for too long, the FIFO becomes either full (blocking the sender) or empty (blocking the receiver). *(TMS320C8x, TMS320C4x*)

FIFO buffer: *First-in, first-out buffer.* A portion of memory in which data is stored and then retrieved in the same order in which it was stored. The synchronous serial port has two four-word-deep FIFO buffers: one for its transmit operation and one for its receive operation. (*TMS320C24x*)

FIFO flag: Indicator that gets set or cleared depending on the state of the FIFO. (*TMS320C8x)*

FIFO status register: A register located within a FIFO device used to store status information regarding the device. *(TMS320C8x*)

FIG: See *frame ignore (FIG) bit*.

file header: A portion of the common object file format (COFF) object file that contains general information about the object file, such as the number of section headers, the type of system the object file can be downloaded to, the number of symbols in the symbol table, and the symbol table's starting address.

file-level optimization: A level of optimization where the compiler uses the information that it has about the entire file to optimize your code (as opposed to program-level optimization, where the compiler uses information that it has about the entire program to optimize your code).

FILE window: A window that displays the contents of the current C code. The FILE window is intended primarily for displaying C code but can be used to display any text file. (This window is part of the standard graphical user interface for all TI debuggers.)

fill-with-value transfer: A type of source transfer that does not transfer data but instead specifies a source value within the packet transfer parameters. This fill value is used to fill the destination memory as defined by the destination transfer parameters.

FIR: *Finite impulse response*.

fixed-patch guided transfer: Guided transfer that uses an on-chip guide table consisting of 32-bit word-aligned entries. See also *guided transfer*.

flag: A binary status indicator whose state indicates whether a particular condition has occurred or is in effect.

flag offsets: The offset into a FIFO memory device that determines when FIFO flags get set or cleared.

flash memory: Nonvolatile read-only memory that is electronically erasable and programmable.

floating-point add unit busy: A condition in which the floating-point add unit is stalled or its pipeline is full; therefore, the unit cannot accept a new instruction.

floating-point empty: A condition in which there are no instructions in any of the pipeline stages of the floating-point unit.

floating-point exception handler routine: A routine used to service master processor floating-point exception traps in an effort to provide information to the user or to attempt recovery.

floating-point multiply unit busy: A condition in which the master processor's floating-point multiply unit is stalled or its pipeline is full; therefore, the unit cannot accept a new instruction.

floating-point unit (FPU): The master processor's IEEE standard 754 hardware that consists of a full double-precision floating-point add unit and a double-precision floating-point multiply unit with a single precision core.

flush: See *cache flush*.

FMV: *Full motion video*.

FO: See *format (FO) bit*.

FPU: See *floating-point unit*.

foreign node: A processor node other than the one in which the executable code for a particular task resides. This term is relative. A task that executes on a particular node *n* considers this node its local node, but tasks that execute on other nodes consider node *n* to be a foreign node.

format (FO) bit: A field that specifies the word length of the serial port transmitter and receiver. The data is transferred with the most significant bit (MSB) first. At reset, FO = 0. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC).

format extension (FE) bit: A field used in conjunction with the format (FO) bit to specify the word length of the buffered serial port (BSP) transmitter and receiver. When FO = FE = 00, the format is 16-bit words; when FO = FE = 01, the format is 10-bit words; when FO = FE = 10, the format is 8-bit words; and when FO = FE = 11, the format is 12-bit words. For 8-,10-, and 12-bit words, the received words are right-justified and the sign bit is extended to form a 16-bit word. The words to transmit must be right-justified. At reset, FE = 0. This bit is stored in the BSP control extension register (SPCE).

FR0/FR1: *FIFO receive-interrupt bits*. Bits within the synchronous serial port control register (SSPCR) which set an interrupt trigger condition based on the number of words in the receive FIFO buffer. (*TMS320C2xx*)

frame: The screen image output during a single vertical sweep.

frame ignore (FIG) bit: A field used only in transmit continuous mode with external frame and in receive continuous mode. At reset, FIG = 0. This bit is stored in the BSP control extension register (SPCE).

frame lock: Video controller (VC) mode that allows the two frame timers to be locked together so that they are synchronous. This is useful when different timing signal parameters are required in the capture and display systems, but where it is otherwise desirable to coordinate the two.

frame synchronization mode (FSM) bit: A field that specifies whether frame synchronization pulses (FSX and FSR) are required for serial port operation. At reset, FSM = 0. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC).

frame synchronization polarity (FSP) bit: A field that determines the status of the frame synchronization pulses. At reset, FSP = 0. This bit is stored in the BSP control extension register (SPCE).

frame synchronization (frame sync) mode: One of two modes in the synchronous serial port that determine whether frame synchronization pulses are necessary between consecutive data transfers. See also *burst mode*; *continuous mode*.

frame synchronization (frame sync) pulse: A pulse that signals the start of a transmission from or reception into the synchronous serial port.

frame timer: A timer In the video controller (VC) that provides video timing control and indicates to the serial register transfer (SRT) controller when an SRT is necessary. (*TMS320C8x*)

framing error: An error that occurs when a data character received by the asynchronous serial port does not have a valid stop bit. See also *FE bit*.

Free bit: A field used in conjunction with the Soft bit to determine the state of the serial port or timer when a breakpoint is encountered in the high-level language debugger. At reset, Free = 0. *(TMS320C2xx*)

front porch: The interval of a video waveform between the start of blanking and the corresponding sync pulse. The horizontal front porch is specified as an integral number of frame clock (FCLK) periods; the vertical front porch is specified as an integral number of lines (halflines for interlaced mode). See also *back porch*.

FSM: See *frame synchronization mode (FSM) bit*.

FSM bit: A bit within the synchronous serial port control register (SSPCR) that determines the frame synchronization mode for the synchronous serial port. See also *burst mode*; *continuous mode*.

FSP: See *frame synchronization polarity (FSP) bit*.

FSR pin: See *receive frame synchronization pin.*

FSX pin: *Transmit frame synchronization pin.*

FT0/FT1: *FIFO transmit-interrupt bits.* Bits within the synchronous serial port control register (SSPCR) which set an interrupt trigger condition based on the number of words in the transmit FIFO buffer. (*TMS320C2xx*)

function inlining: Process of inserting code for a function at the point of call. This saves the overhead of a function call, and allows the optimizer to optimize the function in the context of the surrounding code.

G

gain stage: That portion of a circuit that increases a signal; also that portion of an algorithm that imposes a gain onto a digital signal. (*TMS320C8x*)

GBC: *Global bus controller*.

general-purpose input/output pins: Pins that can be used to accept input signals and/or send output signals but are not linked to specific uses.

global address unit: Parallel processor hardware that generates addresses using a global address register (a8 – a12, a14, a15) with preaddition, postaddition, presubtraction, or postsubtraction of a global index register (x8 – x10) or an immediate offset.

global-data memory space: One of four memory spaces. The global-data memory space can either share data with other processors within the system or serve as additional data-memory space.

global interrupt enable (GIE): A bit in the control status register (CSR) used to enable or disable maskable interrupts. (*TMS320C62xx*)

global legal: A parallel processor's access that can be performed over the global port because the address is in the shared RAMs. If an access is not globally legal, a direct external access (DEA) is performed by the transfer controller (TC). The parallel processor's pipeline stalls until the DEA is completed.

global memory allocation register (GREG): A memory-mapped register used for specifying the size of the global data memory. Addresses not allocated by the GREG for global data memory are available for local data memory.

global port: The data port with access to any of the shared RAMs (any parallel processor data RAM or parameter RAM).

global symbol: A symbol that is either 1) defined in the current module and accessed in another or 2) accessed in the current module but defined in another.

global transfer: A parallel processor's operation performed by the global address unit. This can be either a memory access (load or store), an address unit arithmetic, or a register-to-register move.

GMICR: *Global memory interface control register*.

GP: *General purpose*.

graphical user interface (GUI): A screen format that provides windows, menus, dialog boxes, icons, lists, and options that allow you to start a program or perform a task by pointing to a pictorial representation, selecting an item using a mouse, or using a keyboard.

graphics output monitor cable: The cable provided by a monitor manufacturer that connects a video graphics array (VGA) source to the monitor.

grayscale: Or *greyscale*. A range of accurately known shades of gray printed out for use in calibrating those shades on a display or printer. In graphics, composed of discrete shades of gray. For displays, a color format in which each pixel is determined by an 8-bit value. This value maps to RGB space with the red, green, and blue components all taking on the 8-bit value. The result is pixels which can range from black, to gray, to pure white. (*TMS320C8x*)

GREG: See *global memory allocation register*.

ground strap: A strip of conductive material attached at one end to earth ground and at the other to a person or an object so that static electricity can dissipate to ground and bypass electronic circuitry. Typically used by people when they are handling discrete electronic components or assemblies that are sensitive to static electricity.

GROUP: A directive to the linker in TI's code generation toolset that forces specified output sections to be allocated contiguously (as a group).

GSM: *Global System for Mobile Communications*.

GUI: See *graphical user interface.*

guided transfer: A transfer in which the sequence of dimension addresses is guided from an on-chip memory table, rather than calculated solely from values within the packet transfer parameters. See also *dimensioned transfer*.

guide table: A table of parameters describing individual patches within a packet transfer. See also *patch.*

H

halfword: A 16-bit value.

HALTR: See *autobuffering receiver halt (HALTR) bit*.

HALTX: See *autobuffering transmitter halt (HALTX) bit*.

hardware interrupt: An interrupt triggered through physical connections with on-chip peripherals or external devices.

$\overline{\text{HBLNK}}$: *Horizontal blanking*. A bidirectional horizontal timing signal that enables or disables pixel capture and display. $\overline{\text{HBLNK}}$ occurs once per line and has a pulse width defined as an integral number of frame clock (FCLK) periods. See also *blanking pulse*.

heap: A large pool of memory that can be allocated at runtime by application programs and by the executive.

hex command file: A file that contains hex conversion utility options and names input files for the hex conversion utility.

hex conversion utility: A program which accepts common object file format (COFF) files and converts them into one of several standard ASCII hexadecimal formats suitable for loading into an EPROM programmer.

high-level language debugging: The ability of a compiler to retain symbolic and high-level language information (such as type and function definitions) so that a debugging tool can use this information.

HINT bit: *DSP-to-host processor interrupt*. A field that enables and/or disables an interrupt from the DSP to a host processor. At reset, HINT = 0. This bit is stored in the host port interface control register (HPIC). (*TMS320C57*, *TMS320C54x*)

hit: A condition in which the instruction that the processor fetches is available in the cache.

HM: See *hold mode (HM) bit*.

$\overline{\text{HOLD}}$: An input signal that allows external devices to request control of the external buses. If an external device drives the $\overline{\text{HOLD}}$ pin low and the CPU sends an acknowledgement at the $\overline{\text{HOLDA}}$ pin, the external device has control of the buses until it drives $\overline{\text{HOLD}}$ high or a nonmaskable hardware interrupt is generated. If $\overline{\text{HOLD}}$ is not used, it should be pulled high.

$\overline{\text{HOLDA}}$: *$\overline{\text{HOLD}}$ acknowledge signal*. An output signal sent to the $\overline{\text{HOLDA}}$ pin by the CPU in acknowledgement of a properly initiated HOLD operation. When $\overline{\text{HOLDA}}$ is low, the processor is in a holding state and the address, data, and memory-control lines are available to external circuitry.

hold mode (HM) bit: A 1-bit field that determines whether the CPU can stop or continue when the $\overline{\text{HOLD}}$ signal initiates a power-down mode. At reset, HM = 1. This bit is stored in status register 1 (ST1).

HOLD operation: An operation that allows for direct access of memory and I/O devices. When a HOLD operation is initiated by a $\overline{\text{HOLD}}$ signal, the external buses enter a high-impedance state and the $\overline{\text{HOLDA}}$ signal is asserted. The buses return to their normal state and the HOLD operation is concluded when the host processor deasserts $\overline{\text{HOLD}}$ high. (*TMS320C24x*)

hole: An area in memory containing no actual code or data.

HOM: See *host-only mode*.

horizontal blanking: A bidirectional timing signal that enables or disables pixel capture and display. Horizontal blanking occurs once per line; its pulse width is defined as an integral number of frame clock (FCLK) periods. See also *blanking*. (*TMS320C8x*)

horizontal synchronization: The portion of the composite video signal that tells the receiver where to place the image in the left-to-right dimension. The horizontal sync pulse tells the receiving system where the beginning of the new scan line is. See also *vertical sync*. (*TMS320C8x*)

host-only mode (HOM): A mode that allows only the host to access host port interface (HPI) memory. The CPU has no access to the HPI memory block during HOM.

host port interface (HPI): An 8-bit parallel interface that the CPU uses to communicate with a host processor.

host port interface control (HPIC) register: A register that controls the operation of the host port interface (HPI). (*TMS320C54x*)

housekeeping: Those operations or routines that do not contribute directly to the solution of a computer program, but rather to the organization of the program.

HPI: See *host port interface (HPI)*.

HPIA: See *HPI address (HPIA) register*.

HPI address (HPIA) register: A register that stores the address of the host port interface (HPI) memory block. The HPIA can be preincremented or postincremented.

HPI address register high (HPIAH) byte: The higher 8 bits stored in the host port interface address (HPIA) register. See also *HPI address (HPIA) register*.

HPI address register low (HPIAL) byte: The lower 8 bits stored in the host port interface address (HPIA) register. See also *HPI address (HPIA) register*.

HPIAH: See *HPI address register high (HPIAH) byte*.

HPIAL: See *HPI address register low (HPIAL) byte*.

HPIC: See *host port interface control (HPIC) register*.

HPICH: See *HPI control register high (HPICH) byte*.

HPICL: See *HPI control register low (HPICL) byte*.

HPI control register high (HPICH) byte: The higher 8 bits stored in the host port interface control (HPIC) register. See also *HPI control (HPIC) register*.

HPI control register low (HPICL) byte: The lower 8 bits stored in the host port interface control (HPIC) register. See also *HPI control (HPIC) register*.

$\overline{\text{HSYNC}}$: *Horizontal synchronization*. A bidirectional horizontal timing signal occurring once per line with a pulse width defined as an integral number of frame clock (FCLK) periods. Synchronization signals can be used to enable retrace of the electron beam of a display screen.

I

$\overline{\text{IACK}}$: See *interrupt acknowledge signal*.

IC: See *integrated circuit*.

ICPU interrupt flag register (IF): A register that contains CPU, serial ports, timer, and DMA interrupt flags.

ICR: 1) *Instruction-cache reset*. A command you send with the master processor cmnd instruction that resets all instruction cache tag registers and the instruction least recently used (ILRU) register. 2) See *Interrupt control register (ICR)*. (*TMS320C24x, TMS320C8x*)

ID: See *identifier*.

identifier (ID): A field that contains a resource-table index, a sequence number, and a resource-type code; it identifies a kernel resource such as a port, semaphore, or task.

IE: See *internal interrupt enable register*.

IEEE-754 floating point unit: The floating point math unit contained in the core of the TMS320C8x's master reduced instruction set computer (RISC) processor. (*TMS320C8x*)

IEEE-754 standard: A standard sponsored by the Standards Committee of the IEEE Computer Society that describes various aspects for floating-point numbers, such as definitions, formats, exceptions, and rounding details.

IEEE 1149.1 standard: "IEEE Standard Test Access Port and Boundary-Scan Architecture", first released in 1990. See also *JTAG*.

IEEE mode: A master processor (MP) floating-point unit mode in which MP floating-point instructions are executed with denormals handled as defined in the IEEE-754 standard.

IEEE standard 1149.1-1990: See *JTAG.*

IIE: See *internal interrupt enable register*.

IIF: See *IIOF flag register*.

IIOF flag register (IIF): Controls the function (general-purpose I/O or interrupt) of the four external pins ($\overline{\text{IIOF0}}$ to $\overline{\text{IIOF3}}$). It also contains timer and/or DMA interrupt flags. (*TMS320C4x*)

immediate addressing: One of the methods for obtaining data values used by an instruction. The data value is a constant embedded directly into the instruction word; data memory is not accessed.

immediate operand/immediate value: A constant given as an operand in an instruction that is using immediate addressing.

IMR: See *interrupt mask register*.

IN0 bit: *Input 0 bit*. A field that allows the receive clock input (CLKR) pin to be used as an input. IN0 reflects the current level of the CLKR pin of the device. This bit is stored in the serial port control (SPC) and TDM serial port control register (TSPC).

IN1 bit: *Input 1 bit*. A field that allows the transmit clock input/output (CLKX) pin to be used as an input. IN1 reflects the current level of the CLKX pin of the device. This bit is stored in the section program counter (SPC) and time-division multiplexed (TDM) serial port control register (TSPC).

incremental linking: Linking files in several passes. Incremental linking is useful for large applications, because you can partition the application, link the parts separately, and then link all of the parts together.

index register (INDX): A memory-mapped register that specifies increment sizes greater than 1 for indirect addressing updates. In bit-reversed addressing, the INDX defines the array size. (*TMS320C2x, TMS320C2xx, TMS320C5x*)

index registers: Two registers (IR0 and IR1) that are used by the auxiliary register arithmetic unit (ARAU) for indexing an address. (*TMS320C3x/4x*)

indirect addressing: One of the methods for obtaining data values used by an instruction. When an instruction uses indirect addressing, data memory is addressed by the current auxiliary register. See also *direct addressing*.

indirect call: A function call where one function calls another function by giving the address of the called function.

INDX: See *index register (INDX)*.

$\overline{\text{INTn}}$: An external pin used to generate general-purpose hardware interrupts.

init.cmd: A batch file that contains debugger-initialization commands. If this file isn't present when you first invoke the debugger, then all memory is invalid. (This is a standard part of the TI debugger environment.)

initdb.bat: As part of normal debugger use, you must enter DOS commands to set up the debugger environment. The most convenient method for doing this is to edit your PC's autoexec.bat or to create a separate initdb.bat file that is used only for this purpose.

initialization at load time: An autoinitialization method used by the linker when linking C code. The linker uses this method when you invoke the linker with the –cr option. This method initializes variables at load time instead of runtime.

initialized section: A common object file format (COFF) section that contains executable code or data. An initialized section can be built with the .data, .text, or .sect directive.

initiator: A small computer system interface (SCSI) device (usually a host computer) that requests another SCSI device to take an action.

init-list: A list of functions that are executed by the kernel each time a new task is created.

input clock signal (CLKIN): A clock source signal supplied to the on-chip clock generator at the CLKIN/X2 pin or generated internally by the on-chip oscillator. The clock generator divides or multiplies CLKIN to produce the CPU clock signal (CLKOUT1).

input data-scaling shifter: A 16- to 32-bit barrel left-shifter that shifts incoming 16-bit data from 0 to 16 positions left, relative to the 32-bit output, within the fetch cycle with no cycle overhead. Also called *input shifter*.

input section: A section from an object file that is linked into an executable module.

instruction: The basic unit of programming that causes the execution of one operation; it consists of an opcode and operands along with optional labels and comments.

instruction bus: A processor-dependent bus used to access instructions from on-chip static RAM (SRAM). The parallel processors each use a 64-bit instruction bus, and the master processor uses a 32-bit instruction bus.

instruction cache: An on-chip static RAM (SRAM) that contains current instructions being executed by one of the processors. Cache misses are handled by the transfer controller. (*TMS320C8x, TMS320C3x/4x*)

instruction-decode phase: The second phase of the pipeline; the phase in which the instruction is decoded. See also *pipeline*.

instruction-execute phase: The fourth phase of the pipeline; the phase in which the instruction is executed. See also *pipeline*.

instruction-fetch phase: The first phase of the pipeline; the phase in which the instruction is fetched from program-memory. See also *pipeline*. (*TMS320C8x*)

instruction pointer (IP): The master processor register that points to the instruction currently in the fetch stage of the pipeline.

instruction pointer address (IPA): The parallel processor register that points to the current statement in the address pipeline stage of your program.

instruction pointer execution (IPE): The parallel processor register that points to the current statement in the execute pipeline stage of your program.

instruction port: The port used by the parallel processor for communication with its instruction cache.

instruction register (IREG) or (IR): A register that contains the actual instruction being executed.

instruction word: In fixed-point DSP programming, an instruction word is a 16-bit value representing all or half of an instruction. An instruction that is fully represented by 16 bits uses one instruction word. An instruction that must be represented by 32 bits uses two instruction words; the second word is a constant. (In floating-point devices, all instruction words are 32-bits.)

integrated circuit (IC): A tiny wafer of substrate material upon which is etched or imprinted a complex of electronic components and their interconnections.

integrated preprocessor: A C preprocessor that is merged with the parser, allowing for faster compilation. Standalone preprocessing or preprocessed listing is also available.

Integrated Services Digital Network (ISDN): A worldwide digital communications network evolving from existing telephone services. Its goal is to replace current telephone lines that require DA conversions with totally digital switching and transmission facilities capable of carrying a variety of data—from voice to computer transmissions, music, and video. The ISDN is built on two main types of communications channels: a B channel, which carries data at 64 Kb/s, and a D channel, which carries control information at either 16 or 64 Kb/s. Computers and other devices connect ISDN lines through simple, standardized interfaces. When fully implemented (possibly around the year 2000), the ISDN is expected to provide users with faster, more extensive communications services. (TGC4000 DM Supp)

interlaced mode: A video mode in which each frame consists of two vertical fields. One field displays odd horizontal lines, and the other field displays even horizontal lines. In effect, the number of transmitted pictures is doubled, thereby reducing flicker.

interlist utility: A utility that inserts your original C source statements as comments into the assembly language output from the assembler. The C statements are inserted next to the equivalent assembly instructions.

internal address: An address internal to the multimedia video processor (MVP) chip. Addresses from 0x0000 0000 to 0x1FFF FFFF are on-chip addresses. Also called *on-chip address.*

internal data memory block: A set of memory banks forming a contiguous set of addresses. ’C6x memory banks are interleaved such that striding half-word addresses takes from one bank in the block to the next.

internal interrupt enable register: A register in the CPU register file that determines whether or not the CPU responds to interrupts from the communication ports, the timers, and the DMA coprocessor. (*TMS320C4x*)

internal interrupt: A hardware interrupt caused by an on-chip peripheral.

internal memory bank: A physical bank of memory. Only a single access is permitted to a single bank at a time.

internal transmit clock division factor (CLKDV) bits: A field that determines the internal transmit clock duty cycle. At reset, CLKDV = 00011. These bits are stored in the buffered serial port (BSP) control extension register (SPCE).

internode message manager: A special task that manages an interface with another processor node to facilitate message transfers across the interface. Routing of messages across internode boundaries is one of the system services provided by the multimedia video processor (MVP) executive.

interprocessor command: A message sent through the crossbar to the other on-chip processors.

interrupt: A signal sent by hardware or software to a processor requesting attention. An interrupt tells the processor to suspend its current operation, save the current task status, and perform a particular set of instructions. Interrupts communicate with the operating system and prioritize tasks to be performed.

interrupt acknowledge signal ($\overline{\text{IACK}}$): An output signal that indicates an interrupt has been received and that the program counter is fetching the interrupt vector that forces the processor into the appropriate interrupt service routine.

interrupt control register (ICR): A register used to differentiate $\overline{\text{HOLD}}$ and $\overline{\text{INT1}}$ and to individually mask and flag $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$. (*TMS320C2xx, TMS320C24x*)

interrupt flag register (IFR): A memory-mapped register that indicates pending interrupts. Read the IFR to identify pending interrupts; write to the IFR to clear selected interrupts. Writing a 1 to any IFR flag bit clears that bit to 0. (*TMS320C24x*)

interrupt latency: The delay between the time an interrupt request is made and the time it is serviced.

interrupt mask register (IMR): A memory-mapped register used to mask external and internal interrupts. Writing a 1 to any IMR bit position enables the corresponding interrupt (when INTM = 0).

interrupt mode (INTM) bit: A field that globally masks or enables all interrupts. When INTM = 0, all unmasked interrupts are enabled. When INTM = 1, all maskable interrupts are disabled. INTM has no effect on the nonmaskable $\overline{\text{RS}}$ and $\overline{\text{NMI}}$ interrupts. At reset, INTM = 1.This bit is stored in status register 0 (ST0).

interrupt service fetch packet (ISFP): A fetch packet used to service interrupts. If eight instructions are insufficient, the user must branch out of this block for additional interrupt service. If the delay slots of the branch do not reside within the ISFP, execution continues from execute packets in the next ISFP. (TMS320C62xx)

interrupt service routine (ISR): A module of code that is executed in response to a hardware or software interrupt.

interrupt service table (IST): Sixteen contiguous interrupt service fetch packets (ISFPs), each corresponding to a condition in the interrupt flag register (IFR). The IST resides in memory accessible by the program memory system. The IST must be aligned on a 256-word boundary (32 fetch packets x 8 words/fetch packet). Although only 16 interrupts are defined, space in the IST is reserved for 32 for future expansion. The IST's location is determined by the interrupt service table pointer (ISTP) register. (*TMS320C62xx*)

interrupt trap: See *interrupt service routine (ISR)*.

interrupt-trap table pointer (ITTP): A bit field in the status register that indicates the starting location (base address) of the interrupt-trap vector table. The base address is formed by left-shifting the value of the ITTP bit field by 8 bits.

interrupt vector: A branch instruction that leads the CPU to an interrupt service routine (ISR).

interrupt vector location: An address in program memory where an interrupt vector resides. When an interrupt is acknowledged, the CPU branches to the interrupt vector location and fetches the interrupt vector.

interrupt vector pointer (IPTR) bits: A field that identifies the 2K page where the interrupt vectors currently reside in the system. The IPTR bits enable you remap the interrupt vectors to RAM for boot-loaded operations. At reset, IPTR = 0. These bits are stored in the processor mode status register (PMST). (*TMS320C5X*)

interrupt vector table (IVT): An ordered list of addresses, each of which correspond to an interrupt; when an interrupt occurs and is enabled, the processor executes a branch to the address stored in the corresponding location in the interrupt vector table.

interrupt vector table pointer (IVTP): A register in the CPU expansion register file that contains the address of the beginning of the interrupt vector table. (*TMS320C4x*)

INTM bit: See *interrupt mode bit*.

IO0–IO3 bits: Bits 0–3 of the IOSR. When pins IO0–IO3 are configured as inputs, these bits reflect the current logic levels on the pins. For example, the IO0 bit reflects the level on the IO0 pin. See also *CIO0–CIO3 bits*; *DIO0–DIO3 bits*. (*TMS320C2xx*)

IO0–IO3 pins: Four pins that can be individually configured as inputs or outputs. These pins can be used for interfacing the asynchronous serial port or as general-purpose I/O pins. See also *CIO0–CIO3 bits; DIO0–DIO3 bits; IO0–IO3 bits*. (*TMS320C2xx*)

I/O flag (IOF) register: Controls the function (general-purpose I/O or interrupt) of the external pins. It also contains timer/DMA interrupt flags.

I/O-mapped register: One of the on-chip registers mapped to addresses in input/output (I/O) space. These registers, which can include the registers for the on-chip peripherals, must be accessed with the IN and OUT instructions. See also *memory-mapped register*.

I/O port wait-state register (IOWSR): A memory-mapped register that specifies the number of wait states for the input/out (I/O) port. The IOWSR can be mapped in one of two ways as specified by the BIG bit in the wait-state control register (CWSR). At reset, IOWSR = FFFF.

IOSR: See *I/O status register.*

I/O status register (IOSR): A register in the asynchronous serial port that provides status information about signals IO0–IO3 and about transfers in progress. (*TMS320C2xx*)

I/O switches: Hardware switches on the emulator or evaluation module (EVM) board that identify the PC I/O memory space used for emulator-debugger or EVM-debugger communications.

IOWSR: See *I/O port wait-state register*.

IP: See *instruction pointer.*

IPA: See *instruction pointer address.*

IPE: See *instruction pointer execution.*

IPTR: See *interrupt vector pointer (IPTR) bits*.

IR: See *instruction register*.

IREG: See *instruction register*.

$\overline{\text{IS}}$: *I/O space select pin*. The DSP asserts $\overline{\text{IS}}$ to indicate an access to external I/O space.

ISA: *Industry Standard Architecture*. A subset of the Extended Industry Standard Architecture (EISA) standard.

ISDN: See *Integrated Services Digital Network*.

ISR: See *interrupt service routine*.

ISWS: *I/O-space wait-state bit(s).* A value in the wait-state generator control register (WSGR) that determines the number of wait states applied to reads from and writes to off-chip I/O space. On the ’C209, ISWS is bit 2 of the WSGR; on other ’C2xx devices, ISWS is bits 11–9. *(TMS320C2xx)*

ITTP: See *interrupt-trap table pointer*.

IVTP: See *interrupt vector table pointer*.

J

JPEG standard: *Joint Photographic Experts Group standard*. A standard used for compressed still-picture data.

JTAG: *Joint Test Action Group*. The Joint Test Action Group was formed in 1985 to develop economical test methodologies for systems designed around complex integrated circuits and assembled with surface-mount technologies. The group drafted a standard that was subsequently adopted by IEEE as IEEE Standard 1149.1-1990, “IEEE Standard Test Access Port and Boundary-Scan Architecture”. See also *boundary scan*; *test access port (TAP)*.

K

kernel: 1) The core portion of the operating system that manages memory, files, and peripheral devices. It also starts applications, allocates resources, and maintains time and date. 2) A set of low-level software primitives within the TMS320C8x multitasking executive that implement multitasking, the passing of messages and signals, and the monitoring of multiple events.

kernel resource: A data item or object created by and used within the kernel. The kernel defines three types of resources: port, semaphore, and task. See also *port*, *semaphore*, *task*.

K & R: *Kernigan and Ritchie*. Authors of *The C Programming Language* (second edition), by Brian Kernighan and Dennis M. Ritchie, published by Prentice-Hall, Englewood Cliffs, New Jersey, 1988.

L

LA0–LA*n*: External address pins for data/program memory or I/O devices. These pins are on the local bus.

label: A symbol that begins in column 1 of an assembler source statement and corresponds to the address of that statement. A label is the only assembler statement that can begin in column 1.

latch phase: The phase of a CPU cycle during which internal values are held constant. See also *logic phase*; *CLKOUT1*.

latency: The delay between when a condition occurs and when the device reacts to the condition. Also, in a pipeline, the necessary delay between the execution of two instructions to ensure that the values used by the second instruction are correct.

LCR cycle: See *load color register cycle*.

LCSR: See *local control synchronization register*.

LD0–LD*n*: External data bus pins that transfer data between the processor and external data/program memory or I/O devices. *See also D0–Dn*.

least significant bit (LSB): The bit having the smallest effect on the value of a binary numeral, usually the rightmost bit.

least significant byte (LSByte): The byte in a multibyte word that has the least influence on the value of the word.

linear assembly: Assembly code that has not been register-allocated or scheduled, which is used as input for the assembly optimizer. Linear assembly files have a .sa extension.

line dropping: The process of eliminating lines of video from an image to downscale the image vertically.

line number entry: An entry in a common object file format (COFF) output module that maps lines of assembly code back to the original C source file that created them.

linker: A software program that combines object files to form an object module that can be allocated into system memory and executed by the device.

linker command file: A file that contains linker options and names input files for the linker.

listing file: An output file created by the assembler that lists source statements, their line numbers, any unresolved symbols or opcodes, and their effects on the section program counter (SPC).

little-endian: An addressing protocol in which bytes are numbered from right to left within a word. More significant bytes in a word have higher numbered addresses. Endian ordering is specific to hardware and is determined at reset. See also *big endian*.

live in: A value that has been defined before a procedure and is used as an input to that procedure.

live out: A value that has been defined within a procedure and is used as an output from that procedure.

lmbc: *Leftmost-bit change.* The parallel processor operation that returns the position of the leftmost bit that has a value different from the sign bit.

LMICR: *Local memory interface control register*.

lmo: *Leftmost 1.* The master processor (MP) or parallel processor operation that returns the position of the leftmost bit that has a value of 1. In the MP, lmo is an instruction, while in the parallel processor, it is a bit detection function.

load: To enter data into storage or working registers.

load address: The beginning address to which a section of code is loaded.

load color register (LCR) cycle: A memory cycle generated by the transfer controller (TC) that writes a specified value into the video RAM (VRAM's) color registers for use during a block-write cycle. LCR cycles are supported only on 64-bit data buses and are indicated by STATUS [5:0] = 001101.

loader: A device that places an executable module into system memory.

local address unit: Parallel processor hardware that generates addresses using a local address register with preaddition, postaddition, presubtraction, or postsubtraction of an index register or an immediate offset.

local bus: A bus allocated to each parallel processor to access on-line SRAM data in a single cycle.

local control synchronization register (LCSR): The LCSR controls software synchronization between the four TMS320C40s and their dedicated erasable programmable ROM (EPROM) and static RAM (SRAM).

local data space: The portion of data-memory addresses that are not allocated as global by the global memory allocation register (GREG). If none of the data-memory addresses are allocated for global use, all of data space is local. See also *global data space*.

local legal: An access in a parallel processor's local RAM that can be performed through the local port. Such access is done in a single cycle. If an access is attempted through the local port but is not local legal, access must be diverted to the global port, causing a pipeline stall.

local node: The local processor node. This term is relative. A task that executes on a particular node *n* considers node *n* its local node, but tasks that execute on other nodes consider node *n* to be a foreign node.

local port: The parallel processor data port with access restricted to a parallel processor's local RAMs.

local RAM: The on-chip RAM that is associated with a particular parallel processor in a multimedia video processor (MVP).

local transfer: A local address unit operation. This is a memory access that usually occurs over the local port.

logical address: A memory location that is referenced by device instructions; the logical address is a part of the processor's logical memory map.

logical unit: A physical or virtual device that is addressable through a target.

logical unit number (LUN): A 3-bit code for a logical unit.

logic phase: The phase of a CPU cycle during which internal values are changed. See also *latch phase*; *CLKOUT1*.

long immediate: On the master processor (MP), a 32-bit value that is either a signed or unsigned integer, a single-precision floating-point constant, a relative branch word offset, or an absolute address. The MP long-immediate instruction format requires two 32-bit instruction words.

long-immediate value: A 16-bit constant given as an operand of an instruction that is using immediate addressing.

long offset: An unsigned 15-bit offset for halfword or word transfers, or an unsigned 16-bit offset for byte transfers.

look-up table: A table, used during scan conversions of a digital image, that converts color-map addresses into the actual color values displayed.

loop: A sequence of instructions executed repeatedly until a terminal condition prevails.

loop unrolling: An optimization that expands small loops so that each iteration of the loop appears in your code. Although loop unrolling increases code size, it can improve the efficiency of your code.

LPRAM: The parallel processor-relative reference to a parallel processor's local 2K-byte parameter RAM.

LRAM0: The parallel processor-relative reference to a parallel processor's local 2K-byte data RAM bank with the lowest address.

LRAM1: The parallel processor-relative reference to a parallel processor's local 2K-byte data RAM bank with the second lowest address.

LRAM2: The parallel processor-relative reference to a parallel processor's local 2K-byte data RAM bank with the highest address.

LRU cache replacement: *Least recently used cache replacement*. A cache management strategy that replaces the least recently used cache block in memory (while retaining the blocks more recently used) when a cache block-miss occurs.

LSB: See *least significant bit.*

LSByte: See *least significant byte.*

luminance: The National Television Standards Committee (NTSC) or phase alternation line (PAL) video signal contains two pieces that make up what you see on the screen: the black and white part (luminance) and the color part (chrominance). See also *chrominance*.

LUN: See *logical unit number*.

M

μ-Law companding: See *companded*.

MAC: *Multiply and accumulate*.

machine cycle: See *CPU cycle*.

macro: A user-defined routine that can be used as an instruction.

macro call: The process of invoking a macro.

macro definition: A block of source statements that define the name and the code that make up a macro.

macro expansion: The source statements that are substituted for the macro call and are subsequently assembled.

macro library: An archive library composed of macros. Each file in the library must contain one macro; its name must be the same as the macro name it defines, and it must have an extension of .asm.

magic number: A common object file format (COFF) file header entry that identifies an object file as a module that can be executed.

mailbox: A 32-bit word in a parallel processor's parameter RAM in which it places messages to clients (chiefly, the master processor).

mantissa: A component of a floating-point number consisting of a fraction and a sign bit. The mantissa represents a normalized fraction whose binary point is shifted by the exponent.

map file: An output file, created by the linker, that shows the memory configuration, section composition, section allocation, symbol definitions, and the addresses at which the symbols were defined for your program.

maskable interrupt: An interrupt that can be enabled or disabled through software.

mask generator: A parallel processor's arithmetic logic unit (ALU) data path hardware device that takes a 5-bit input *n* and outputs a mask containing *n* 1s specified by the input when it is right-justified.

masking: The ability to selectively ignore part of a data word.

master clock output signal (CLKOUT1): The output signal of the on-chip clock generator. The CLKOUT1 high pulse signifies the CPU's logic phrase (when internal values are changed), while the CLKOUT1 low pulse signifies the CPU's latch phase (when the values are held constant).

master phase: See *logic phase*.

master processor (MP): A general-purpose reduced instruction set computer (RISC) processor that coordinates the activity of the other processors on the multimedia video processor (MVP). The MP includes an IEEE-754 floating-point hardware unit.

MCBL/$\overline{\text{MP}}$ pin: A pin used to select between microprocessor mode or microcomputer mode. MCBL/$\overline{\text{MP}}$ high selects microcomputer mode; MCBL/$\overline{\text{MP}}$ low selects microprocessor mode.

MCM: See *clock mode (MCM) bit*.

MCS: See *microcall stack (MCS)*.

member: An element of a structure, union, or enumeration.

memory map: A graphical representation of a computer system's memory, showing the locations of program space, data space, reserved space, and other memory-resident elements.

memory-mapped register: An on-chip register mapped to an address in memory. Some memory-mapped registers are mapped to data memory, and some are mapped to input/output memory.

memory stall: The CPU is stalled while waiting on a memory load or store.

memory width: The number of bits that can be stored in a single external memory address.

MEMORY window: A window that displays the contents of memory. (This window is part of the standard graphical user interface for all TI debuggers.)

menu bar: A row of pulldown menu selections found at the top of the debugger display.

merge mode: A serial register transfer (SRT) mode for the video controller (VC) during which an image is captured and stored in memory. Memory locations not corresponding to the captured image are preserved. See also *capture mode*, *display mode*. (*TMS320C8x*)

message buffer pool: A group of message buffers, typically of uniform size, that belong to a particular task.

message event: An event caused by the arrival of a message at a port. If a task is waiting for the event, that task is scheduled to begin executing.

message header: A fixed-size structure at the beginning of a message buffer that contains the information that describes the message, its destination port, and so on, to the kernel functions that handle the message.

message interrupt: A multimedia video processor (MVP) hardware mechanism through which one on-chip processor can signal an interrupt to another on-chip processor, if that interrupt is enabled.

message port: See *port*.

message-routing table: A table that specifies the routing ports for messages sent to foreign processor nodes.

metric parameters: A set of parameters that define state dimensions and attributes for the audio subsystem, display subsystem, or video capture subsystem.

MFLOPS: *Millions of floating-point operations per second*. A measure of floating-point processor speed that counts of the number of floating-point operations made per second.

MHz: *Megahertz*.

microcall stack (MCS): A single-word stack that temporarily stores the contents of the prefetch counter (PFC) while the PFC addresses data memory with the block move (BLDD/BLPD), multiply-accumulate (MAC/MACD), and table read/write (TBLR/TBLW) instructions.

microcomputer: An integrated circuit that consists of a microprocessor, controller, storage registers, some sort of arithmetic logic unit (ALU), and memory.

microcomputer mode: A mode in which the on-chip ROM or flash memory is enabled. This mode is selected with the MP/$\overline{\text{MC}}$ pin. See also *MP/$\overline{\text{MC}}$ pin*; *microprocessor mode*.

microprocessor: An integrated circuit that can be programmed with stored instructions to perform a wide variety of functions.

microprocessor/microcomputer (MP/$\overline{\text{MC}}$) bit: A 1-bit field used to select microprocessor mode or microcomputer mode. MP/$\overline{\text{MC}}$ high selects microprocessor mode. MP/$\overline{\text{MC}}$ low selects microcomputer mode.

microprocessor mode: A mode in which the on-chip ROM or flash memory is disabled. This mode is selected with the MP/$\overline{\text{MC}}$ pin. See also *MP/$\overline{\text{MC}}$ pin*; *microcomputer mode*.

microstack (MSTACK): A register used for temporary storage of the program counter (PC) value when an instruction needs to use the PC to address a second operand. (*TMS320C24x*)

MIMD: *Multiple instruction stream, multiple data stream.* A parallel processing structure composed of multiple independent processors.

mini-DIN connector: A connector that is similar to a Deutsch Industrie Norm (DIN) connector (only much smaller) using multiple pins in accordance with the German national standard organization. Two 8-pin mini-DIN connectors are used on the software development board (SDB) to connect input/output peripherals. *(TMS320C8x)*

minimal mode: A debugging mode that displays the COMMAND window, WATCH window, and DISP window only.

MIPS: *Million instructions per second*.

miscellaneous operation: One of several operations that do not involve the data unit, including nop, eint, and dint. The data unit portion of the opcode is used to specify the operation.

miss: A condition in which an instruction is not available in the cache when it is fetched by the processor.

mixed mode: A debugging mode that simultaneously shows both assembly language code in the DISASSEMBLY window and C code in the FILE window.

mnemonic: An alphanumeric symbol designed to aid human memory; it commonly represents the operation code of an assembly language instruction name that the assembler translates into machine code.

MODE bit: A bit within the interrupt control register (ICR) that determines whether the $\overline{\text{HOLD}}$/$\overline{\text{INT1}}$ pin is only negative-edge sensitive or both negative- and positive-edge sensitive. (*TMS320C24x*)

model statement: Instructions or assembler directives in a macro definition that are assembled each time a macro is invoked.

modular port scan device (MPSD): Technology that allows complete emulation through a serial scan path of the 'C3x. (*TMS320C3x*)

modulo addressing: See circular addressing.

monitor timing (parameters): Parameters used by the display application programming interface (API) to determine what signal rates are needed to drive a monitor.

mono mode: A mode of the audio codec in which only one channel of audio exists.

most significant bit (MSB): The highest order bit in a word. The plural form (MSBs) refers to a specified number of high-order bits, beginning with the highest order bit and counting to the right. For example, the eight MSBs of a 16-bit value are bits 15 through 8.

most significant byte (MSByte): The byte in a multibyte word that has the most influence on the value of the word.

motherboard: The main circuit board that contains the processor, main memory, circuitry, bus controller, connectors, and primary components of the computer. The TMS320C8x software development board (SDB) is connected to the motherboard through the peripheral component interconnect (PCI) local bus. Depending upon the computer system design, daughter boards, expansion boards, input/output boards, other boards, or additional memory may also be connected to the motherboard using the bus controller.

mouse cursor: A block-shaped cursor that tracks mouse movements over the entire display.

MP: See *master processor*.

mpcl: A shell utility that invokes the multimedia video processor (MVP) master processor compiler, assembler, and linker to create an executable object file version of your master processor program.

MPEG standard: *Moving Picture Experts Group standard*. A proposed standard for compressed video data.

MP/$\overline{\text{MC}}$ bit: See *microprocessor/microcomputer (MP/$\overline{\text{MC}}$) bit*.

MP/$\overline{\text{MC}}$ pin: A pin used to select between microprocessor mode or microcomputer mode. MP/$\overline{\text{MC}}$ high selects microprocessor mode; MP/$\overline{\text{MC}}$ low selects microcomputer mode. *(TMS320C24x*)

MPSD: See *modular port scan device*.

MPY||ADD: A parallel processor's data unit opcode format that allows a multiply to be specified in parallel with an add or subtract by the arithmetic logic unit (ALU). See also *arithmetic logic unit*.

MPY||EALU: A parallel processor's data unit opcode format that allows a multiply to be specified in parallel with an extended arithmetic logic unit (EALU) operation. See also *extended arithmetic logic unit*.

MSB: See *most significant bit.*

MSByte: See *most significant byte.*

MSTACK: See *microstack*.

MULT: See *multiplier.*

multimedia video processor (MVP): A single-chip multiprocessor device that accelerates applications such as video compression and decompression, image processing, and graphics. The multimedia video processor contains a master processor and from one to eight parallel processors, depending on the device version. For example, the TMS320C80 device contains four parallel processors.

multiplexing: A process of transmitting more than one set of signals at a time over a single wire or communications link. (Also known as muxing.)

multiple arithmetic: A parallel processor's arithmetic logic unit (ALU) operation in which the carry from bit to bit is disabled at certain points in the ALU, causing the ALU to act as multiple smaller ALUs. A status bit, either carry-out or 0, from each ALU segment is saved in the mf register. Multiple arithmetic is also referred to as split ALU.

multiple-byte arithmetic: Multiple arithmetic with ASize set to byte. The arithmetic logic unit (ALU) acts like four parallel byte ALUs because the carry-path is broken between bits 24 and 23, bits 16 and 15, and bits 8 and 7.

multiple-halfword arithmetic: Multiple arithmetic with Asize set to halfword. The arithmetic logic unit (ALU) acts like two parallel ALUs because the carry-path is broken between bits 16 and 15.

multiplier (MULT): A part of the CPU that performs multiplication and generates a product. The multiplier operates using either signed or signed 2s-complement arithmetic.

multisync monitor: A monitor that adjusts itself to the horizontal and vertical synchronization rate of the video signal. A multisync monitor can be used with a variety of video adapters.

multitasking executive: The portion of a multitasking software system that is responsible for executing application tasks, providing communications among tasks, and managing shared resources. See also *executive*.

mutual exclusion: A collection of techniques for sharing resources so that different uses do not conflict and cause unwanted interactions. One of the most commonly used techniques for mutual exclusion is the semaphore. See also *semaphore*.

MVP: See *multimedia video processor*.

MVP multitasking executive: See *executive*.

N

named section: 1) An initialized section that is defined with a .sect directive; 2) an uninitialized section that is defined with a .usect directive.

National Television Standards Committee (NTSC): A color television broadcast standard wherein the image consists of a:

- Format that has 525 scan lines
- Field frequency of 60 Hz
- Broadcast bandwidth of 4 MHz
- Line frequency of 15.75 kHz
- Frame frequency of one–thirtieth of a second
- Color subcarrier frequency of 3.58 MHz

See also *PAL*. (*TMS320C8x*)

NDX: See *enable extra index register (NDX) bit*.

nested interrupt: A higher-priority interrupt that must be serviced before completion of the current interrupt service routine (ISR). An executing ISR can set the interrupt mask register (IMR) bits to prevent being suspended by another interrupt.

next AR: See *next auxiliary register*.

next auxiliary register: The register that is pointed to by the auxiliary register pointer (ARP) when an instruction that modifies ARP is finished executing. See also *auxiliary register*; *current auxiliary register*.

next program address register (NPAR): Part of the program-address generation logic. This register provides the address of the next instruction to the program counter (PC), the program address register (PAR), the micro stack (MSTACK), or the stack.

$\overline{\text{NMI}}$: A hardware interrupt that uses the same logic as the maskable interrupts but cannot be masked. It is often used as a soft reset. See also *maskable interrupt*; *nonmaskable interrupt*.

node: Any entity capable of sending and receiving messages, such as a processor port.

node-global port ID: A port ID that contains an explicit node number in the range 0 to 127. A node-global destination port ID is required to route a message across processor node boundaries in a multiprocessor system.

node-local port ID: A port ID that does not contain an explicit processor node number but that is implicitly local. The resource-type code in the eight most significant bits (MSBs) of a node-local port ID is set to a value of –1.

node number: A small nonnegative integer that uniquely identifies each processor node in a multiprocessor system. A node-global port ID contains a node number in the range 0 to 127.

non-D operand: A non-D register used as an operand in a parallel processor instruction.

noninterlaced graphics mode: A mode for the video controller (VC) in which each frame consists of a single vertical field. A method of scanning out a video display where all of the lines in the frame are scanned out sequentially, one right after the other. Also called *progressive scan*.

noninterlaced mode: A mode for the video controller (VC) in which each frame consists of a single vertical field.

nonmaskable interrupt: An interrupt that can be neither masked nor disabled.

NPAR: See *next program address register.*

NTSC: See *National Television Standards Committee*.

O

object file: A set of related records treated as a unit that is the output of an assembler or compiler and is input to a linker.

object format converter: A program that converts common object file format (COFF) object files into Intel-format, Tektronix-format, TI-tagged-format, or Motorola-S-format object files.

object library: An archive library made up of individual object files.

OE: *Receiver register overrun indicator bit*. A bit within the I/O status register (IOSR) which indicates whether overrun has occurred in the receiver of the asynchronous serial port; that is, whether an unread character in the asynchronous data transmit and receive register (ADTR) has been overwritten by a new character. (*TMS320C2xx)*

off-chip: A device external to the device.

off-chip address: An address external to the chip. Addresses from 0x0200 0000 to 0xFFFF FFFF are off-chip addresses. See also *on-chip address*.

on-chip: An element or module internal to the device.

on-chip address: An address internal to the multimedia video processor (MVP) chip. Addresses from 0x0000 0000 to 0x1FFF FFFF are on-chip addresses. See also *off-chip address*.

offset-guided look-up table transfer: Type of guided transfer in which the guide table consists of values to be left-shifted (zero-filled) by zero, one, two, or three bits and added to a base address given in the packet transfer parameters to form the starting address of each patch. See also *guided transfer*.

offset-guided transfer: Type of source-guided transfer in which the guide table consists of values to be added to a base address given in the packet transfer parameters to form the starting address of each patch. See also *guided transfer*.

opcode: *Operation code.* In most cases, the first byte of the machine code that describes the type of operation and combination of operands to the central processing unit (CPU).

open-collector output: An output circuit that actively drives only low logic levels.

operand: The part of an instruction that designates where the central processing unit (CPU) will fetch or store data. The operand consists of the arguments, or parameters, of an assembly language instruction, assembler directive, or macro directive.

operand-fetch phase: The third phase of the pipeline; the phase in which an operand or operands are fetched from memory. See also *pipeline*.

operation: 1) A defined action; namely, the act of obtaining a result from one or more operands in accordance with a rule that completely specifies the result of any permitted combination of operands. 2) The set of such acts specified by a rule, or the rule itself. 3) The act specified by a single computer instruction. 4) A program step undertaken or executed by a computer, e.g., addition, multiplication, extraction, comparison, shift, transfer, etc. 5) The specific action performed by a logic element.

operation class: Specific multiplexer setting combinations that cause the same arithmetic logic unit (ALU) function to perform various distinct operations by controlling the routing of operands to the ALU. Eight operation classes are supported by the base set of ALU operations.

optimizer: A software tool that improves the execution speed and reduces the size of C programs.

optimization: Improvement in the execution speed of a program or in the reduction of the size of C programs.

options: Command parameters that allow you to request additional or specific functions when you invoke a software tool.

optional header: A portion of a common object file format (COFF) object file that the linker uses to perform relocation at download time.

output data-scaling shifter: A 32- to 16-bit barrel left shifter. Shifts the 32-bit accumulator output from 0 to 7 bits left for quantization management, and outputs either the 16-bit high or low half of the shifted 32-bit data to the data write bus. Also called *output shifter*.

output module: A linked, executable object file that is downloaded and executed on a target system.

output section: A final, allocated section in a linked, executable module.

overflow: A condition in which the result of an arithmetic operation exceeds the capacity of the register used to hold that result.

overflow flag (OV) bit: A status bit that indicates whether or not an arithmetic operation has exceeded the capacity of the corresponding register. 2) Bit 12 of status register ST0; indicates whether the result of an arithmetic operation has exceeded the capacity of the accumulator. (*TMS320C24x)*

overflow (in a register): A condition in which the result of an arithmetic operation exceeds the capacity of the register used to hold that result.

overflow (in the synchronous serial port): A condition in which the receive FIFO buffer of the port is full and another word is received in the receive shift register (RSR). (None of the contents of the FIFO buffer are overwritten by this new word.) (*TMS320C2xx*)

overflow mode (OVM) bit: A 1-bit field that determines if an overflow in the arithmetic logic unit (ALU) wraps around or saturates. This bit is stored in status register 0 (ST0).

overflow mode: This mode determines the behavior of the accumulator in the event of an overflow. In saturation mode, an overflow in the accumulator causes the accumulator to be loaded with a preset value. If the overflow is in the positive direction, the accumulator is loaded with its most positive number. If the overflow is in the negative direction, the accumulator is filled with its most negative number.

overlay page: A section of physical memory that is mapped into the same address range as another section of memory. A hardware switch determines which range is active.

overlay mode: *Mixed video mode*. The input from the video graphics array (VGA) pass-through cable is mixed with the random-access memory digital-to-analog (RAMDAC) converter output to form video overlaid onto VGA.

overrun: A condition in the receiver of the asynchronous serial port. Overrun occurs when an unread character in the asynchronous data transmit and receive register (ADTR) is overwritten by a new character.

OV: See *overflow (OV) bit*.

OVF bit: See *overflow (OV) bit*.

overflow (OV) bit: *(Synchronous serial port).* A bit within the synchronous serial port control register (SSPCR) that indicates when the receive FIFO buffer of the port is full and another word is received in the receive shift register (RSR). The contents of the FIFO buffer are not overwritten by this new word. (*TMS320C2xx*)

OVLY: See *RAM overlay (OVLY) bit*.

P

P × 64: A video teleconferencing standard designed by the Consultative Committee for International Telephony and Telegraphy (CCITT) to permit full duplex video displays over data lines that have a bit rate of P × 64, where 1 < P < 30.

PAB: See *program-address bus*.

packed bytes: Four bytes contained in a 32-bit word. The individual bytes within a word of packed bytes are often operated on in parallel using multiple-byte arithmetic.

packed halfwords: Two halfwords contained in a 32-bit word. The individual bytes within a word of packed halfwords are often operated on in parallel using multiple-halfword arithmetic.

packet: A collection of patches of data. See also *patch*.

packet transfer access mode (PAM): A mode that modifies the method for writing source data to the destination, including normal, peripheral device transfer, block write, serial register transfer (SRT), and 8-bit, 16-bit, 32-bit, and 64-bit source transparency.

packet transfer (PT): A transfer of data blocks between two areas of memory. The multimedia video transfer (MVP) supports packet transfers of one, two, or three dimensions. See also *dimensioned transfer*, *guided transfer*.

packet transfer request: An I/O request submitted to the transfer controller (TC) that is issued when a block of data is to be moved through packet transfer. Packet transfer requests can be submitted by the master processor, the parallel processors, the video controller (VC), or an external device.

PAER: See *block repeat program address end register*.

PAL: See *phase alternation line*.

PAM: See *packet transfer access mode.*

PAR: See *program address register.*

parallel debug manager (PDM): A program used for creating and controlling multiple debuggers for the purpose of debugging code in a parallel-processing environment. (*TMS320C27x*)

parallel logic unit (PLU): A 16-bit logic unit that executes logic operations from long immediate operands or from the contents of the dynamic bit manipulation register (DBMR) directly upon data locations without affecting the contents of the accumulator (ACC) or product register (PREG).

parallel port: The parallel printer port interface is primarily used for connecting printers to the computer system, although the parallel port can also be used for other peripherals. In this case, the ’C3x digital signal processor starter kit (DSK) is connected to the parallel printer port. *(TMS320C3x*)

parallel processor (PP): An advanced digital signal processor that is used for video compression/decompression (P$\times$64 or MPEG), still-image compression/decompression (JPEG), 2-D and 3-D graphic functions such as line draw, trapezoid fill, antialiasing, and a variety of high-speed integer operations on image data. A ’C8x single-chip multiprocessor device may contain from one to eight parallel processors, depending on the device version. (*TMS320C8x*)

parallel processor command interface: The software interface through which the master processor (or other client processor) issues commands to be executed by a server parallel processor.

parallel transfers: The address unit operations specified in parallel with a data unit operation.

parameter RAM: A general-purpose 2K-byte RAM that is associated with a specific processor, part of which is dedicated to packet transfer information and the processor interrupt vectors. (*TMS320C8x*)

parameter table: A group of parameters, eight doublewords long, that describe a data packet and how it is to be moved from source to destination. (*TMS320C8x*)

parser: A software tool that reads the source file, performs preprocessing functions, checks syntax, and produces an intermediate file that can be used as input for the optimizer or code generator.

partial linking: Linking files in several passes. Incremental linking is useful for large applications because you can partition the application, link the parts separately, and then link all of the parts together.

PASR: See *block repeat program address start register*.

patch: A group of lines of equal length whose starting addresses are an equal distance apart.

pba: The assembler keyword for the parallel processor-relative parameter RAM base address that can be used to set up address registers for parallel processor-independent code; pba corresponds to 0x0100 *n*000, where *n* is the parallel processor number.

PC: *Personal computer* or *program counter*. 1) In installation instructions or information relating to hardware and boards, *PC* means *personal computer* (as in IBM PC). 2) In general debugger and program-related information, *PC* means *program counter*, which is the register that identifies the current statement in your program.

PCA: See *printed-circuit assembly*.

PCB: *Printed circuit board*.

PC field: See *program counter (PC) field*.

PCI: See *peripheral component interconnect*.

PCM: See *pulse coded modulation mode (PCM) bit*.

PC register: The register that contains the address of the next instruction.

PDM: See *parallel debug manager.*

PDWSR: See *program/data wait-state register*.

pending interrupt: A maskable interrupt that has been successfully requested but is awaiting acknowledgement by the CPU.

periodic event: An event that repeats at regular intervals, as opposed to an event that either occurs only once or repeats at irregular intervals.

period (PRD) register: A memory-mapped register that specifies the period for the on-chip timer. When the timer counter register (TIM) is decremented past zero, the TIM is loaded with the value in the PRD.

peripheral bus: A bus that is used by the CPU to communicate the direct memory access (DMA) coprocessor, communication ports, and timers.

peripheral cable: A cable that is used to connect a peripheral to the software development board (SDB). Peripheral cables for the SDB include the video graphics array (VGA) pass-through cable, graphics output monitor cable, S-VHS-to-RCA adapter cable, and audio breakout cable.

peripheral component interconnect (PCI): A high-speed local bus that supports data-transfer speeds of up to 132M bytes per second at 33 MHz.

PFC: See *prefetch counter (PFC)*.

PGA: *Pin-grid array.*

physical address: The address that appears at the device address pins.

phase alternation line (PAL): A European deviation of the standard U.S. National Television Standards Committee (NTSC) signal with a format of 625 lines and a frequency of 50-Hz . See also *National Television Standards Committee*.

PIO mode: *Programmed input/output mode*. A mode of the audio codec in which direct memory access (DMA) is not used; rather, samples are directly read from or written to the PIO port.

pipeline: A method of executing instructions in an assembly line fashion.

pipelined-loop epilog: The portion of code that drains a pipeline in a software-pipelined loop. See also *epilog*.

pipelined-loop prolog: The portion of code that primes the pipeline in a software-pipelined loop. See also *prolog*.

pipelined mode: A master processor (MP) floating-point unit mode in which multiple MP floating-point instructions are in various stages of completion in the floating-point multiply and/or add unit simultaneously.

pipeline stall: Temporary halt to the normal fetching of operations. Events which cause a pipeline stall include: a cache-miss, an illegal operation detection, diversion of local port access to global port, a direct external access (DEA), and crossbar contention.

pipelining: A design technique for reducing the effective propagation delay per operation by partitioning the operation into a series of stages, each of which performs a portion of the operation. A series of data is typically clocked through the pipeline in sequential fashion, advancing one stage per clock period.

pitch: The number of bytes between the start of one line to the start of the next line in a frame of video.

PIXBLT: See *pixel-block transfer.*

pixel: One picture element (pel).

pixel-block transfer (PIXBLT): A pixel-array operation in which each pixel is represented by one or more bits. PIXBLTs are a superset of bitBLTs and include the commonly used Boolean functions as well as integer arithmetic and multibit operations. See also *bitBLT*.

pixel dropping: The process of removing pixels from a line of video to downscale that line.

PLL: *Phase lock loop circuit*.

PLA: Programmable logic array. (*TMS320C3x*)

playback mode: A mode of the audio subsystem in which direct memory access (DMA) transfers supply audio data for playback.

PLD: *Programmable logic device*.

PLU: See *parallel logic unit (PLU)*.

PM: See *product shift mode (PM) bits*.

pma: See *program memory address*.

PM bits: See *product shift mode (PM) bits*.

PMST: See *processor mode status register (PMST)*.

point: To move the mouse cursor until it overlays the desired object on the screen.

poll: A continuous test used by the program until a desired condition is met.

pool: See *message buffer pool*.

pop: Action of removing a word from a stack.

porch: The portion of a video display signal that corresponds to the blanking interval on either side of a horizontal or vertical synchronization pulse. Front porch refers to the blanking interval that precedes the sync pulse and back porch refers to the blanking interval that follows the sync pulse. See also *back porch, front porch*.

port: A type of shared data object that contains a queue of messages.

port address: The PC I/O memory space that the debugger uses for communicating with the emulator. The port address is selected through switches on the emulator board and communicated to the debugger with the –p debugger option.

port ID: A 32-bit value the kernel uses to identify a port it has opened. See also *ID*.

port table: A fixed-size table of pointers that the kernel uses to keep track of the ports it has opened.

POSTSCALER: *Postscaling shifter*. A 0- to 7-bit left barrel shifter used to postscale data coming out of the accumulator (ACC).

power-down mode: The mode in which the processor enters a dormant state and dissipates considerably less power than during normal operation. This mode is initiated by the execution of an IDLE instruction. During a power-down mode, all internal contents are maintained so that operation continues unaltered when the power-down mode is terminated. The contents of all on-chip RAM also remains unchanged.

PP: See *parallel processor*.

ppcl: A shell utility that invokes the multimedia video processor's (MVP's) parallel processor compiler, assembler, and linker to create an executable object file version of your parallel processor program.

pragma: A preprocessor directive that provides directions to the compiler about how to treat a particular statement.

PRD: See *timer period register*.

PRDB: *Program-read data bus*. A bus that provides data for program memory reads and is driven by the memories or the logic interface.

preempt: To interrupt the processing of a task to allow a more urgent task to begin executing.

prefetch counter (PFC): A register that prefetches program instructions. The PFC contains the address of the instruction currently being prefetched and is updated when a new prefetch is initiated.

PREG: See *product register (PREG).*

preprocessor: A software tool that interprets macro definitions, expands macros, interprets header files, interprets conditional compilation, and acts upon preprocessor directives.

PRESCALER: *Prescaling shifter*. A 0- to 16-bit left barrel shifter used to prescale data coming into the arithmetic logic unit (ALU). This shifter is also used as a 0- to 16-bit right barrel shifter of the accumulator (ACC). The shift count is specified by a constant in the instruction or by the value in temporary register 1 (TREG1).

prescaler counter (PSC): Bits within the timer control register (TCR) which specify the prescale count for the on-chip timer. See also *timer prescaler counter*. (*TMS320C2xx, TMS320C54x*)

present flag: A bit in the cache tag register associated with a cache subblock that indicates whether the information in the subblock is present in the cache.

printed-circuit assembly (PCA): A printed-circuit board on which separately manufactured component parts have been installed in an electrical circuit that performs a defined function.

private context: A portion of a task's context that is private to a particular software library or group of related functions and is hidden to the main task program and to the other libraries used by that program.

processor: The central processing unit (CPU) or microprocessor of the computer. In most instances, it refers to one or more chips that form the core brain of the computer.

processor mode status register (PMST): A memory-mapped register that contains status and control bits.

processor node: In a multiprocessor system, a processor that executes the multimedia video processor (MVP) executive and that is able to communicate with the other processors through the executive's internode message-passing mechanisms.

product register (PREG): A register that holds the output from the multiplier. The high and low words of the PREG can be accessed individually. See also *multiplier (MULT)*.

product-scaling shifter: A 32-bit shifter that performs a 0, 1, or 4-bit left shift, or a 6-bit right shift of the multiplier product. The left-shift options are used to manage the additional sign bits resulting from the 2s-complement multiply. The right-shift option is used to scale down the number to manage the overflow of product accumulation in the central arithmetic logic unit (CALU).

product shift mode (PM) bits: A field that defines the product shifter (P-SCALER) mode. These two bits determine the shift value (0-, 1-, 4-bit left shifter, 6-bit right shifter) for the output of the product register (PREG).These bits are stored in status register 1 (ST1). (*TMS320C2xx, TMS320C24x, TMS320C5x*)

PROFILE window: A window that displays statistics about code execution. This window is available only when you are in the profiling environment. (This window is part of the graphical user interface for all TI debuggers.)

profiling: A technique used to determine how long a processor spends in each section of a program.

program address bus (PAB): An internal bus that provides the addresses for program-memory reads and writes. (*TMS320C2xx, TMS320C24x*)

program address register (PAR): A register that holds the address currently being driven on the program address bus for as many cycles as it takes to complete all memory operations scheduled for the current machine cycle.

program-address generation logic: Logic circuitry that generates the addresses for program memory reads and writes, and an operand address in instructions that require two registers to address operands. This circuitry can generate one address per machine cycle. See also *data-address generation logic.*

program control logic: Logic circuitry that decodes instructions, manages the pipeline, stores the status of operations, and decodes conditional operations.

program controller: Logic circuitry that decodes instructions, manages the pipeline, stores the central processing unit (CPU) status, and decodes conditional operations.

program counter (PC): A register that identifies the current statement in the program. The PC addresses program memory sequentially and always contains the address of the next instruction to be fetched. The PC contents are updated following each instruction decode operation.

program counter (PC) field: The 29-bit parallel processor or 30-bit master processor counter field within the 32-bit PC register that contains the address of the next instruction.

program/data wait-state register (PDWSR): A memory-mapped register that specifies the number of wait states for the program, data, and input/output (I/O) space. The higher byte of PDWSR specifies the data space wait states and the lower byte specifies the program space wait states. At reset, PDWSR = FFFF. (*TMS320C5x)*

program flow control unit: A unit that manages the opcode fetches from the parallel processor's instruction cache.

program-level optimization: An aggressive level of optimization where all of the source files are compiled into one intermediate file. Because the compiler can see the entire program, several optimizations are performed with program-level optimization that are rarely applied during file-level optimization.

programmable read-only memory (PROM): A large-scale integrated circuit chip for storing digital data. It can be erased with ultraviolet light and reprogrammed, or it can be programmed only once, either at the factory or in the field.

program memory: A memory region used for storing and executing programs.

program memory address (pma): A register that provides the address of a multiplier operand that is contained in program memory.

program read bus (PRDB): An internal bus that carries instruction code and immediate operands, as well as table information, from program memory to the CPU. (*TMS320C2xx, TMS320C24x*)

program-space wait-state (PSWS) bit: Bit 0 of the wait-state generator control register (WSGR). PSWS determines the number of wait states applied to reads from off-chip program memory space. (*TMS320C2xx*)

progressive scan: See *noninterlaced graphics mode*.

prolog: The portion of code in a function that sets up the stack. See also *pipelined-loop prolog*.

PROM: See *programmable read-only memory.*

protected mode: 32-bit extended DOS mode. These programs require an extended memory manager and run only on larger processors (’386 or better). They can use all the available RAM on the computer up to 64M bytes.

$\overline{\text{PS}}$: *Program select pin*. The DSP assert $\overline{\text{PS}}$ to indicate an access to external program memory.

PSC: See *prescaler counter;* also *timer prescaler counter*.

P-SCALER: See *product-scaling shifter*.

PSLWS: *Lower program-space wait-state bits.*

PSUWS: *Upper program-space wait-state bits.* A value in the wait-state generator control register (WSGR) that determines the number of wait states applied to reads from and writes to off-chip upper program space (addresses 8000h–FFFFh). PSUWS is not available on the ’C209; instead, see *program-space wait-state bit (PSWS)*. On other ’C2xx devices, PSUWS is bits 5–3 of the WSGR. See also *PSLWS*. (*TMS320C2xx, TMS320C24x*)

PSWS: See *program-space wait-state (PSWS) bit.*

PT: See *packet transfer*.

PT options field: Packet-transfer parameter field which selects the form of transfer for source and destination. It determines if the packet will end the linked list and enables the selection of additional features such as special transfer modes.

pulldown menu: A command menu that is accessed by name or with the mouse from the menu bar at the top of the debugger display.

pulse code modulation (PCM): A technique for digitizing speech by sampling the sound waves and converting each sample into a binary number.

pulse coded modulation mode (PCM) bit: A 1-bit field that enables/disables the buffered serial port (BSP) transmitter. This bit is stored in the BSP control extension register (SPCE).

push: Action of placing a word onto a stack.

Q

quiet run: Suppresses the normal banner and the progress information.

quantization error: The error resulting from converting an analog signal into a digital signal due to the fact that a digital signal can only have discrete values whereas an analog signal may take on any value within dynamic range of the signal.

quantum levels: When a signal can only take on certain discrete values, these values are referred to as quantum levels.

QNaN: *Quiet not-a-number.* A floating-point number with no numerical value that is used as a signal to the master processor in certain exception conditions.

R

RAMDAC: *Random-access memory digital-to-analog converter.* Used to convert digital RGB (red-green-blue) information to analog signals that drive a display.

RAMEN: See *RAM enable pin*.

RAM enable pin (RAMEN): This pin enables or disables on-chip single-access RAM. (*TMS320C2xx, TMS320C4x*)

RAM model: An autoinitialization model used by the linker when linking C code. The linker uses this model when you invoke the linker with the –cr option. The RAM model allows variables to be initialized at load time instead of runtime.

RAM overlay (OVLY) bit: A 1-bit field that determines if on-chip single-access RAM is addressable in data memory space. At reset, OVLY = 0. This bit is stored in the processor mode status register (PMST).

random-access memory (RAM): A memory element that can be written to, as well as read.

$\overline{\text{RAS}}$: *Row address strobe*. A memory interface signal that drives the row address strobe inputs of dynamic RAM (DRAM) and/or video RAM (VRAM).

raster: The series of scan lines that comprise a television picture or a computer's display. A raster line is the same as a scan line, which is an individual sweep across the face of the display by the electron beam that makes the picture.

raster-op: A raster operation, which is an arithmetic or logical combination of the source and destination data that takes place during the transfer of a pixel array from one location to another.

raw data: Executable code or initialized data in an output section.

RC: See *repeat counter register*.

RCA connector: A connector used for attaching audio and video devices such as stereo equipment or a composite video monitor to a computer's video adapter.

RCA jack: The female portion of an RCA connector usually located on audio or video equipment.

$\overline{\text{RD}}$: See *read select pin*.

REA: See *block repeat program address end register*.

read-only memory (ROM): A semiconductor storage element containing permanent data that cannot be changed.

read select pin ($\overline{\text{RD}}$): The DSP asserts $\overline{\text{RD}}$ to request a read from external program, data, or I/O space. $\overline{\text{RD}}$ can be connected directly to the output enable pin of an external device.

read/write (R/$\overline{\text{W}}$) pin: This memory-control signal indicates the direction of transfer when communicating to an external device.

ready: A task state indicating that the task either is currently executing or is able to execute as soon as it acquires the processor.

READY: *External device ready pin*. Used to create wait states externally. When this pin is driven low, the device waits one CPU cycle and then tests READY again. After READY is driven low, the device does not continue processing until READY is driven high.

ready queue: A linked list that contains the descriptors for all tasks that are in the READY state.

real mode: 16-bit native MS-DOS mode. This mode limits the available memory to 640K bytes. Calls to DOS may involve switching from protected to real mode. *DOS real-mode tools are no longer supported by the TMS320C3x/C4x code generation tools.*

real time: The actual time during which the physical process of a computation transpires in order that results of the computation interact with the physical process.

real-time processing: The mechanisms required for ensuring that operations on a computer system are completed within strict time intervals.

real-time system: A system in which each processing job is completed by a specified deadline. A real-time system is characterized not so much by its best-case speeds as by its worst-case delays, which must be specified to guarantee job completion by a given time.

receive buffer half received (RH) bit: A 1-bit buffered serial port (BSP) flag that indicates which half of the receive buffer has been received. At reset, RH = 0. This bit is stored in the BSP control extension register (SPCE).

receive clock input (CLKR) pin: A pin that receives an external clock signal to clock data from the serial data receive (DR) pin into the synchronous serial port receive shift register (RSR). (*TMS320C2xx*)

receive FIFO buffer not empty (RFNE) bit: A bit within the synchronous serial port control register (SSPCR) that indicates whether the receive FIFO buffer of the synchronous serial port contains data to be read. (*TMS320C2xx*)

receive frame synchronization (FSR) pin: An input pin that accepts a frame sync pulse that initiates the reception process of the synchronous serial port.

receive interrupt (asynchronous serial port): An interrupt (TXRXINT) caused during reception by any one of the following events: the aynchronous data transmit and receive register (ADTR) holds a new character; overrun occurs; a framing error occurs; a break has been detected on the RX pin; a character *A* or *a* has been detected in the ADTR by the automatic baud-rate detection logic. (*TMS320C2xx*)

receive interrupt mask bit (RIM): A bit within the asynchronous serial port control register (ASPCR) that enables or disables receive interrupts of the asynchronous serial port. (*TMS320C2xx*)

receive interrupt (synchronous serial port) (RINT): An interrupt (RINT) generated during reception based on the number of words in the receive FIFO buffer. The trigger condition (the desired number of words in the buffer) is determined by the values of the receive-interrupt bits (FR1 and FR0) of the synchronous serial port control register (SSPCR). (*TMS320C2xx*)

receive (RX) pin (asynchronous serial port): During reception in the asynchronous serial port, this pin accepts a character one bit at a time, transferring it to the asynchronous serial port receive shift register (ARSR). (*TMS320C2xx*)

receive (DR) pin (synchronous serial port): A synchronous serial port pin that receives serial data. As each bit is received at DR, the bit is transferred serially into the receive shift register (RSR). (TMS320C2xx)

receive ready (RRDY) bit: A 1-bit flag that transitions from 0 to 1 to indicate the data receive shift register (RSR) contents have been copied to the data receive register (DRR) and that data can be read. A receive interrupt (RINT) is generated upon the transition. The RRDY bit can be polled in software instead of using serial port interrupts. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC).

receive register (asynchronous serial port) (ADTR): A register in the asynchronous serial port that writes the data to transmit and reads the data received. See also *asynchronous serial port receive shift register*. (*TMS320C2xx*)

receive register (synchronous serial port) (SDTR): An I/O-mapped read/write register that sends data to the transmit FIFO buffer and extracts data from the receive FIFO buffer. (*TMS320C2xx*)

receive reset (RRST) bit: A bit within the serial port control register that resets the receiver portion of the serial port.

receiver reset ($\overline{\text{RRST}}$) bit: A 1-bit flag that resets the serial port receiver. At reset, $\overline{\text{RRST}}$ = 0. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC).

receive shift register (asynchronous serial port): See *ARSR*.

receive shift register full (RSRFULL) bit: A 1-bit flag that indicates if the serial port receiver has experienced overrun. This bit is stored in the serial port control register (SPC).

receive shift (RSR) register (synchronous serial port): Shifts data serially into the synchronous serial port from the DR pin. See also *XSR*.

reclamation port: The message port to which a message buffer is returned when the message is discarded. The buffer containing the message is then available to send another message. See also *port ID*.

reconnect: A function used by a target to select an initiator to resume processing after it has been disconnected.

reduced instruction set computer (RISC): A computer whose instruction set and related decode mechanism are much simpler than those of microprogrammed complex instruction set computers. The result is a higher instruction throughput and a faster real-time interrupt service response from a smaller, cost-effective chip.

redundant loops: Two versions of the same loop, where one is a software-pipelined loop and the other is an unpipelined loop. Redundant loops are generated when the TMS320C6x tools cannot guarantee that the trip count is large enough to pipeline a loop for maximum performance.

reentrant code: Program code that can be executed concurrently by more than one task. Reentrant code contains no task-specific data.

refresh: A method of restoring the charge capacitance to a memory device, such as a dynamic RAM (DRAM) or video RAM (VRAM), or of restoring memory contents.

refresh rate: The speed with which a video source redisplays the screen.

register: A small area of high speed memory, located within a processor or electronic device, that is used for temporarily storing data or instructions. Each register is given a name, contains a few bytes of information, and is referenced by programs.

register file: A bank of registers.

relocation: A process in which the linker adjusts all the references to a symbol when the symbol's address changes. Also refers to the linker's process of placing each output section in memory.

remote procedure call (RPC): A procedure (or function) call that is executed on a processor other than the one on which the call originated. See also *stub routine*.

repeat counter (RC) register: A register in the CPU register file that specifies the number of times minus one that a block of code is to be repeated when a block repeat is performed.

repeat mode: A zero-overhead method for repeating the execution of a block of code. Using repeat modes allows time-critical sections of code to be executed in the shortest possible time.

reply message: A message sent by a server in reply to a request message from a client.

reply port: The message port to which a reply to a request message is to be sent. See also *port ID*.

request message: A message sent by a client to request service from a server.

reserved (R): A term used for a bit-, byte-, field-, or coded-value that is set aside for future small computer system interface (SCSI) standardization.

reset: A means to bring processors to known states by setting registers and control bits to predetermined values and signaling execution to start at a specified address.

reset asynchronous serial port (URST) bit: A bit within the asynchronous serial port control register (ASPCR) that resets the asynchronous serial port. (*TMS320C2xx)*

reset pin ($\overline{\text{RS}}$, also RS on 'C209): This pin causes a reset.

reset vector: The interrupt vector for reset.

resource: See *kernel resource*.

resource ID: A 32-bit value the kernel uses to identify a port, semaphore, or task it has opened or created. See also *ID*.

resource table: A fixed-size table of pointers that the kernel uses to keep track of the internal resources it has opened or created. See also *kernel resource*.

resume: To make a suspended task ready to execute again.

retrace: A line traced by the scanning beam(s) of a display screen as it travels from the end of one horizontal line (vertical field) to the beginning of the next horizontal line (vertical field).

return address: The address of the instruction to be executed when the CPU returns from a subroutine or interrupt service routine.

reverse assembly: The process of translating the contents of memory from machine language to assembly language (also known as disassembly).

RFNE bit: See *receive FIFO buffer not empty (RFNE) bit*.

RH: See *receive buffer half received (RH) bit*.

rightmost 1 (rmo): The operation that returns the bit position of the rightmost 1. In the master processor, it is an actual instruction, while in the parallel processor, it is a bit-detection function.

rightmost-bit change (rmbc): The parallel processor operation that returns the position of the rightmost bit that has a value different from bit 0. The overflow status bit is set if all bits in the source are identical.

RIM bit: See *receive interrupt mask bit (RIM).*

RINT: See *receive interrupt (synchronous serial port) (RINT)*.

ripple-carry output signal: An output signal from a counter indicating that the counter has reached its maximum value.

RISC: See *reduced instruction set computer*.

rmbc: See *rightmost-bit change.*

rmo: See *rightmost 1.*

ROMEN: See *ROM enable*.

ROM enable (ROMEN): An external pin that determines whether or not the the on-chip ROM is enabled. (*TMS320C4x*)

ROM model: An autoinitialization model used by the linker when linking C code. The linker uses this model when you invoke the linker with the –c option. In the ROM model, the linker loads the .cinit section of data tables into memory and initializes the variables at runtime.

ROM width: The width (in bits) of each output file, or, more specifically, the width of a single data value in the file. The ROM width determines how the TI Hex conversion utility partitions the data into output files. After the target words are mapped to memory words, the memory words are broken into one or more output files. The number of output files is determined by the ROM width.

round-robin scheduling: A method for scheduling the execution of a set of tasks of equal priority. The tasks share the processor on a rotating basis. Each of the tasks takes its turn executing for a time interval that is roughly equal for all tasks.

routing port: In a multiprocessor system, a local port through which the kernel of the multimedia video processor (MVP) executive routes messages that are destined for a particular foreign processor node. See also *message-routing table*.

RPC: See *remote procedure call*.

RPTB: *Repeat block*.

RRDY: See *receive ready (RRDY) bit*.

RRST: See *receive reset (RRST) bit*.

RSA: See *block repeat program address start register*.

RSR: See *receive shift (RSR) register*.

RSRFULL: See *receive shift register full (RSRFULL) bit*.

run address: The address where a section runs.

runtime environment: The runtime parameters in which your program functions. These parameters are defined by the memory and register conventions, stack organization, function call conventions, and system initialization.

runtime-support functions: Standard ANSI functions that perform tasks that are not part of the C language (such as memory allocation, string conversion, and string searches).

runtime-support library: A library file that contains the source for the runtime-support functions.

R/$\overline{W}$: See *read/write pin*.

RX pin: See *receive (RX) pin (asynchronous serial port)*.

S

SAM: See *serial access memory*.

SAMINC: See *serial access memory increment*.

SAMMASK: See *serial access memory mask*.

SAM overflow event: In the video controller (VC), a serial access memory overflow event generated by the serial register transfer (SRT) controller that determines when cycles need to be performed to service the inactive half of the split serial access memory (SAM).

sample rate: The rate at which the audio codec samples audio data. Usually specified in hertz (samples per second).

SARAM: See *single-access RAM*.

scalar type: A C programming type in which the variable is a single variable, not composed of other variables.

scan chain: A shift register made up of the logic storage elements (stand-alone bit-storage devices). In test mode, the storage elements are connected in a shift register. During normal operation they carry out their normal system functions. The scan path is used to shift test data into the logic storage elements for controllability and to shift out test response data for observability. (Also called *scan path*.)

scheduler: Also *task scheduler*. The portion of the kernel that is responsible for determining the order in which the tasks in the ready queue are executed.

scheduling: The strategy used in an operating system to share a resource such as a processor or memory.

SCLK: See *serial clock*.

scratch-pad RAM: Another name for dual-access RAM (DARAM) block B2 in data space (32 words). (*TMS320C2xx, TMS320C24x, TMS320C5x*)

script: A file that contains a set of shell commands.

scrolling: A method of moving the contents of a window up, down, left, or right to view contents that weren't originally shown.

SCSI: *Small computer system interface*.

SCSI address: A unique address (0–7) assigned to a small computer system interface (SCSI) device.

SCSI device: A host computer, peripheral controller, or intelligent peripheral unit that is connected to the small computer system interface (SCSI) bus.

SCSI ID: The bit-significant representation of a small computer system interface (SCSI) address (this bit address is associated with a bit number of the data bus).

SDB: *TMS320C8x software development board*.

SDTR: *Synchronous data transmit and receive register.* See *receive (SDTR) register*.

section: A relocatable block of code or data that ultimately occupies a space adjacent to other blocks of code in the memory map.

section header: A portion of a common object file format (COFF) object file that contains information about a section in the file. Each section has its own header. The header points to the section's starting address, contains the section's size, and so forth.

section program counter (SPC): An element in the assembler that keeps track of the current location within a section; each section has its own SPC.

semaphore: A classic method for restricting access to shared resources (for example, storage) in a multiprocessing environment. A semaphore is a protected variable (or abstract data type) that can be accessed only by certain operations for testing and incrementing the value of the variable.

semaphore ID: A 32-bit value that the kernel uses to identify a semaphore that it has opened. See also *ID*.

semiomnipresent pixel: A pixel that appears to be at two locations on the screen at once in a video display.

semaphore table: A fixed-size table of pointers that the kernel uses to keep track of the semaphores that it has opened.

sequential mode: A master processor (MP) floating-point unit mode in which the MP executes a single floating-point instruction to completion before starting another floating-point instruction.

serial access memory (SAM): A memory array in video RAM (VRAM) that can be accessed through serial register transfer cycles. See *SRT controller*, *video random access memory (VRAM)*.

serial access memory increment (SAMINC): A 32-bit control mask used by the serial register transfer (SRT) controller for address calculation. This mask contains a 1 in the bit position above the most significant 1 in the serial access memory mask (SAMMASK) register.

serial access memory mask (SAMMASK): A serial register transfer (SRT) controller register that contains a string of continuous 1s. The number and position of these 1s depend on the video RAM (VRAM) serial access memory (SAM) width and the address lines connected to the VRAM.

serial clock (SCLK): An input clock signal used by the serial register transfer (SRT) controller to track the video RAM (VRAM) tap point.

serial data receive (DR) pin: A synchronous serial port pin that receives serial data. As each bit is received at DR, the bit is transferred serially into the receive shift register (RSR).

serial data transmit (DX) pin: The pin on which data is transmitted serially from the synchronous serial port; accepts a data word one bit at a time from the transmit shift register (XSR).

serial port: A DSP peripheral used for sending and receiving data samples sequentially in order to communicate with serial devices such as, A/D and D/A converters and codecs, microprocessors, and DSPs. See also *serial port interface*.

serial-port control register (SPC): A memory-mapped register that contains status and control bits for the serial-port interface. The SPC is identical to the time-division multiplexed (TDM) serial-port control register (TSPC), except that bit 0 is reserved for the TDM bit.

serial-port interface: An on-chip full-duplex serial-port interface that provides direct serial communication to serial devices with a minimum of external hardware, such as codecs and serial analog-to-digital (A/D) converters. Status and control of the serial port is specified in the serial port control register (SPC).

serial port receive interrupt (RINT) bit: A 1-bit flag that indicates the data receive shift register (RSR) contents have been copied to the data receive register (DRR). This bit is stored in the interrupt flag register (IFR).

serial port transmit interrupt (XINT) bit: A 1-bit flag that indicates that the contents of the data transmit register (DXR) have been copied to the data transmit shift register (XSR). This bit is stored in the interrupt flag register (IFR).

serial register transfer (SRT) controller: Hardware that schedules requests to the transfer controller to move data into and out of video RAM (VRAM) frame memories.

server: A program or task that provides services to a client program or task.

SETBRK: A bit within the asynchronous serial port control register (ASPCR) that selects the output level (high or low) on the asynchronous transmit (TX) pin when the port is not transmitting. (*TMS320C2xx*)

shared-access mode (SAM): The mode that allows both the DSPand the host to access host port interface (HPI) memory. In this mode, asynchronous host accesses are synchronized internally and, in case of conflict, the host has access priority and the DSP waits one cycle.

shared-access mode (SMOD) bit: A 1-bit field that enables/disables the shared access mode (SAM). This bit is stored in the host port interface (HPI) control register (HPIC). See also *shared-access mode (SAM)* and *host-only mode (HOM)*.

shared RAMs: Memory that can be shared by TMS320C8x's processors. This consists of the parallel processor data RAMs and the parallel processor parameter RAMs. (*TMS320C8x*)

shell program: A utility that lets you compile, assemble, and optionally link in one step. The shell runs one or more source modules through the compiler (including the parser, optimizer, and code generator), the assembler, and the linker.

shifter: A unit that shifts bits in a word to the left or to the right. See also *P-SCALER*.

short-floating-point format: A 16-bit representation of a floating-point number with a 12-bit mantissa and a 4-bit exponent.

short immediate: On the master processor (MP), a 15-bit signed or unsigned integer provided by MP instructions as one of the operands within a 32-bit instruction format.

short-immediate value: An 8-, 9-, or 13-bit constant given as an operand of an instruction that is using immediate addressing.

short offset: Unsigned 3-bit immediate index for halfword or word transfers; unsigned 4-bit immediate index for byte transfers. A short offset can be used in an addressing mode for any other operations specified in parallel in the instruction.

short integer format: A 2s-complement,16-bit format for integer data.

short unsigned-integer format: A 16-bit unsigned format for integer data.

side effects: A feature of C expressions in which using an assignment operator in an expression affects the value of one of the components used in the expression.

signal: To increment the count at a semaphore. See also *semaphore*.

signal event: The event caused by the arrival of a signal at a semaphore. If a task is waiting for the event, that task is scheduled to begin executing.

sign bit: The most significant bit (MSB) of a value when it is seen by the CPU to indicate the sign (negative or positive) of the value.

sign-extend: To fill the unused most significant bits (MSBs) of a value with the value's sign bit.

sign extension: An operation that fills the high order bits of a number with the sign bit.

sign-extension mode (SXM) bit: A 1-bit field that enables/disables sign extension of an arithmetic operation. This bit is stored in status register 1 (ST1).

simulator: A development tool that simulates the operation of the device for executing and debugging applications programs by using the device debugger.

single-access RAM (SARAM): Memory space that only can be read from or written to in a single clock cycle; RAM that can accessed (read from or written to) once in a single CPU cycle.

single-precision floating-point: 32-bit floating-point number.

single-precision floating-point format: A 32-bit representation of a floating point number with a 24-bit mantissa and an 8-bit exponent.

single-precision integer format: A 2s-complement 32-bit format for integer data.

single-precision unsigned-integer format: A 32-bit unsigned format for integer data.

single-step: A form of program execution that allows you to see the effects of each statement. The program is executed statement by statement; the debugger pauses after each statement to update the data-display windows.

single-threaded: A method of programming in which only a single thread or program element executes on a processor at any one time. This is in contrast to a multitasking system in which multiple tasks run concurrently on a single processor.

skew: Time differences in multiple clock signals based on physical distances between the origin of the signals and their destinations. Switching delays caused by gates in the logic.

slave phase: See *latch phase*. (*TMS320C2xx*)

SNaN: *Signaling not-a-number.* A floating-point number that has no numerical value but is used to signal the master processor in certain exception conditions.

Soft bit: A 1-bit field used in conjunction with the Free bit to determine the state of the serial port or timer when a breakpoint is encountered in the high-level language debugger. At reset, Soft = 0.

software interrupt: An interrupt caused by the execution of an INTR, NMI, or TRAP instruction.

software pipelining: A technique used by the C optimizer and the assembly optimizer to schedule instructions from a loop so that multiple iterations of the loop execute in parallel.

software stack: A program control feature that allows you to extend the hardware stack into data memory with the PSHD and POPD instructions. The stack can be directly stored and recovered from data memory, one word at time. This feature is useful for deep subroutine nesting or protection against stack overflow.

software write: A write to the destination register specified in the master processor or parallel processor instruction. Software writes take precedence over writes performed automatically by hardware, such as the increment of the program counter or the setting of arithmetic logic unit (ALU) status.

source file: A file that contains C code or assembly language code that is compiled or assembled to form an object file.

SMOD: See *shared-access mode (SMOD) bit*.

SPC: See *section program counter* or *serial-port-control register*.

SPCE: See *BSP control extension register (SPCE)*.

spinning: A technique for continuous monitoring of a status flag in a register or memory location in which the processor repeatedly polls the flag until the awaited status change occurs.

split ALU: See *multiple arithmetic*.

split mode: A mode of operation of the direct memory access (DMA) coprocessor that allows one DMA channel to service both the receive and transmit portions of a communication port.

split multiply: A parallel processor operation that performs two simultaneous 8-bit by 8-bit multiplies. The parallel processor multiplier can perform two 8-bit unsigned by 8-bit unsigned multiplies or two 8-bit unsigned by 8-bit signed multiplies.

SRAM: See *static random access memory*.

SRAM banks: *Static random access memory banks*. These include parameter and data RAM and instruction and data caches.

SRT controller: See *serial register transfer (SRT) controller*.

SSPCR: See *synchronous serial port control register.*

ST0 and ST1: See *status registers ST0 and ST1*.

ST: See *status register*.

standalone preprocessor: A software tool that expands macros, #include files, and conditional compilation as an independent program. It also performs integrated preprocessing, which includes parsing of instructions.

standalone simulator: A software tool that loads and runs an executable COFF .out file. When used with the C I/O libraries, the standalone simulator supports all C I/O functions with standard output to the screen.

stack: A block of memory reserved for storing return addresses for subroutines and interrupt service routines.

stack pointer: A special-purpose 32-bit register that contains (points to) the address of the top of the system stack.

start bit: Every 8-bit data value transmitted or received by the asynchronous serial port must be preceded by a start bit, a logic 0 pulse. (*TMS320C2xx*)

state: See *task state*.

static random-access memory (SRAM): Fast memory that does not require refreshing, as DRAM does. It is more expensive than DRAM, though, and is not available in as high a density as DRAM.

static variable: A kind of variable whose scope is confined to a function or a program. The values of static variables are not discarded when the function or program is exited; their previous value is resumed when the function or program is reentered.

status: One byte of information sent from a target to an initiator on completion of a command.

status bit: A bit in a status word or register that contains a single piece of status information. (*TMS320C8x*)

status register (ST): A register in the CPU register file that contains global information related to the CPU.

status registers ST0 and ST1: Two 16-bit registers that contain bits for determining processor modes, addressing pointer values, and for indicating various processor conditions and arithmetic logic results. These registers can be stored into and loaded from data memory, allowing the status of the machine to be saved and restored for subroutines. (*TMS320C2x/C2xx/C5x/C54xx*)

STB bit: *Stop bit selector*. A bit within the asynchronous serial port control register (ASPCR) that selects the number of stop bits (one or two) used in transmission and reception. (*TMS320C2xx*)

stop bit: Every 8-bit data value transmitted or received by the asynchronous serial port must be followed by one or two stop bits, each a logic 1 pulse. The number of stop bits required depends on the stop bit selector (STB) bit of the asynchronous serial port control register (ASPCR).

storage class: Any entry in the symbol table that indicates how a symbol should be accessed.

$\overline{\text{STRB}}$: See *external access active strobe*.

string table: A table that stores symbol names that are longer than eight characters. Symbol names of eight characters or longer cannot be stored in the symbol table; instead, they are stored in the string table. The name portion of the symbol's entry points to the location of the string in the string table.

structure: A collection of one or more variables grouped together under a single name.

subblock: See *cache subblock*.

subblock miss: A cache miss where the desired block is present but the desired subblock is not; results in a pipeline stall until the required subblock is brought into cache.

subroutine: A routine that is called from an applications program by means of a standard function call but that does not itself execute the specified function. See also *remote procedure call (RPC)*.

subsection: A relocatable block of code or data that ultimately occupies contiguous space in the TMS320C6200 memory map. Subsections are smaller sections within larger sections. Subsections give you tighter control of the memory map. (*TMS320C6200*)

substitution symbol table: A table that is maintained by the assembler during the assembler execution to track the text to be associated with given symbols.

supervisor mode: A mode in which the master processor (MP) has write access to all control registers and can write into the MP parameter RAM.

suspend: To halt further execution of a task indefinitely or until another task instructs the kernel to resume the suspended task.

S-VHS: *Super VHS (vertical helical scan).* Similar to the VHS video recording standard, except that the chrominance and luminance data are treated as components that provide higher quality video.

S-VHS-to-RCA adapter cable: A cable provided by TI that connects a video source to the software development board (SDB).

swap file: The file where virtual memory(secondary memory) is allocated on the hard disk.

SWDS: *Software Development System*. A PC-compatible plug-in board that provides a low-cost method of program evaluation and development.

SXM bit: See *sign-extension mode (SXM) bit*.

symbol: 1) A programmer-defined letter, numeral, sign, or other mark that represents the location of a particular datum item, instruction, routine, value, or address. 2) A string of alphanumeric characters that represents an address or a value.

symbolic debugging: The ability of a software tool to retain symbolic information that can be used by a debugging tool such as a simulator or an emulator.

symbol table: A portion of a common object file format (COFF) object file that contains information about the symbols that are defined and used by the file.

symbolic debugging: The ability of a software tool to retain symbolic information that can be used by a debugging tool such as a simulator or an emulator.

sync: A synchronization signal that tells the display where to put the picture. See also *horizontal sync* and *vertical sync*.

synchronous serial port control register (SSPCR): An I/O-mapped register that you write to when setting the configuration of the synchronous serial port and that you read when obtaining the status of the port. (*TMS320C2xx*)

synchronous serial port receive interrupt: A bit within the interrupt mask register that is tied to the receive interrupt for the synchronous serial port. It is internally generated by the serial port.

syntax: The grammatical and structural rules of a language. All higher-level programming languages possess a formal syntax.

system shell: A method implemented with the SYSTEM command, by which the debugger can blank the debugger display and temporarily exit to the DOS prompt. This allows you to enter DOS commands *or* allows the debugger to display information resulting from a DOS command.

T

T320C2xLP: *Texas Instruments configurable digital signal processor (cDSP) core.*

TADD: See *TDM address (TADD)*.

tag: 1) An optional type name that can be assigned to a structure, union, or enumeration. 2) A register holding the address of the cache block.

TAP: See *test access port*.

tap point: The address of the point at which data is shifted into or out of the video RAM's (VRAM's) serial I/O port. The serial register transfer (SRT) controller tracks the VRAM tap point using the serial clock (SCLK) input.

target: A small computer system interface (SCSI) device (usually a controller) that takes the actions requested by an initiator.

target memory: Physical memory in a device into which executable object code is loaded.

target system: The system on which the object code you have developed is executed.

task: A program element that executes concurrently with other program elements in a multitasking system.

task argument: The pointer value that is passed to a task as an argument at the time that the kernel begins executing the task.

task descriptor: A data structure that specifies a task's state, priority, function pointer, argument, and event flags. A task descriptor is allocated for each task at the time that the task is created.

task error: An error that occurs within a task during a call to a kernel function. In contrast to a system error that can affect the entire system, a task error has no direct effect on tasks other than the task in which the error occurred.

task function: The program code for a task, which is written in the form of a standard C function. The task scheduler in the executive's kernel begins executing a task by making a standard C function call to the task function.

task ID: A 32-bit value that the kernel uses to identify a task that it has created. See also *ID*.

task interrupt: A multimedia video processor (MVP) hardware mechanism through which the master processor (MP) cmnd instruction can signal a task interrupt to one or more parallel processors if their interrupts are enabled. The MP uses this mechanism to spawn tasks on the various parallel processors.

task priority: A number assigned to a task to indicate its relative urgency. The kernel of the multimedia video processor (MVP) executive allows you to assign a priority number in the range 0 to 31 to a task. Larger numbers represent higher (more urgent) priorities.

task scheduler: The portion of the kernel that is responsible for determining the order in which the tasks in the ready queue are executed.

task state: The state of a master processor (MP)-resident task running under the kernel of the multimedia video processor (MVP) executive. A task can be in one of four states: READY, WAITING, SUSPENDED, and WAITSUSPEND.

task table: A fixed-size table of pointers that the kernel uses to keep track of the tasks it has created.

TAZ: Tool-actuated zero insertion force (ZIF).

TC: See *transfer controller* or *test/control flag (TC) bit*.

TCLK: See *TDM clock*.

TCOMP: See *transmission complete bit*.

TCR: See *timer control register* or *timer counter register*.

TCSR: See *TDM channel select register*.

TDAT: See *TDM data*.

TDDR: See *timer divide-down register*.

TDM: See *time-division multiplexed (TDM) bit*.

TDM address (TADD): A single, bi-directional address line that identifies which devices on the four-wire serial bus should read in the data on the TDM data (TDAT) line.

TDM channel select register (TCSR): A memory-mapped register that specifies in which of the eight time slots (channels) a device on the four-wire serial bus is to transmit. A 1 in any one or more of bits 0–7 of the TCSR sets the device transmitter active during the corresponding time slot. Bits 8–15 are reserved.

TDM clock (TCLK): A single, bi-directional clock line for time-division multiplexed (TDM) operation. The TDM receive clock (TCLKR) and TDM transmit clock (TCLKX) pins are externally connected to form the TCLK line.

TDM data (TDAT): A single, bi-directional line from which all time-division multiplexed (TDM) data is carried. The TDM serial data receive (TDR) and TDM serial data transmit (TDX) pins are externally connected to form the TDAT line.

TDM data receive register (TRCV): A memory-mapped register that holds serial data copied from the time-division multiplexed (TDM) receive shift register (TRSR). When multiprocessing is enabled (TDM = 1), the TRCV is no longer available for software access as a memory-mapped register. See also *TDM data receive shift register (TRSR)*.

TDM data receive shift register (TRSR): A register that holds serial data received from the time-division multiplexed (TDM) data (TDAT) line. See also *TDM data receive register (TRCV)*.

TDM data transmit register (TDXR): A memory-mapped register that holds serial data to be copied to the data transmit shift register (XSR). When multiprocessing is enabled (TDM = 1), the TDXR is no longer available for software access as a memory-mapped register. See also *data transmit shift register (XSR)*.

TDM receive address register (TRAD): A memory-mapped register that contains various information regarding the status of the time-division multiplexed (TDM) address (TADD) line and verifies the relationship between instruction cycles and TDM port timing.

TDM receive interrupt (TRNT) bit: A 1-bit flag that indicates the time-division multiplexed (TDM) data receive shift register (TRSR) contents have been copied to the TDM data receive register (TRCV). This bit is stored in the interrupt flag register (IFR).

TDM receive/transmit address register (TRTA): A memory-mapped register that specifies to which device(s) on the four-wire serial bus a given device can transmit. The lower byte of the TRTA specifies the receive address (RA) of the device and the higher byte specifies the transmit address (TA). The address is sent over the time-division multiplexed (TDM) address (TADD) line.

TDM serial port control register (TSPC): A memory-mapped register that contains status and control bits for the time-division multiplexed (TDM) serial port interface. The TSPC is identical to the serial port interface control register (SPC), except for the TDM bit 0.

TDM transmit interrupt (TXNT) bit: A 1-bit flag that indicates the time-division multiplexed (TDM) data transmit register (TDXR) contents have been copied to the data transmit shift register (XSR). This bit is stored in the interrupt flag register (IFR).

TDXR: See *TDM data transmit register (TDXR)*.

TEC: *Texas Instruments embedded gate array*. A gate array embedded with a hardware macro.

temporary register (TREG): A register that holds one of the operands for a multiply operation; the dynamic bit position for the BITT instruction; or the dynamic shift count for the LACT, ADDT, and SUBT instructions.

temporary register 0 (TREG0): A memory-mapped register that holds an operand for the multiplier. See also *multiplier (MULT)*.

temporary register 1 (TREG1): A memory-mapped register that holds a dynamic prescaling shift count for data inputs to the arithmetic logic unit (ALU). See also *PRESCALER*.

temporary register 2 (TREG2:) A memory-mapped register that holds a dynamic bit pointer for the BITT instruction.

TEMT bit: See *transmit empty indicator*.

test access port (TAP): A standard communication port defined by IEEE standard 1149.1–1990 included in the device to implement boundary scan functions and/or to provide communication between the DSP and emulator.

test/control (TC) flag bit: A 1-bit flag that stores the results of the arithmetic logic unit (ALU) or parallel logic unit (PLU) test bit operations. The TC bit is affected by the APL, BIT, BITT, CMPR, CPL, LST #1, NORM, OPL, and XPL instructions. The status of the TC bit influences the execution of the conditional branch, call, and return instructions. This bit is stored in status register 1 (ST1). (*TMS320C2xx, TMS320C24x, TMS320C5x, TMS320C54x*)

.text section: One of the default common object file format (COFF) sections. The .text section is an initialized section that contains executable code. You can use the .text directive to assemble code into the .text section.

TGC: *Texas Instruments gate array*.

thread of execution: A schedulable unit of execution in a multitasking system. The term refers specifically to the progressive execution of a program element; it excludes other attributes, such as the system resources allocated to a task or process.

THRE bit: See *transmit register empty indicator*.

tightly coupled multiprocessor: A multiprocessor system in which the processors communicate with each other through shared memory, in-contrast to a loosely coupled multiprocessor system in which processors communicate over a network.

TIM bit: See *transmit interrupt mask (TIM) bit*.

time-division multiplexed (TDM): The process by which a single serial bus is shared by multiple devices with each device taking turns to communicate on the bus. The total number of time slots (channels) depends on the number of devices connected. During a time slot, a given device may talk to any combination of devices on the bus.

time-division multiplexed (TDM) bit: A 1-bit field that enables/disables the TDM serial port. This bit is stored in the TDM serial port control register (TSPC).

timer: A programmable peripheral used to generate pulses or to time events.

timer control register (TCR): A register that controls the operation of the on-chip timer.

timer counter register (TIM): A memory-mapped register that specifies the current count for the on-chip timer. The TIM is decremented once after each timer prescaler counter (PSC) decrement past 0. When the TIM is decremented past 0 or the timer is reset, the TIM is loaded with the contents of the timer period register (PRD) and an internal timer interrupt (TINT) is generated.

timer divide-down register (TDDR) bits: A field that specifies the timer divide-down ratio (period) for the on-chip timer. When the timer prescaler counter (PSC) is decremented past 0, the PSC is loaded with the contents of the TDDR. At reset, TDDR = 0000. These bits are stored in the timer control register (TCR).

timer interrupt (TINT): An interrupt generated by the timer on the next CLKOUT1 cycle after the main counter (TIM register) decrements to 0. (*TMS320C2xx, TMS320C5x, TMS320C54x*)

timer interrupt (TINT) bit: A 1-bit flag that indicates the timer counter register (TIM) has decremented past 0. This bit is stored in the interrupt flag register (IFR).

timer output (TOUT) pin: Provides access to an output signal based on the rate of the on-chip timer. On the next CLKOUT1 cycle after the main counter (TIM register) decrements to 0, a signal is sent to TOUT.

timer period register (PRD): A memory-mapped register that specifies the main period for the on-chip timer. When the timer counter register (TIM) is decremented past zero, the TIM is loaded with the value in the PRD. See also *TDDR*. (*TMS320C2xx, TMS320C24x, TMS320C5x, TMS320C54x*)

timer prescaler counter (PSC) bits: A field that specifies the count for the on-chip timer. When the PSC is decremented past 0 or the timer is reset, the PSC is loaded with the contents of the timer divide-down register (TDDR) and the timer counter register (TIM) is decremented. These bits are stored in the timer control register (TCR).

timer reload (TRB) bit: A 1-bit flag that resets the on-chip timer. When TRB = 1, the timer counter register (TIM) is loaded with the value in the timer period register (PRD) and the timer prescaler counter (PSC) is loaded with the value of the timer divide-down register (TDDR) bits. This bit is stored in the timer control register (TCR).

timer stop status (TSS) bit: A 1-bit flag that stops and restarts the on-chip timer. At reset, TSS = 0 and the timer immediately starts timing. This bit is stored in the timer control register (TCR).

time slicing: A method of multitasking in which each task is allotted a maximum amount of execution time, referred to as a time slice or quantum, before the next task is allowed to run.

TIM register: See *timer counter register (TIM)*.

TINT: See *timer interrupt*.

top of stack (TOS): Top level of the 8-level last-in, first-out hardware stack. (*TMS320C2xx*)

TOS: See *top of stack.*

totem-pole output: An output circuit that actively drives both high and low logic levels.

TOUT: See *timer output pin.*

TRAD: See *TDM receive address register.*

transfer controller (TC): The multimedia video processor's (MVP's) on-chip direct memory access (DMA) controller for servicing the cache and for transferring one-, two-, and three-dimensional data blocks between each processor on the MVP and its external memory.

transmission control (TCOMP) bit: A bit within the synchronous serial port control register (SSPCR); indicates when all data in the transmit FIFO buffer of the synchronous serial port has been transmitted. (*TMS320C2xx*)

transmit buffer half transmitted (XH) bit: A 1-bit flag that indicates which half of transmit buffer transmitted. The XH bit can be read when an XINT interrupt occurs (interrupt program or IFR polling). At reset, XH = 0. This bit is stored in the BSP control extension register (SPCE).

transmit clock input/output (CLKX) pin: A pin used to clock data from the synchronous serial port transmit shift register to the DX pin. If the serial port is configured to accept an external clock, this pin receives the clock signal. If the port is configured to generate an internal clock, this pin transmits the clock signal. (*TMS320C2xx*)

transmit empty indicator (TEMT bit): A bit within the I/O status register (IOSR) that indicates whether the asynchronous data transmit and receive register (ADTR) and/or the asynchronous serial port transmit shift register (AXSR) are full or empty. (*TMS320C2xx, TMS320C24x*)

transmit frame synchronization (FSX) pin: This input/output pin accepts and/or generates a frame sync pulse that initiates the transmission process of the synchronous serial port. If the port is configured for accepting an external frame sync pulse, the FSX pin receives the pulse. If the port is configured for generating an internal frame sync pulse, the FSX pin transmits the pulse.

transmit interrupt mask (TIM) bit: A bit within the asynchronous serial port control register (ASPCR) that enables or disables transmit interrupts of the asynchronous serial port. (*TMS320C2xx*)

transmit interrupt (serial port): An interrupt generated when the transmit register empties during transmission. This condition indicates that the trnasmit register is ready to accept a new transmit character. *(TMS320C2xx)*

transmit interrupt (synchronous serial port) (XINT): An interrupt generated during transmission based on the number of words in the transmit FIFO buffer. The trigger condition (the desired number of words in the buffer) is determined by the values of the transmit-interrupt bits (FT1 and FT0) of the synchronous serial port control register (SSPCR).

transmit mode (TXM) bit: 1) A 1-bit field that specifies the source of the frame synchronization transmit (FSX) pulse. At reset, TXM = 0. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC). 2) Bit 3 of the synchronous serial port control register (SSPCR); determines whether the source signal for frame synchronization is external or internal. (*TMS320C2xx*)

transmit ready (XRDY) bit: A 1-bit flag that transitions from 0 to 1 to indicate the data transmit register (DXR) contents have been copied to the data transmit shift register (XSR) and that data is ready to be loaded with a new data word. A transmit interrupt (XINT) is generated upon the transition. The XRDY bit can be polled in software instead of using serial port interrupts. This bit is stored in the serial port control register (SPC) and TDM serial port control register (TSPC).

transmit/receive interrupt: The CPU interrupt used to respond to a delta interrupt, receive interrupt, or transmit interrupt from the serial port. See also *delta interrupt*. *(TMS320C2xx)*

transmit register: A register used by the on-chip serial port. Data to transmit is written to the 8 least significant bits (LSBs) of the transmit register, and received data is read from the 8 LSBs of the transmit register.

transmit register empty indicator (THRE bit): A bit within the I/O status register (IOSR) that indicates when the contents of the asynchronous data transmit and receive register (ADTR) are transferred to the asynchronous serial port transmit shift register (AXSR). *(TMS320C2xx*)

transmit reset (XRST) bit: A bit within the synchronous serial port control register (SSPCR) that resets the transmitter portion of the synchronous serial port.

transmit shift register (serial port) (XSR): This register shifts data serially out of the serial port through the data transmit pin. See *asynchrounous serial port transmit shift register*. *(TMS320C2xx, TMS320C3x, TMS320C5x, TMS320C54x)*

transmit shift register empty ($\overline{\text{XSREMPTY}}$) bit: A 1-bit flag that indicates if the serial port transmitter has experienced underflow. This bit is stored in the serial port control register (SPC).

transmit shift register (synchronous serial port) (XSR): This register shifts data serially out of the synchronous serial port through the serial data transmit (DX) pin. See also *receive shift register (RSR)*.

transmitter reset ($\overline{\text{XRST}}$) bit: A 1-bit flag that resets the serial port transmitter. At reset, $\overline{\text{XRST}}$ = 0. This bit is stored in the serial port control register (SPC) and time-division multiplexed (TDM) serial port control register (TSPC).

transparency: A pixel attribute that renders a source pixel invisible so that portions of the destination array show through portions of the source array.

transparency on source operation: A transfer by the transfer controller (TC) in which the source data is compared to a transparency value on a byte-by-byte basis; these comparisons are grouped according to the transparency data size. If the compared bytes within a group match, the TC disables the corresponding byte strobes to prevent writes to any of the bytes within that group.

trap: An exceptional condition caused by the currently executing instruction that forces a program to be interrupted before execution of the next instruction begins. After the processor has serviced the trap, it typically resumes execution of the interrupted program at the instruction that immediately follows the instruction that caused the trap.

trap vector table (TVT): An ordered list of addresses which each correspond to an interrupt; when a trap is executed, the processor executes a branch to the address stored in the corresponding location in the trap vector table. (*TMS320C4x)*

trap vector table pointer (TVTP): A register in the CPU expansion-register file that contains the address of the beginning of the trap vector table. (*TMS320C4x*)

TRB: See *timer reload (TRB) bit.*

TRCV: See *TDM data receive register*.

TREG: See *temporary register*.

TREG0: See *temporary register 0*.

TREG1: See *temporary register 1*.

TREG2: See *temporary register 2*.

trickle refresh cycles: Low-priority refresh cycles. These refresh cycles occur only when the bus is idle.

trigraph sequence: A three-character sequence that has a meaning as defined by the ISO 646-1983 Invariant Code Set. These characters cannot be represented in the C character set and are expanded to one character. For example, the trigraph ??' is expanded to ^. (*TMS320C6200*)

trip count: The number of times that a loop executes before it terminates.

triple: A row in a table consisting of three columns. For example, an RGB triple contains the red, green, and blue values which define a particular color.

tri-state: High impedance.

TRM: See *enable multiple TREGs (TRM) bit*.

TRNT: See *TDM receive interrupt (TRNT) bit*.

TRSR: See *TDM data receive shift register*.

TRTA: See *TDM receive/transmit address register*.

TSPC: See *TDM serial port control register*.

TSS: See *timer stop status (TSS) bit*.

TSS bit: See *timer stop status (TSS) bit.*

TTL: *Transistor-to-transistor logic*.

TVTP: See *trap vector table pointer*.

TX pin: See *asynchronous transmit pin*.

TXM: See *transmit mode (TXM) bit*.

TXNT: See *TDM transmit interrupt (TXNT) bit*.

TXRXINT: See *transmit/receive interrupt (TXRXINT)*.

U

UART: See *universal asynchronous receiver and transmitter.*

unconfigured memory: Memory that is not defined as part of the memory map and cannot be loaded with code or data.

unified mode: A mode of operation for the direct memory access (DMA) coprocessor. The mode is used mainly for memory-to-memory transfers. This is the default mode of operation for a DMA channel. See also *split mode*.

uninitialized section: A common object file format (COFF) section that reserves space in the memory map but that has no actual contents. These sections are built with the .bss and .usect directives.

union: A variable that can hold objects of different types and sizes.

UNION: An option of the SECTIONS directive that causes the linker to allocate the same address to multiple sections.

universal asynchronous receiver and transmitter (UART): Another name for the asynchronous serial port. (*TMS320C2xx*)

unsigned value: A value that is treated as a positive number, regardless of its actual sign.

urgent refresh cycles: High-priority refresh cycles that occur when the backlog of refresh requests exceeds 16. A burst of four refresh cycles is performed, with remaining refresh requests waiting for the completion of higher priority cycles.

URST: See *reset asynchronous serial port (URST) bit*.

user mode: A mode in which the master processor (MP) cannot write into control register numbers lower than 0x4000 and cannot write into the MP's parameter RAM.

V

variable: A symbol representing a quantity that can assume any of a set of values.

variable-patch guided transfer: A type of guided transfer in which all patch size information is specified within the guide table rather than in the packet transfer parameters, allowing each patch within the transfer to have different dimensions. See also *delta-guided transfer*, *offset-guided transfer*, *guided transfer*.

$\overline{\text{VBLNK}}$: See *vertical blanking*.

VC: See *video controller*.

vector: See *interrupt vector*.

vector dot product: A mathematical term applied to the sum of the products of individual elements from two different vectors a and b.

vector instruction: An operation that allows you to perform a floating-point operation in parallel with a load or store instruction.

vector location: See *interrupt vector location*.

vendor unique (VU): A bit-, field-, or coded-value that can be uniquely defined for each vendor or device.

vertical blanking ($\overline{\text{VBLNK}}$): Bidirectional vertical timing signals that occur once per frame (once per field for interlaced systems) and have a pulse width defined as an integral number of lines (halflines for an interlaced system). *$\overline{\text{VBLNK}}$* is used to disable pixel capture and display during vertical retrace. See also *blanking.*

vertical synchronization ($\overline{\text{VSYNC}}$): .A bidirectional vertical timing signal occurring once per frame with a pulse width defined as an integral number of of lines (halflines for interlaced mode).

VGA: See v*ideo graphics array.*

VGA pass-through cable: A cable provided by TI as part of the TMS320C8x software development board (SDB) kit or package. The cable connects the output of a standard video graphics array (VGA) graphics board to the VGA pass-through connector of the SDB. (*TMS320C8x*)

video controller: The portion of the multimedia video processor (MVP) responsible for the video interface.

video digitizer: A device that converts an analog video signal to a digital representation.

video graphics array (VGA): An industry standard for video cards.

video interface palette (VIP): Used to convert digital RGB (red-green-blue) information to analog signals that drive a display.

video random access memory (VRAM): A portion of the microprocessor's memory address space reserved for the temporary storage of video data before it is sent to the display monitor. A type of dynamic read access memory that lets the video circuitry serially access the memory bit by bit. VRAM has separate pins for the processor and video circuitry. It is used in high-speed video applications and is easily interfaced to a video display.

VIP: See *video interface palette*.

virtual memory: The ability of a program to use more memory than a computer actually has available as RAM. This is accomplished by using a swap file on disk to augment RAM. When RAM is not sufficient, part of the program is swapped out to a disk file until it is needed again. The combination of the swap file and available RAM is the virtual memory.

VRAM: See *video random access memory*.

$\overline{\text{VSYNC}}$: See v*ertical synchronization*.

VU: See *vendor unique*.

W

wait and signal: See *semaphore*.

waiting: A state in which a task has voluntarily blocked itself from further execution until an awaited event occurs. The kernel allows a task to wait either for the arrival of a message at a port or for the arrival of a signal at a semaphore.

WAITING state: See *task state*.

wait queue: A queue of tasks waiting at a port for messages or waiting at a semaphore for signals.

wait state: A period of time that the CPU must wait for external program, data, or I/O memory to respond when reading from or writing to that external memory. The CPU waits one extra cycle for every wait state.

wait-state control register (CWSR): A memory-mapped register that controls the mapping of the program/data wait-state register (PDWSR), the input/output port wait-state register (IOWSR), and the number of wait states. At reset, CWSR = 01111_2.

wait-state generator: An on-chip peripheral that generates a limited number of wait states for a given off-chip memory space (program, data, or I/O). Wait states are set in the wait-state generator control register (WSGR). (*TMS320C2xx, TMS320C24x*)

wait-state generator-control register (WSGR): A register that is mapped to I/O memory to control the wait-state generator. (*TMS320C2xx, TMS320C24x*)

warm boot: The method by which the processor transfers control to the entry address of a previously-loaded program.

WATCH window: A window that displays the values of selected expressions, symbols, addresses, and registers.

$\overline{\text{WE}}$: See *write enable ($\overline{WE}$) pin*.

well-defined expression: An expression that contains only symbols or assembly-time constants that are defined before they appear in the expression.

window: A defined rectangular area of virtual space on the display.

word: A character or bit string considered as an entity.

write enable ($\overline{\text{WE}}$) pin: The DSP asserts $\overline{\text{WE}}$ to request a write to external program, data, or I/O space.

WSGR: See *wait-state generator control register.*

WWW: *World Wide Web*.

X

XA0–XA13: External address pins for data/program memory or I/O devices. These pins are on the expansion bus of the ’C30. See also *A0–An*. (*TMS320C30*)

xba: The assembler keyword for a parallel processor-relative base address in local RAM (either data or parameter RAM). After memory allocation is performed by the linker, xba is changed to either dba (data RAM) or pba (parameter RAM), depending on where space is allocated by the linker.

XD0–XD31: External data bus pins that transfer data between the processor and external data/program memory or I/O devices of the ’C30. See also *D0–D31*. (*TMS320C30*)

XDS: *Extended development system*.

XF bit: See *external flag (XF) pin status bit*.

XF pin: See *external flag (XF) pin*.

XH: See *transmit buffer half transmitted (XH) bit*.

XINT: See *transmit interrupt (synchronous serial port)*.

XPT: See *externally initiated packet transfer*.

XRDY: See *transmit ready (XRDY) bit*.

XRST: See *transmit reset bit*.

XSR: See *transmit shift register (synchronous serial port).*

$\overline{\text{XSREMPTY}}$: See *transmit shift register empty ($\overline{\text{XSREMPTY}}$) bit*.

Y

YUV: A color space standard in which the luminance (Y) and chrominance (U and V) values are separate components.

Z

zero fill: A method of filling the low- or high-order bits with zeros when loading a 16-bit number into a 32-bit field. (*TMS320C62xx*)

ZIF socket: Zero insertion force socket.