Application Report
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How to Begin Development With the TMS320C6712 DSP

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ABSTRACT

This application report describes how you can begin development now for the Texas Instruments TMS320C6712 digital signal processor (DSP) systems. The similarities and differences between the C6712 and the C6711 devices are briefly discussed. Because of the compatibility between TMS320C6000™ generation devices, existing C6000™ software tools and development platforms can be used to develop code for the C6712 and other future devices. This capability allows for systems to be up and running when silicon becomes available.

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1 How to Begin Development Today With the TMS320C6712 DSP

The Texas Instruments TMS320C6000 generation of high-performance digital signal processors (DSPs) now includes the TMS320C6712. The C6712 is the lowest-cost entry in the C6000 family of floating-point DSPs. The C6712 device is sampling now, providing 600 MFLOPS (million floating-point operations per second) at 100MHz.

Introduced in February 1997, the C6000 generation is based on TI's VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Figure 1 shows the low-cost roadmap for C6000 platform.

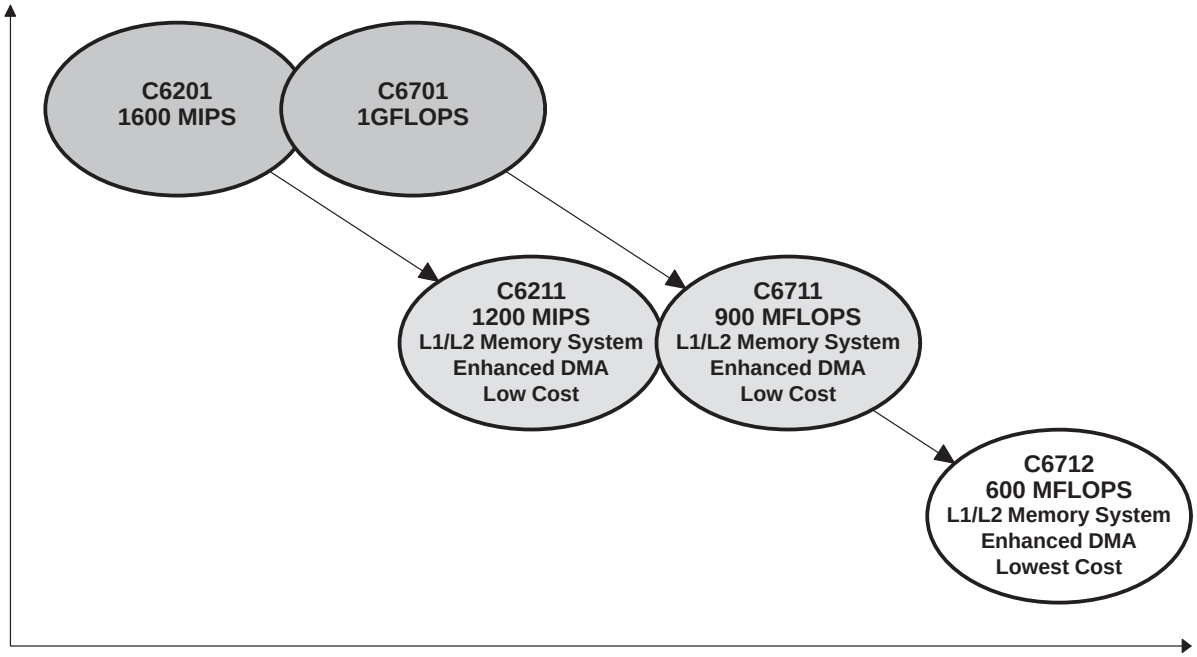


Figure 1. TMS320C6000 Low-Cost DSP Roadmap

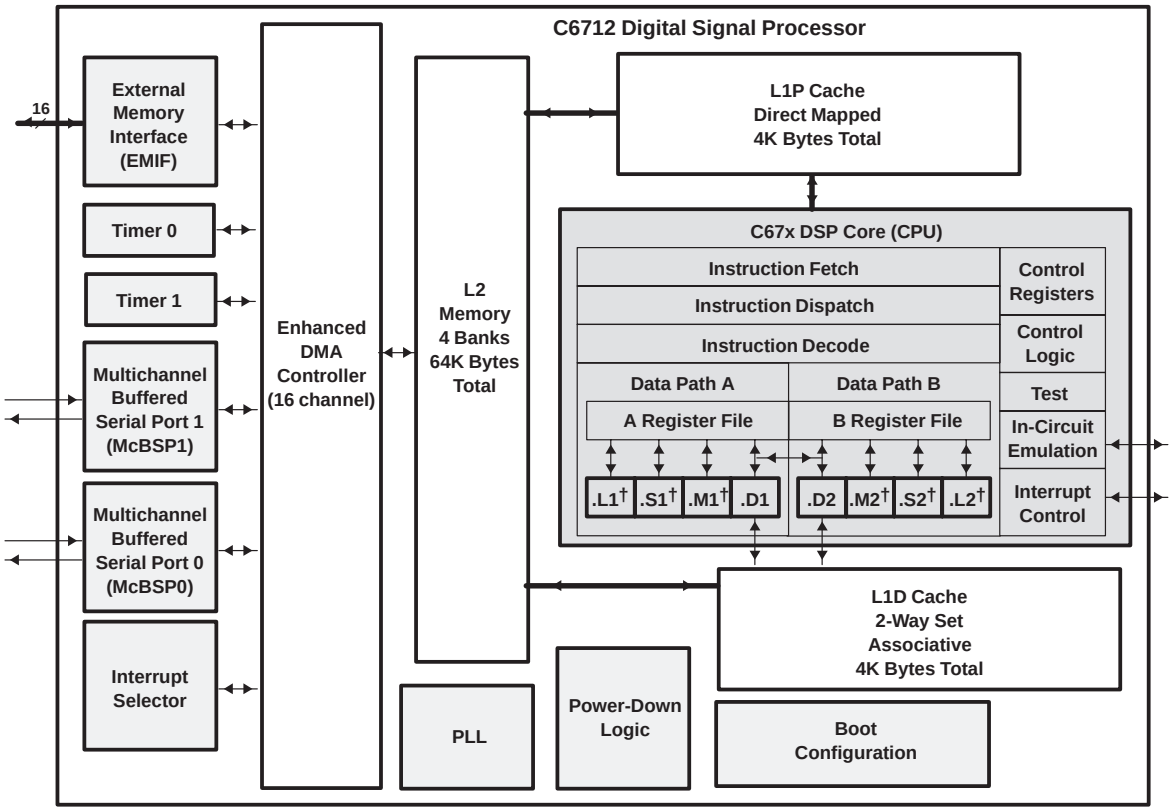
2 TMS320C6000 Compatibility

All C6000 generation devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (C67x) members. All of the C67x devices are based on the same DSP core (CPU) designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to six floating-point instructions during a single clock cycle—up to 600 MFLOPS at 100MHz.

VelociTI's advanced features include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

This common architecture allows designers to begin development with existing C6000 software tools for those devices currently in development. This also allows for migration from one C6000 processor to another, as design specifications require.

In addition to the DSP core, many of the on-chip peripherals are common between C6000 devices. Figure 2 shows a block diagram of the C6712. Those blocks in dark gray are shared between the C6701, C6711, and C6712. Those blocks in white are shared between the C6211, C6711, and C6712. Those blocks in light gray are shared between all C6000 devices.



† In addition to fixed-point instructions, these functional units execute floating-point instructions.

Figure 2. TMS320C6712 DSP Block Diagram

2.1 Similarities Between the C6712 and C6711 DSPs

The C6712 is pin-to-pin compatible with the C6711 device. The C6712 is essentially a subset of the C6711 device with the following device components identical between the two devices:

- C67x floating-point DSP core
- Internal memory structure including L1 and L2 cache architectures
- Enhanced DMA (EDMA) Controller
- Multi-channel Buffered Serial Ports (McBSPs)
- 32-bit timers
- Interrupt selector
- Power down logic
- PLL (x1, x4)

2.2 Differences Between the C6712 and C6711 DSPs

Several modifications have been made to allow the C6712 to be available at a lower cost than the C6711. These include:

- Clock rate: The C6712 runs at 100MHz, while the C6711 runs at 100 and 150 MHz.
- Host Port Interface (HPI): The C6712 does not have a Host Port Interface (HPI). An external device can communicate with the C6712 via the McBSP, EMIF, or timer general-purpose input/output interface.

- External Memory Interface (EMIF): The C6712 has a 16-bit EMIF data bus, while the C6711 has a 32-bit EMIF. The C6712 can interface to 8- and 16-bit wide SDRAM, SBSRAM, and asynchronous memory. These narrower interfaces allow development of lower cost systems with a single 8- or 16-bit wide memory.

- Boot configuration: The C6712 device does not support HPI boot mode or 32-bit ROM boot. The C6712 device has dedicated device configuration pins: BOOTMODE and LENDIAN, to specify boot-load operation and device endianness, respectively, during device reset. These device configuration pins are integrated with HPI pins on the C6711. The pins, however, are located at the same positions on the C6711 and C6712 to allow pin-compatibility between the two devices. Boot mode configuration, with the exception of HPI boot mode and 32-bit ROM boot, is the same between the two devices.

3 Best Price/Performance

The cache architecture of the C6712 allows for this device to be offered at a low cost, while keeping the high performance floating-point capabilities of the C6000 generation. By having an efficient on-chip cache, system designers may use slower, cheaper external memory devices for data and program storage without significantly impeding the performance of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market. The C6712 was designed with TI's low-power high-density TSC6000 ASIC Standard Cell library for low cost, while still providing 100MHz performance.

The enhanced direct memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the C6712 memory map, the EDMA controller transfers data in the background of DSP core operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA controller offers 16 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA controller channel is synchronized by an event to allow minimal intervention by the DSP core.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. Like the C6211 and C6711, the C6712 has 72 Kbytes of on-chip memory, with 8 Kbytes serving as a level-one (L1) cache that the DSP core can directly access. The L1 cache is divided into 4 Kbytes of program (L1P) and 4 Kbytes of data (L1D) cache memory. The remaining 64 Kbytes of on-chip memory is a unified program and data memory space. It can serve as a level-two (L2) cache, be directly mapped as internal memory, or serve as a combination of these functions.

L1P is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a 256-bit wide data path to the DSP core, so that the DSP core may fetch eight instructions (one fetch packet) every cycle.

L1D is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both DSP core data ports, so that the DSP core can load or store two 32-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations on a cache miss.

The L2 memory is divided into four 8-Kbyte banks, each of which can be programmed as a cache or RAM space. Each bank selected as cache adds one way of associativity, allowing the L2 cache to be 1-, 2-, 3-, or 4-way associative. Banks of L2 that are selected as cache are not included in the C6711 memory map. The mapability of L2 blocks as addressable locations allows critical code and data to be locked into internal memory.

TI has run extensive tests on this L1/L2 architecture to determine how it performs with an enhanced full-rate GSM vocoder, system-level applications in ADSL, V.90 modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent. In other words, only one instruction or data word in fifty needs to be fetched from L2 or external memory.

The high L1 hit rate, combined with the flexibility of L2 memory organization, means that this architecture can operate at more than 80 percent of the cycle performance of a more expensive device with an traditional memory organization where all system memory is on the chip. This high degree of efficiency allows systems such as DSL client modems to rely on inexpensive external memory for program and data storage, while at the same time performing high-speed number-crunching routines in real time.

4 Begin Writing Code for the C6712 Today

The identical DSP cores in the C6701, C6711, and C6712 devices allow for code to be written for the C6712 using existing C6000 tools. C6701/C6711 code or fixed-point C6211 code that does not utilize the HPI will require almost no modification to use on the C6712. The EMIF CE Space Control Register value in C6701/C6211/C6711 code need to be adjusted in order to support the 16-bit EMIF on the C6712. The 32-bit memory type is no longer available on the C6712, thus EMIF CE Space Control Register can no longer use the MTYPE values of 0010b, 0011b, and 0100b. See the *TMS320C6000 Peripherals Reference Guide* (SPRU190) for more details. All other peripheral-specific code will run unchanged on the C6712.

The identical architectures of the C6211, C6711, and C6712 devices allow for many system-level issues to be resolved prior to obtaining C6712 silicon. EDMA controller programming may be tested on the C6211 or C6711. Floating-point specific code may be verified on the C6701 or C6711.

This high level of compatibility between the processors allows for system development to begin now. By taking advantage of the C6000 software and hardware tools currently available, C6712 systems can have a running start for when silicon becomes available.

The C6000 compiler may be used for all members of the C6000 device platform. Floating-point devices are object code compatible, so code written for the C6701/C6711 may be used by the C6712.

The C6000 simulator may be used to provide a cycle-accurate account of device performance and to provide a good environment to learn the C6000 VLIW architecture. The C6711 configuration of the simulator may be used to model the C6712 device. The peripherals on the C6711 are identical to those modeled with the C6701 configuration. The C6711 configuration also models the cache performance of the device. Using this configuration, it is possible to optimize code structure and data organization to take advantage of the C6711 cache structure. L1 cache misses to L2 and L2 cache misses are supported with 100% cycle accuracy. C6712 designs may be worked out in detail on the simulator prior to purchasing actual silicon, with cycle-accurate accounts of EDMA, EMIF, and cache performance.

For a development start in hardware, the C6711 DSK may be used to understand the C6000 functionality. In this environment, floating-point code can be debugged while running in real time. All of the peripherals on the C6712 are identical to those of the C6711, with the exception of the HPI and EMIF, so the DSK is a good tool to understand how to incorporate the peripherals into a real-time system. Applications running on the C6711 DSK will be 100% cycle accurate to a C6712 system. The 100 MHz version of the C6711 will provide the exact same performance as the C6712.

Using these development platforms, as well as the C6000 literature currently available will enable C6712 systems to be completed soon after C6712 silicon is made available.

4.1 C6000 Tools Support

C6000 tools are available now for use in all C6000 designs. The C6000 development tools available today for the C6712 are:

- C6000 Simulator Software
- C6000 Optimizing C Compiler/Assembler
- TMS320C6201 Multi-channel Evaluation Module (McEVM)
- TMS320C6701 Evaluation Module (EVM)
- TMS320C6211 DSP Starter Kit (DSK)
- TMS320C6711 DSP Starter Kit (DSK) available in November 2000
- XDS510 C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable

4.2 C6000 Literature Available

A great deal of literature is available today for the C6000 devices.

- *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189)
- *Manual Update Sheet for TMS320C6000 CPU and Instruction Set Reference Guide* (SPRZ168)
- *TMS320C6000 Peripherals Reference Guide* (SPRU190)
- *TMS320C6000 Technical Brief* (SPRU197)
- *Code Composer Studio User's Guide* (SPRU328)
- *TMS320C6000 Code Composer Studio Tutorial* (SPRU301)
- *TMS320C6000 Programmer's Guid*e (SPRU198)
- *TMS320C6000 Evaluation Module User's Guide* (SPRU269)
- *TMS320C6000 Chip Support Library API Reference Guide* (SPRU401)
- *TMS320C6000 Peripheral Support Library Programmer's Reference* (SPRU273)
- *TMS320C6000 Assembly Language Tools User's Guide* (SPRU186)
- *TMS320C6000 Optimizing C Compiler User's Guide* (SPRU187)
- *TMS320C6000 C Source Debugger User's Guide* (SPRU188)
- *TMS320C6000 C Source Debugger For SPARCstations* (SPRU224)
- *TMS320C6000 DSP/BIOS User's Guide* (SPRU303)
- *TMS320C6000 DSP/BIOS Application Programming Interface (API) Reference Guide* (SPRU403)
- *DSP Algorithm Integration Standard (XDAIS) Rules and Guidelines* (SPRU352)
- *DSP Glossary* (SPRU258)
- *TMS320 DSP Standard Algorithm Developer's Guide* (SPRU424)

Many application notes also exist for assistance with C6711 applications.

- *Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation-C6000* (SPRA440)
- *Guidelines For Software Development Efficiency On the TMS320C6000 VelociTI Architecture* (SPRA434)
- *Implementation Of G.726 ADPCM On TMS320C62XX DSP* (SPRA066)
- *Implementing V.32BIS VITERBI Decoding on the TMS320C62XX DSP* (SPRA444)
- *Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201* (SPRA421)
- *TMS320C6201 Power Supply*
- *TMS320C6201 System Clock Circuit Example* (SPRA430)
- *TMS320C6000 EMIF to External SDRAM/SGRAM Interface* (SPRA433)
- *TMS320C6000 BGA Manufacturing Considerations* (SPRA429)
- *TMS320C6000 Board Design: Considerations for Debu*g (SPRA523)
- *Reset Circuit for the TMS320C6000 DSP* (SPRA431)
- *TMS320C6X Thermal Design Considerations* (SPRA432)
- *Using the TMS320C6X McBSP as a High Speed Communication Port* (SPRA455)

NOTE: See http://www.ti.com/sc/docs/dsps/products/c6000/index.htm for more information.

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