Topic 8 - JTAG Boundary Scan

JTAG
(IEEE 1149.1/P1149.4)
Tutorial
Introductory

Agenda

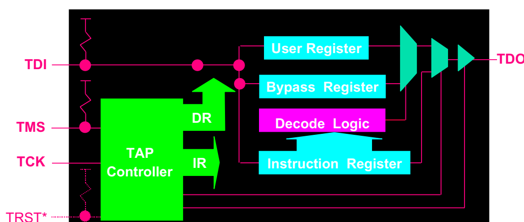
- What Is JTAG? (5 minutes)
- The Increasing Problem of Test (5 minutes)
- Conventional Methods of Test (10 minutes)
- The Boundary-Scan Idea (15 minutes)
- The Boundary-Scan Architecture (15 minutes)
- Typical Applications (15 minutes)
  - Interconnect Testing
  - Logic Cluster Testing
  - Memory Testing
  - System-Level Test
- Real JTAG Applications (10 minutes)
- For More Information (5 minutes)
- Q & A (10 minutes)

What Is JTAG?

Standard Approach To Test

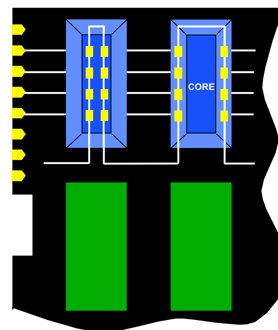
- Developed by Joint Test Action Group (over 200 SC, test, and system vendors) starting in mid '80's
- Sanctioned by IEEE as Std 1149.1 Test Access Port and Boundary-Scan Architecture in 1990
- Solution: Build test facilities/test points into chips
- Focus: Ensure compatibility between all compliant ICs

Standard Test Access Port ...



- 4/5-Wire Interface at Chip-Level
- Serial Instruction/Serial Data Port
- Extensible to Include
  - user-defined instructions
  - user-defined data registers

... and Boundary-Scan Architecture

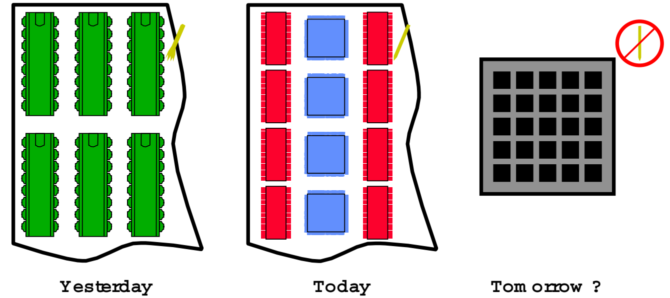


- Scan effectively partitions digital logic to facilitate control and observation of its function
- Chip-Internal Scan: Partitions chips at storage cells (latches/ flip-flops) to effectively partition sequential logic into clusters of combinational logic
- Boundary-Scan: Partitions boards at chip I/Os for control and observation of board-level nodes

The Increasing Problem of Test

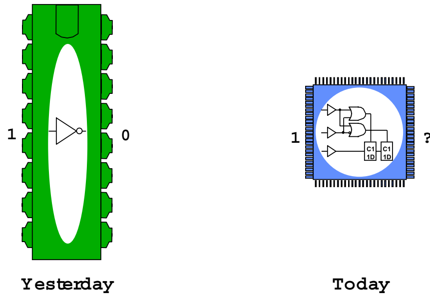
The Incredible Shrinking Board

- Miniaturization results in loss of test access



The Ever-Expanding Chip

- Increasing integration at chip level complicates controllability



Can't Afford Not To Test

Cost will increase by a factor of ten as fault finding moves from one level of complexity to the next. The result:

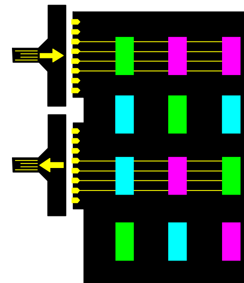
- *Reduced Profit Margins*
- *Delayed Product Introduction*
- *Dissatisfied Customers*

1. Device level	1 unit of cost
2. Board level	10 units of cost
3. System level	100 units of cost
4. Field level	1,000 units of cost

Conventional Methods of Test

Conventional Methods of Board Test

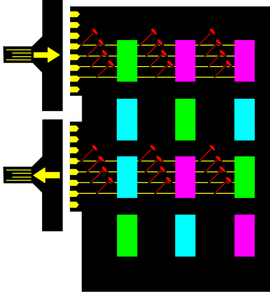
Functional Test (‘Edge-Connector’ Test)



- Based on board function, rather than structure
- Test generation primarily manual
- Test access limited to primary I/O only

Conventional Methods of Board Test

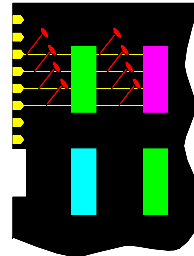
In-Circuit Test ('Bed-of-Nails' Test)



- Based on board structure, but limited by chip complexity
- Expensive testers and fixtures required
- Test access limited by:
  - Fine pitch packages
  - Double-sided boards
  - Conformal coating
  - MCMs

Conventional Methods of Board Test

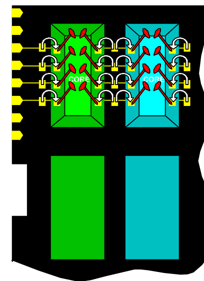
In-Circuit Test ('Bed-of-Nails' Test)



- Chip function can be ignored for shorts testing
- Chip function must be considered for continuity test
- Test generation, though automated, requires ICT models

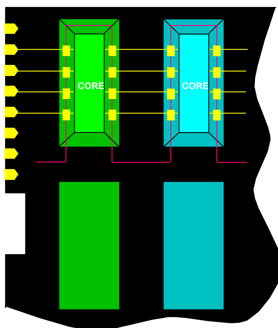
The Boundary-Scan Idea

The __Boundary__ Scan Idea



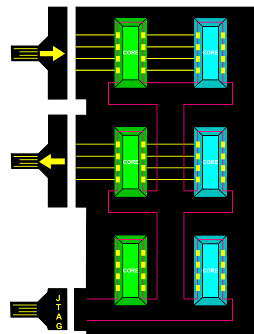
- 'In-Circuit' test points moved onto the silicon, creating 'Virtual Nails'
- Boundary scan cells bound each net, providing for continuity testing
- Observe/Control cells provide for test and normal function

The Boundary __Scan__ Idea



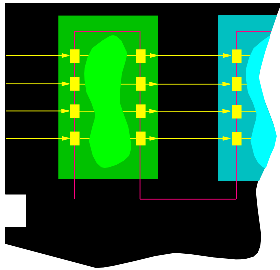
- Scan provides a means to arbitrarily observe test results and source test stimulus
- Scan method requires minimal on chip/board resources (pins/nets)

Boundary Scan Method of Board Test



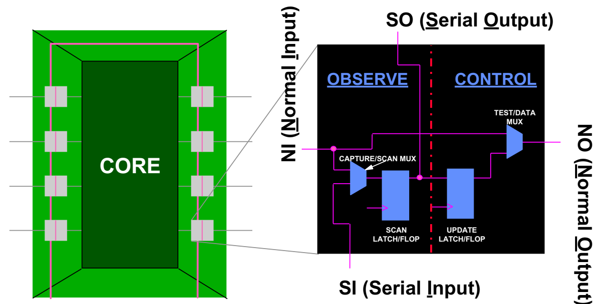
- Based on board structure; Not limited by chip function/ complexity
- Test access is not limited by board physical factors

Boundary Scan Method of Board Test

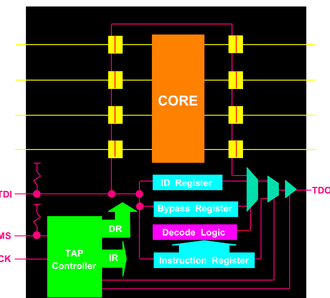


- Chip function need not be considered for board test (shorted/open nets)
- Test generation is highly automated; Simple 'In-Circuit Library' models (BSDL) are vendor-supplied or EDA-generated

The Boundary Scan Cell

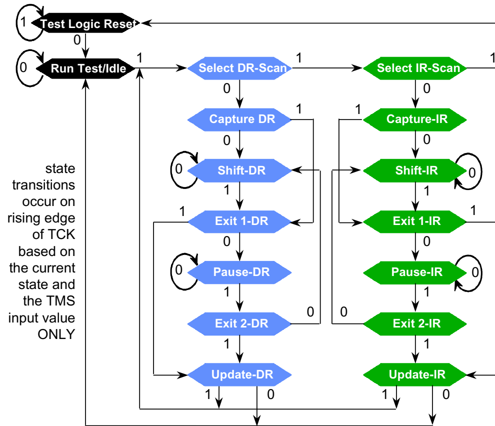


The Control Architecture



- Boundary scan and other test data registers operate under control of instruction register
- Data is scanned from TDI to TDO through selected test data register or instruction register under control of Test Access Port (TAP) controller
- TAP operates synchronously to TCK using TMS for state selection

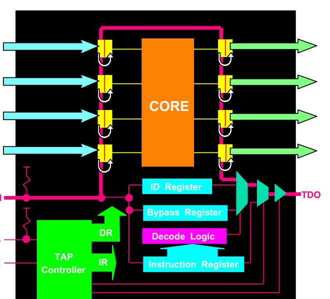
The Test Access Port Controller



- 16-state TAP provides 4 major operations:
  - RESET
  - RUN-TEST
  - SCAN-DR
  - SCAN-IR
- Scans consist of 3 primary steps:
  - CAPTURE
  - SHIFT
  - UPDATE

The Extest Instruction

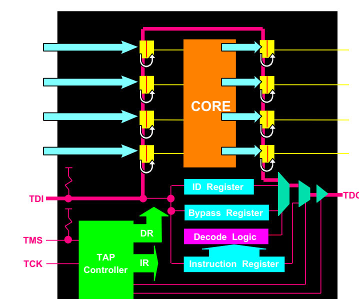
(REQUIRED)



- Provides for test external to chip, such as interconnect test
- Output pins operate in test mode, driven from contents of BSC update latch
- Input data captured in BSC scan latches prior to shift operation
- Shift operation allows test response to be observed at TDO while next test stimulus inserted at TDI
- Following shift operation, new test stimulus transferred to BSC update latches

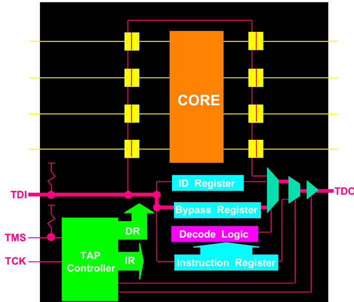
The Sample/Preload Instruction

(REQUIRED)



- Provides means to preload boundary before entry to test mode
- Output and input pins operate in normal mode
- Input pin data and core logic output data captured in BSC scan latches
- Shift operation allows test response to be observed while next test stimulus inserted at TDI
- Following shift operation, new stimulus transferred to BSC update latches

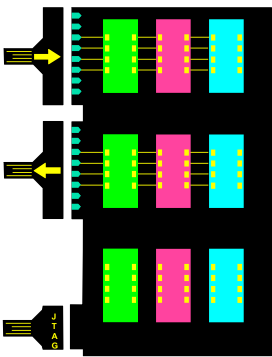
The Bypass Instruction
(REQUIRED)



- Provides for abbreviated scan path through chip
- Output and input pins operate in normal mode
- The one-bit bypass register is selected for scans
- Mandatory that an all-ones value updated into the IR decodes to Bypass, as well as any opcodes which are otherwise undefined

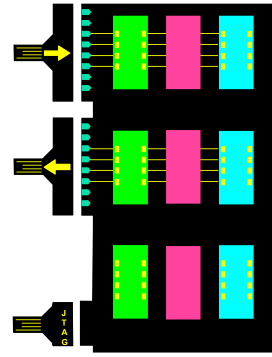
Typical JTAG Applications

Interconnect Test
Full B/S Board



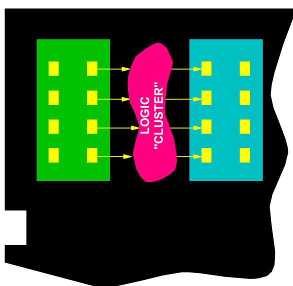
- All nets bound by BSC's and/or primary I/O requiring no physical access
- Parallel access reduced to card edge only
- Test generation and application fast and easy

Interconnect Test
Partial B/S Board



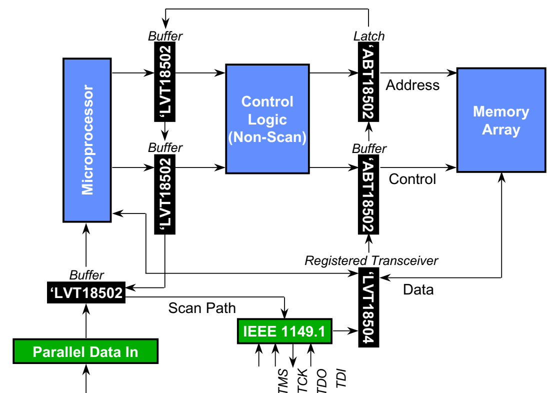
- Not all nets are bound by boundary scan and/or primary I/O, perhaps requiring some ICT access
- Expense and complexity reduced for test generation and test application for chips/nets with B/S access
- Cluster testing may be used to access non-scan nets

Logic Cluster Test

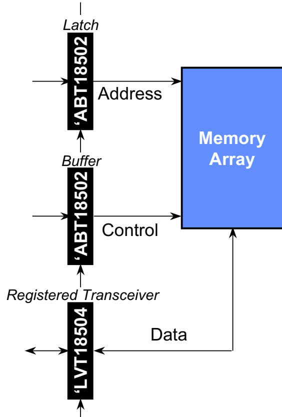


- Random-logic cluster is bound by boundary-scannable chips
- Deterministic test stimulus (ATPG-generated) can be driven to cluster from B/S outputs
- Test response can be captured at B/S inputs
- BIST methods (PRPG/PSA) can be used for increased test throughput and near "At-speed" performance

Logic Cluster Test

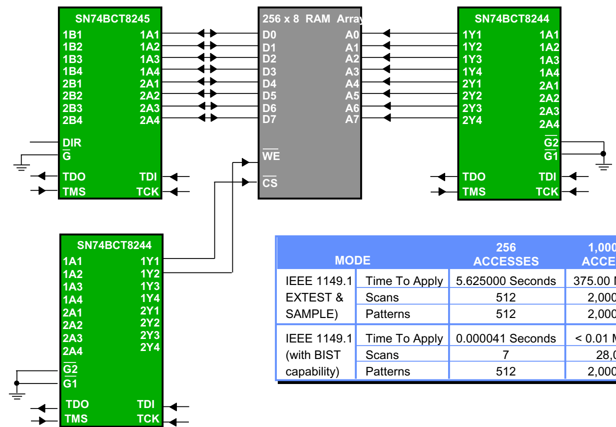


Memory Test



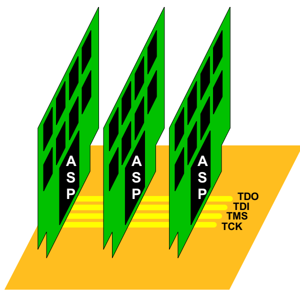
- Memory array bound by boundary scan chips
- Automatic test patterns can be generated and driven from B/S outputs
- Test response can be captured at B/S inputs
- Transceivers can test for net shorts w/o memory R/W
- BIST methods (PRPG/PSA) can be used for increased test throughput

Memory Test



MODE		256 ACCESSES	1,000,000 ACCESSES
IEEE 1149.1	Time To Apply	5.625000 Seconds	375.00 Minutes
EXTEST &	Scans	512	2,000,000
SAMPLE)	Patterns	512	2,000,000
IEEE 1149.1	Time To Apply	0.000041 Seconds	< 0.01 Minutes
(with BIST	Scans	7	28,000
capability)	Patterns	512	2,000,000

System-Level Test

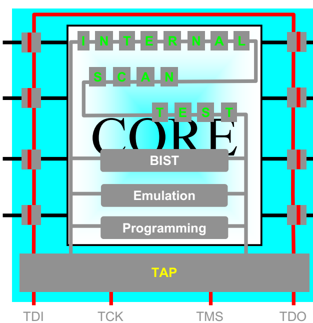


- TAP-addressable interface unit extends JTAG access beyond board-level
- System-level test
- System design verification
- Sys integration (Mfg test)
- Sys self-test (Field Svc)
- Supports in place board test and board-to-board test
- Allows reuse of device/ board test data

✦ ASP-Addressable Scan Port Device

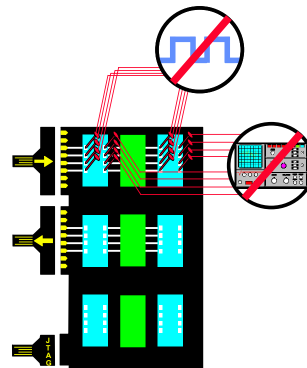
Real JTAG Applications

Real Applications of the TAP



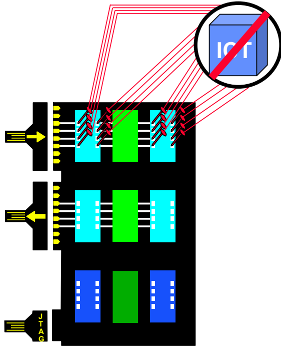
- Scan access to chips, boards, systems for:
  - Design verification/debug
  - Manufacturing test
  - Hardware/software integration
  - Field test/diagnostics
- Access built-in self-test (BIST)
- Access on-chip/in-circuit emulation (ONCE/ICE)
- Access in-system programming (ISP) of PLDs/EEPROMs
- Let your imagination run wild!!!

Design Verification/Debug



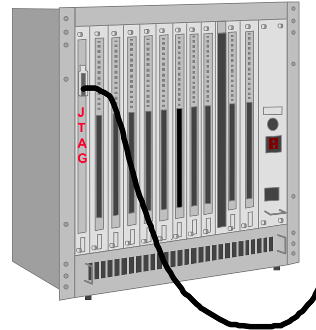
- Provides control and observation of system under test without need for physical access
  - Ease of set-up for test
  - Can be used in standard system configuration (no need for card extenders, etc.)
  - Can be used in environmental chambers
  - Can access on-chip emulation for software/debug
  - Can access ISP for code download/offload/ changes

Manufacturing Test



- Provides test and diagnostic capabilities of in-circuit test without need/expense of physical access
  - Improved fault coverage/diagnostic without large capital expense
  - Highly automated test generation reduces test development time

System Configuration Maintenance

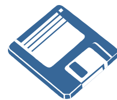


- Provides low-level test access within configured systems for:
  - In-house system integration
  - Fielded-system test and diagnostics
  - Built-in self-test
  - In-field upgradability via ISP, etc.
  - Remote field test, diagnostic and upgrade

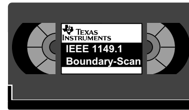
TI's JTAG Educational Products

Call (214)-638-0333 to ORDER

- Scan Educator
  - PC-based tutorial with interactive boundary-scan simulation.
  - FREE download at http://www.ti.com/sc/data/jtag/scanedu.exe



- IEEE 1149.1 Testability videotapes
  - Two-part video presenting an overview and instructions for boundary scan.
  - Item No. SATV001 (NTSC VHS) and SATV002 (PAL VHS), $149 each.
  - In process of converting to MPEG on CD-ROM



IEEE Standards

Call (800) 678-IEEE to ORDER

- IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993), IEEE Standard Test Access Port and Boundary-Scan Architecture, ISBN 1-55937-350-4, IEEE order number SH16626.
  - *The official document which specifies the international standard for a test access port and boundary-scan architecture. Informally known as the JTAG standard, it was officially ratified by the IEEE in February 1990. Since, it has been supplemented twice. The first supplement, ratified in June 1993, is included in the referenced document. The second supplement is currently a separate document, as referenced below.*
- IEEE Std 1149.1b-1994, Supplement to IEEE Std 1149.1-1990, ISBN 1-55937-497-7, IEEE order number SH94256.
  - *The official document which specifies the international standard for a boundary-scan description language. This supplement to IEEE Std 1149.1-1990 was ratified in September 1994.*

Tutorials/Handbooks

- The Test Access Port and Boundary-Scan Architecture, Colin M. Maunder, Rodham E. Tulloss, ed., IEEE CS Press, ISBN 0-8186-9070-4.
  - *Edited by two principal chairs of the IEEE 1149.1 working group, this Computer Society tutorial compiles several of the seminal papers on boundary-scan along with several invited papers on various topics including applications, implementation, and others. It will primarily be of interest to the design and/or test engineer.*
- The Boundary-Scan Handbook, Kenneth P. Parker, Kluwer Academic Publishers, ISBN 0-7923-9270-1.
  - *Authored by the principal force behind the Boundary-Scan Description Language (BSDL) and an IEEE 1149.1 working group principal as well as a long time manufacturing and design-for-test expert, this is truly considered THE indispensable handbook on boundary scan for the design and/or test engineer.*
- Boundary-Scan Test - A Practical Approach, Harry Bleeker, Peter van den Eijnden, Frans de Jong, Kluwer Academic Publishers, ISBN 0-792-9296-5.
  - *Authored by several JTAG and IEEE 1149.1 working group principals, this book is a ready reference to boundary-scan technology, its benefits, and considerations for design and test managers and engineers.*

Abbreviations/Acronyms

ASIC	Application-Specific Integrated Circuit	IEEE	Institute of Electrical & Electronics Engineers IR Instruction Register
ASP	Addressable Scan Port	ISP	In-System Programming
ATE	Automatic Test Equipment	JTAG	Joint Test Action Group
ATPG	Automatic Test Pattern Generation	MCM	Multi-Chip Module
BIST	Built-In Self-Test	Mfg	Manufacturing
B/S	Boundary-Scan	PCB	Printed Circuit Board
BSC	Boundary-Scan Cell	PLD	Programmable Logic Device
BSDL	Boundary-Scan Description Language	PRPG	Pseudo-Random Pattern Generation
BSR	Boundary-Scan Register	PSA	Parallel Signature Analysis
BST	Boundary-Scan Test	PWB	Printed Wiring Board
CAE	Computer-Aided Engineering	SPL	Scan Path Linker
DFT	Design-for-Test	SVF	Serial Vector Format
DR	Data Register	TAP	Test Access Port
DSP	Digital Signal Processing/Processor	TBC	Test Bus Controller
EDA	Electronic Design Automation	TCK	Test Clock
eTBC	Embedded Test Bus Controller	TDI	Test Data Input
FPGA	Field-Programmable Gate Array	TDO	Test Data Output
HSDL	Hierarchical Scan Description Language	TMS	Test Mode Select
ICE	In-Circuit Emulation	TRST	Test Reset
ICT	In-Circuit Test	UUT	Unit Under Test