IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2004

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

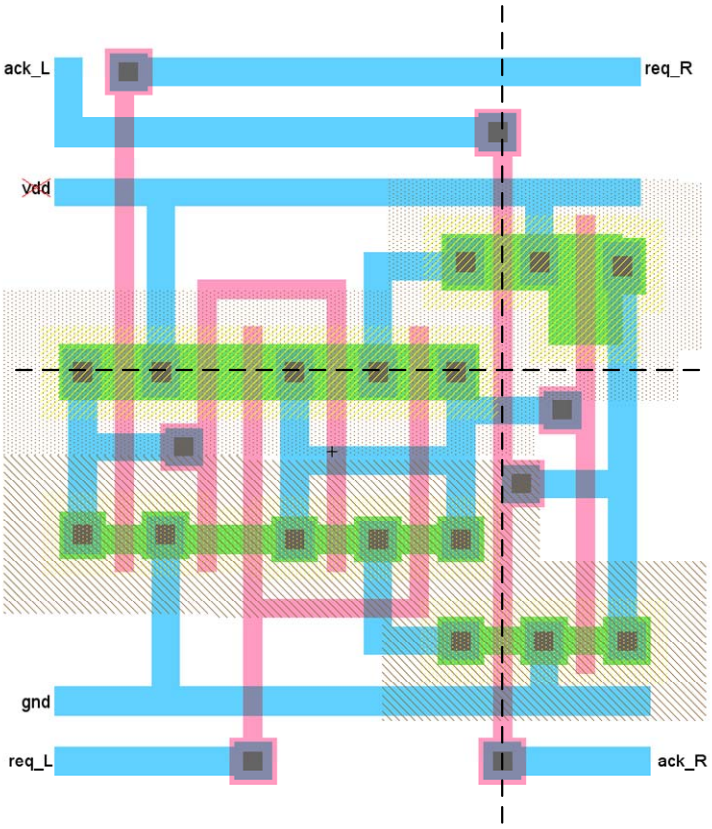
This is an open-book examination.

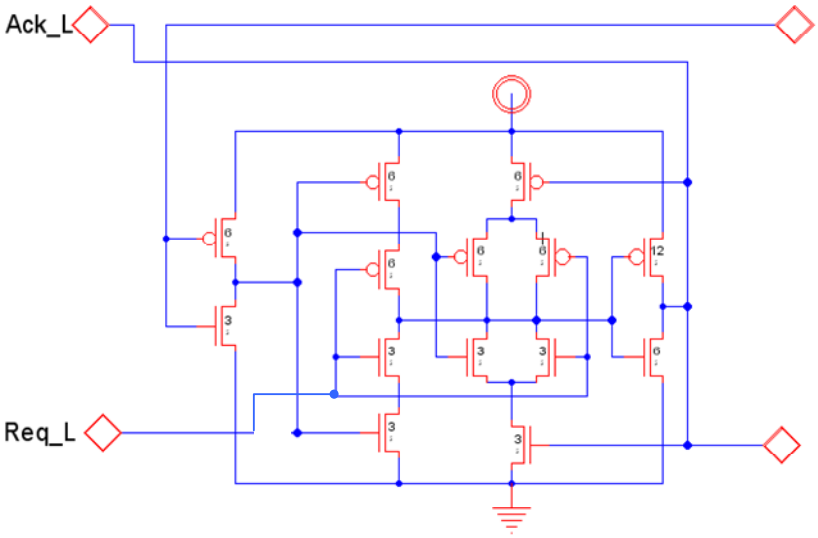
You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Thomas Clarke*

Solution to Question 1

a) This question tests student's ability to understand a full custom layout. This is a special cell for asynchronous systems, known as the Muller-C element with an extra inverter. Students do not need to know the circuit in order to answer this question.



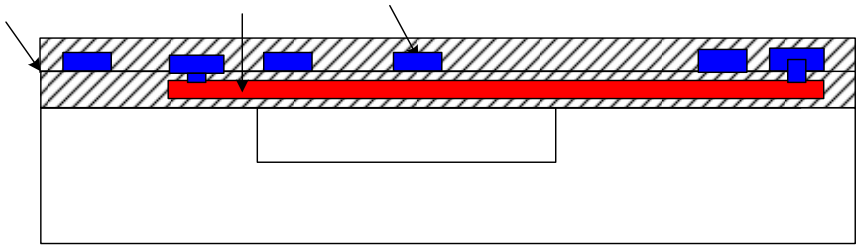


T3 T5 T7

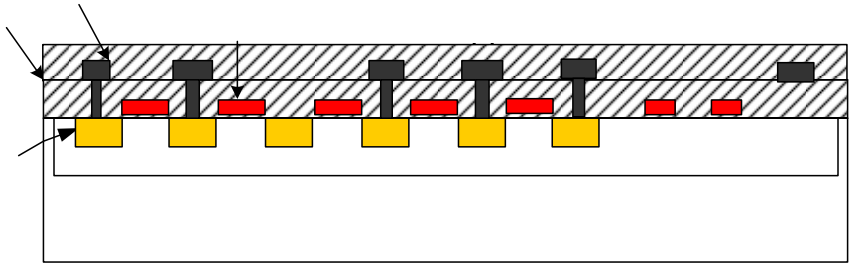
T2 T4 T6 T8

[12 marks]

b) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.

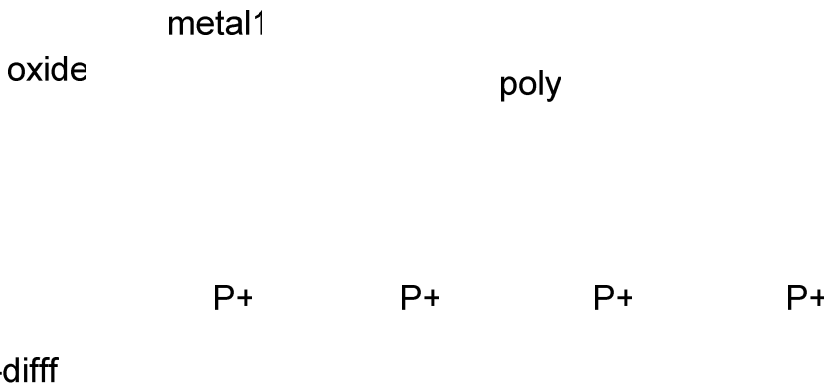


[4]



[4]

[8 marks]



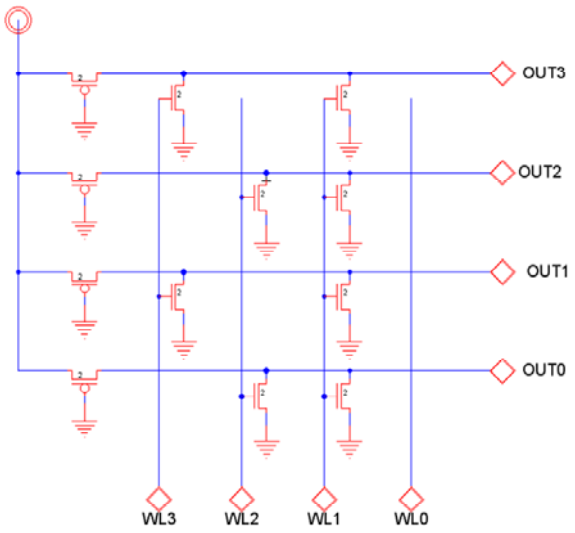
Solution to Question 2 (corrected)

a)

Address	ROM Content
0	0000
1	1111
2	0101
3	1010

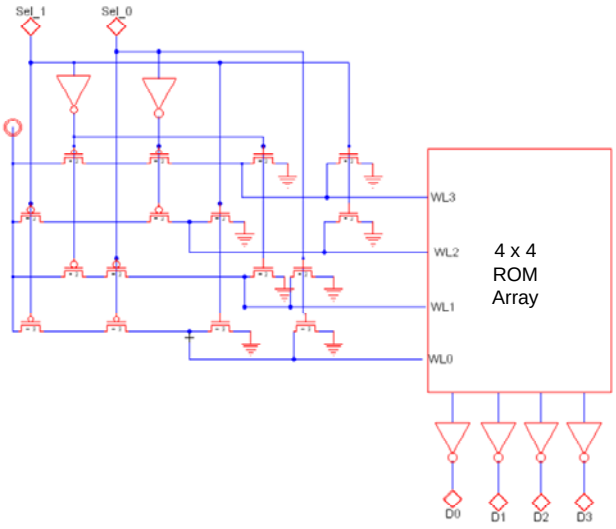
[6 marks]

b)



[8 marks]

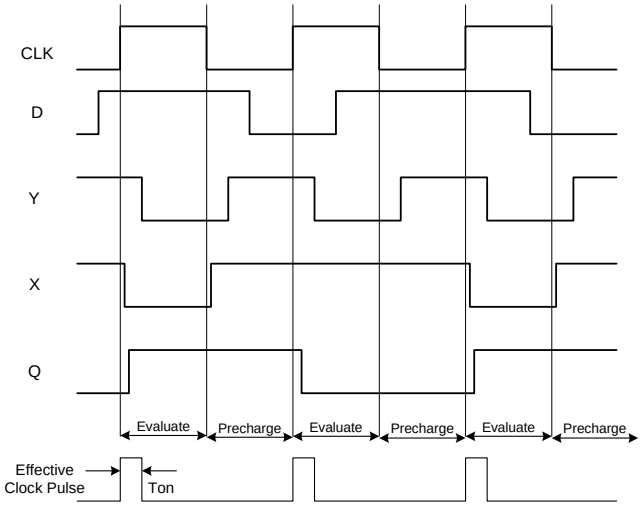
c)



[6 marks]

Solution to Question 3

(a) When clock CLK is low, the flip-flop is in the precharge phase. Node X is precharged to the level of the power supply, and node Q holds its previous value. On the rising edge of the clock, the flip-flop enters the *evaluation phase*. Here two periods are distinguished. In the first period when CLK is high, but Y is also high, it corresponds to an active clock pulse to the circuit and the circuit is in the *sampling* (or transparent) mode. The value of output Q is determined by the value of input D. Once the internal node X is discharged, due to its precharge nature, it will stay low until the next clock cycle. In the second period, the pulse is inactive. The sampling of D is disabled, so X and Q will retain the values they acquired during the sampling period. Notice that any subsequent change at D after the sampling period will have no effect on Q.



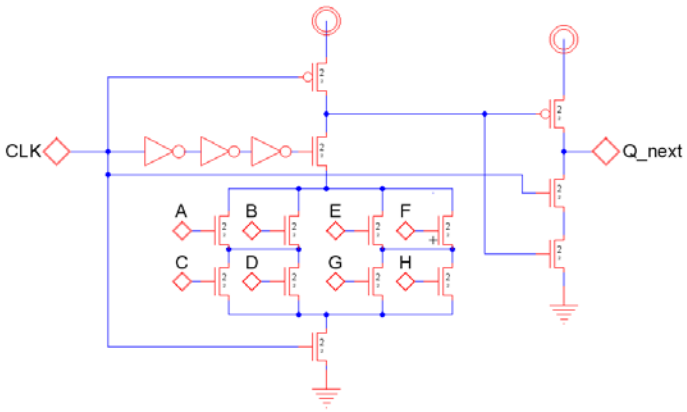
[10 marks]

(b) The shortcoming of this circuit are (any two of the three here will do):

1. Internal node X is a dynamic node and therefore this circuit will not work at low frequency.
2. Output Q is in high impedance when the clock signal CLK is low.
3. The timing of the sampling window Ton is critical: too short a Ton could lead to metastablility or functional failure because the sampling window is too short to correctly evaluate the input. Too long a Ton may cause poor performance by imposing a long hold time.

[4 marks]

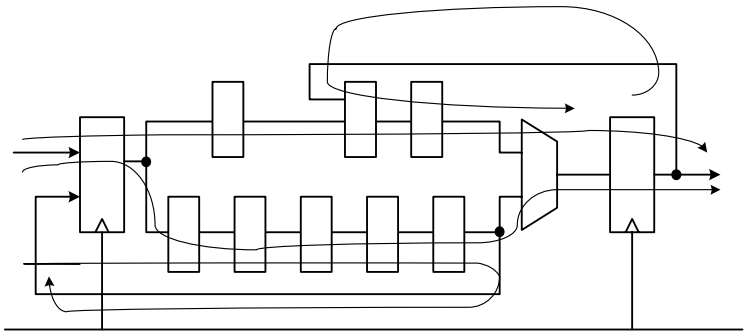
(c)



[6 marks]

Solution to Question 4

a)



(i) Out of the 4 paths shown in the figure, p1 is the critical one and determines the lower bound on the clock period. Using $T \geq t_{reg} + t_{logic} + t_{setup} - \delta$, we get ***Tmin* = 1+7+1 = 9**.

[4 marks]

(ii) As the clock skew increases, the most significant path changes. Repeating the calculations in part (i) we get : Tmin(p1) = 9 - 4 = 5, Tmin(p2) = 6, Tmin(p3) = 7, Tmin(p4) = 7 - 4 = 3. (Note that the clock skew is 0 for paths p2 and p3). Therefore the minimum clock period is Tmin = 7.

[4 marks]

b) (i) Gate width of minimum size inverter is 0.75 μm. t_d = 30ns. Therefore, the Electrical Effort (and total effort F) for the two paths are:

F_{P1} = 900 /0.75 = 1200; F_{P2} = 100 / 0.75 = 133;

Delay estimates of the two paths are: $D_{P1} = 1200 * t_d = 36$ ns; $D_{P2} = 133 * t_d = 4$ ns
P1-P2 skew = 1067 * t_d = 32 ns.

[5 marks]

(ii)

Total effort F for P1 = 1200, P2 = 133. Best number of stages (from notes) is given by:
Nbest = log (F)/ log (3.59). $N_{P1} \approx 5.5$, $N_{P2} \approx 3.8$. P1 should be buffered by 6 inverter stages, P2 also by 4 stages. Therefore

For P1, each stage should increase in size by $\sqrt[6]{1200} = 3.26$,
for P2, each stage should increase in size by $\sqrt[4]{133} = 3.4$.

Solution – increase sizes of p-trans and n-trans by these factors for each of the stages:

Stage	1	2	3	4	5	6
P1:	x 1	x 3	x 10	x 35	x 113	x 368
P2:	x 1	x 3	x 12	x 39		

P1 delay ≈ (3/1 + 10/3 + 35/10 + 113/35 + 368/113 + 1200/368) * t_d = 22.5 t_d
P2 delay ≈ (3/1 + 12/3 + 39/12 + 133/39) * t_d = 13.7 t_d
Clock skew ≈ 8.8* t_d

[7 marks]

Solution to Question 5 (corrected)

a)

$\mathbf{a_j}$	$\mathbf{b_j}$	$\mathbf{c_{j+1}}$	$\mathbf{d_{j+1}}$
0	0	c_j	d_j
0	1	c_j	c_j
1	0	d_j	d_j
1	1	c_j	d_j

[5 marks]

b) Design of the layout depends on student. Marks will be deducted if the layout is inefficient or contains excessive unnecessary crossovers.

[7 marks]

c)

$c_j = (\mathbf{a_j > b_j})$, and $d_j = (\mathbf{a_j = b_j})$

C0 = '0', D0 = '1' indicating that we assume A=B to start.
C4 = (A>B), D4 = (A=B) + (A>B).

Therefore:

Case	C4	D4
A>B	1	1
A=B	0	1
A<B	0	0

[4 marks]

d) (i)

j	0	1	2	3	4
A	1	0	1	1	-
B	0	0	1	1	
C	0	1	1	1	1
D	1	1	1	1	1

(ii)

j	0	1	2	3	4
A	0	1	1	1	-
B	1	0	1	1	
C	0	0	0	0	0
D	1	0	0	0	0

(iii)

j	0	1	2	3	4
A	1	0	0	1	-
B	1	0	0	1	
C	0	0	0	0	0
D	1	1	1	1	1

[4 marks]

Solution to Question 6

a)

Y = NOT (A*B + C*D)

[4 marks]

b) λ = 0.25μ Then all lengths are 1 λ. In order to ensure worst case rise and fall time to be roughly the same, all n-trans use 4 λ width, and all p-trans 8 λ width.

[4 marks]

c) Use Boolean difference method:

Y (B=0) = Y (A,0,C,D) = NOT (C*D)
Y (B=1) = Y (A,1,C,D) = NOT (A + C*D)

Therefore Boolean difference is:

dY/dB = Y(B=0) XOR Y(B=1)
= NOT (C*D) XOR NOT(A + C*D)
= A* NOT(C) + A*NOT(D)

To test for stuck-at-0 fault at B,
test input = B*(dY/dB),
= A*B*NOT(C) + A*B*NOT(D) = 1

Therefore the test vector for B stuck-at-0 = 110x and 11x0, i.e. (1100, 1101, 1110)

To test for stuck-at-1 fault at B,
test input = NOT(B)*(dY/dB),
= A*NOT(B)*NOT(C) + A* NOT(B)*NOT(D) = 1

Therefore the test vector for B stuck-at-1 = 100x and 10x0, i.e. (1000, 1001, 1010)

[5 marks]

d) If B = NOT(C), then we can use the cell as a MUX between A and D inputs.

[7 marks]