Department of Electrical & Electronic Engineeing
Imperial College London

E4.20 Digital IC Design

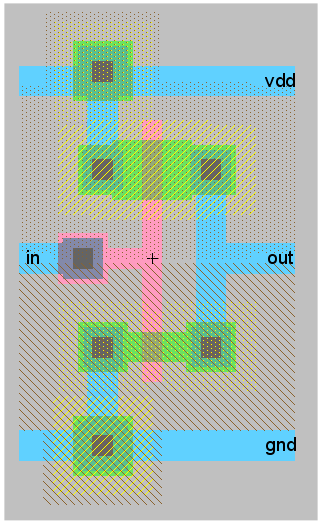
Laboratory 2: Using Electric for Layout

Objectives

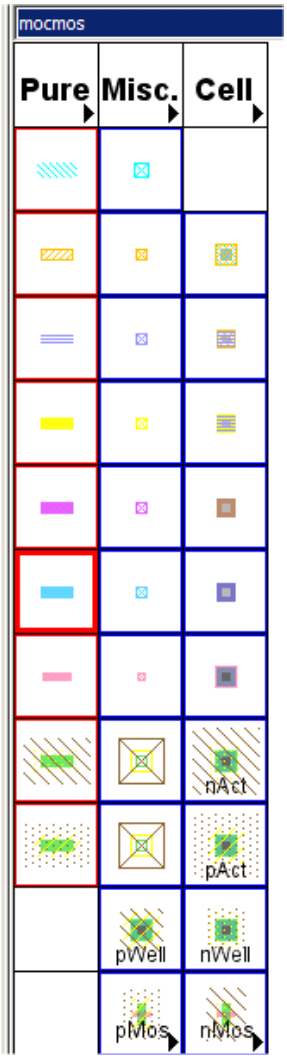
By the end of this laboratory session, you should be able to:

- *Design the layout of an inverter;*
- *Connect multiple stages of the inverter to form an 11-stage ring oscillator;*
- *Simulate this ring oscillator using WinSpice;*
- *Compare the results with those obtained using only schematic.*

Exercise 1: Layout of an inverter



- The goal of this exercise is to create the layout of an inverter as shown on the right. A version of this inverter is made available to you as **lab2.elib** (zipped file) which you may download from the course web page. Open this cell layout for reference on your screen.

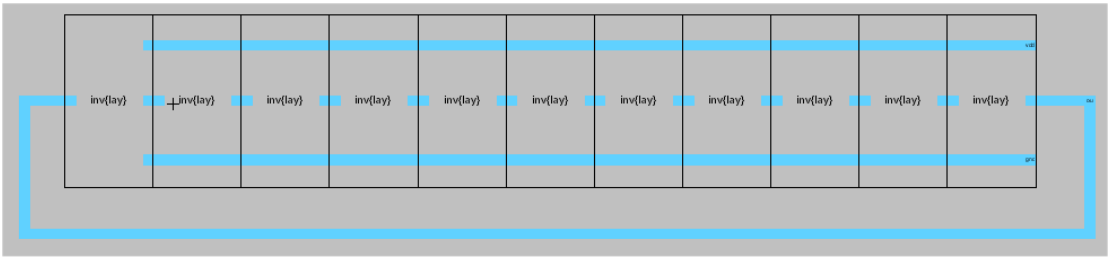


- Create a new layout cell "**myinv**" in a new window. (Do this by ticking the "**make a new window**" button in the new cell popup form.) Size and locate the sample cell and the new cell windows side-by-side.
- Shown below is the menu palette with short descriptions for each entry. Pick and place a n-channel and a p-channel transistor (do not use the "scalable" transistors) in the drawing area. Rotate them with the rotate command (**Ctrl-J**) so that the red polysilicon gates are aligned vertically.
- Double click on the n-transistor and change its size to 3λ x 2λ. Similarly change the p-transistor to 6λ x 2λ.
- Left-click on the p-transistor near to the lower side of the poly gate. The p-channel transistor will be selected and a small cross will appear on the lower poly terminal.
- Right-click on the upper poly terminal of the n-transistor. This will wire the gates of the two transistors together.
- With the n-transistor selected, use the cursor keys to move the transistor so that it is vertically aligned with the p-transistor. Then move two transistors closer together until a Design Rule Error (DRC) is report in the message window. You are recommended NOT to use concurrent DRC, but use F5 key to check for DRC error at each step.
- Press the ">" key to show the next DRC error. The objects that violate the DRC will be highlighted, and an explanation of this error is reported in the message window.
- Check the reported error (Rule 1.4) against the DRC document on the course web page: www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/scmos_rules.html

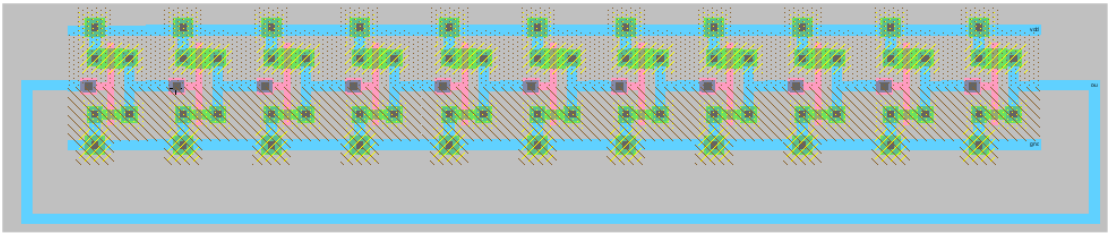
- Move the n-transistor away from the p-transistor until no design rule is violated. Press **F5** to explicitly check for DRC error of the layout so far. It should report 0 error.
- Moving objects together one lambda at a time until DRC error just occurs, then moving them apart by one lambda is a good technique to follow when you are not familiar with design rules.
- Now place a **metal1-ndiffusion contact** on either side of the n-transistors. Connect the contact with the source and drain terminals respectively. Note that n-diffusion is automatically used for the connections. Now move each contact towards the transistor until no DRC error is found. (Note that DRC errors are report when the contact is either too far or too near to the transistor. Why?)
- Similarly place and connect **metal1-pdiffusion contacts** to the drain and source of the p-transistor.
- Place a **metal1-poly contact** to the left of the transistors. Wire the m1-poly contact to the polysilicon gate wire of the transistors. Move the contact as close to the poly wire as possible.
- Place a **metal 1 pin** to the left of the m1-poly contact and export this as a global input terminal "**in**" (**ctrl-E**). Wire it to the m1-poly contact.
- Place a metal 1 pin to the right of the transistors. Wire and export it as a global output terminal "**out**". Wire it to the drain terminals of both transistors.
- Place and wire up a **metal1-nwell contact** and a **metal1-psubstrate contact** as shown on the previous page.
- Place and wire up metal 1 pin to the **vdd** and **gnd** wire, and export them as power and ground terminals.
- Use **F5** key to check for DRC errors throughout the above procedure until you have a layout that is error free and is as compact as possible. You should now have a layout similar to that show on the previous page.

Exercise 2: Create layout of a 11-stage ring oscillator

- Create a new layout cell "**osc11**".
- Select the "**myinv{lay}**" cell from the menu palette and place one in the drawing area.
- Use the **Edit > Array** command (or **F6**) to make an array of 11 inverter cells.
- Wire up the **Vdd** and **Ground** terminals of all the cells. Connect the output of each inverter to the next stage's input terminal. Connect the right-most output back to the left-most stage input in a loop fashion as shown below.



- Place metal 1 pins on the Vdd and Gnd wires, and export them as power and ground global terminals respectively. Place a metal 1 pin on the loop back wire and export it as an output terminal "**ring_out**".
- Select all the cells and use the **Cell > Expand Cell > All the way** command to see the layout of the whole ring oscillator. You should see something like this:



- Save everything.

> Hints: You will find that creating a single inverter without DRC error is relatively straight forward. However, creating an array of inverters to form the ring oscillator can be tricky. The problem lies with the interaction between neighbouring cells (usually the rule on minimum distrance between well areas). One technique to ensure that there are no DRC violation when a cell is duplicated as array is to explore placing two identical cells next to each other and adjust the layout until no DRC is found.

Exercise 3: Simulate the 11-stage ring oscillator

- Write a SPICE desk for the ring oscillator and simulate it with WinSPICE.
- Examine the SPICE netlist with a text editor and compare it with the netlist you obtained in Lab 1. Can you see any differences?
- Check and compare the oscillation frequency of the layout circuit to that from the schematic.

Exercise 4: NAND gate layout & ring oscillator with disable input

- Design the topology of a NAND gate on paper (as symbolic layout or stick diagram).
- Create the layout for the NAND gate. Ensure that has the same pitch as the inverter.
- Create a new 11 stage ring oscillator with a NAND gate followed by 10 inverters.
- Simulate your circuit with WinSPICE and verify that it works properly.

Exercise 5: Routing tools for arrays

- Electric includes various routing tools that reduce the tedium of wiring up structured cells. The most useful one for the ring oscillator is called the Mimic Router. Read the chapter on Mimic Router in Electric's manual on: www.staticfreesoft.com/jmanual/mchap08-05-03.html.
- Create a new cell "osc11_autoroute" and place 11 stances of the inverter (layout view) in the drawing area using the array command. Now issue the command: **Tools > Routing > Enable Mimic-stitching**. This switches on the router routine.
- Wire up the left-most inverter output to the input of the next inverter. You should see that the Mimic Router automatically wire all the remaining inverters input/output terminals for you, mimicking your action. Do the same for the Vdd and Ground terminals. Complete the feedback loop and verify that the final circuit works properly.