Mux-Based Latches

Negative latch (transparent when CLK= 0)

Positive latch (transparent when CLK= 1)

\[ Q = \overline{Clk} \cdot Q + Clk \cdot In \]

\[ Q = Clk \cdot Q + \overline{Clk} \cdot In \]

Mux-Based Latch

NMOS only

Non-overlapping clocks
Master-Slave (Edge-Triggered) Register

Two opposite latches trigger on edge
Also called master-slave latch pair

Master-Slave Register

Multiplexer-based latch pair

Reduced Clock Load
Master-Slave Register

Overpowering the Feedback Loop – Cross-Coupled Pairs

NOR-based set-reset

Forbidden State
Cross-Coupled NAND

Cross-coupled NANDs

Added clock

$V_{DD}$

S

Q

R

Q

M1

M2

M3

M4

M5

M6

M7

M8

CLK

S

R

This is not used in datapaths any more, but is a basic building block for memory cell

Sizing Issues

Output voltage dependence on transistor width

Transient response

Storage Mechanisms

Static

Dynamic (charge-based)

Making a Dynamic Latch Pseudo-Static
Master-Slave Static Flip-flop

- Overlapping Clocks Can Cause
  - Race Conditions
  - Undefined Signals

Two-phase dynamic flip-flop

Use 2-phase non-overlapping clocks

Latch + Logic
Other Latches/Registers: C²MOS

\[
\begin{align*}
D & \quad M_1 \quad M_3 \quad M_5 \\
CLK & \quad M_2 \quad M_4 \quad M_6 \quad M_7 \\
Q & \quad M_8 \\
\end{align*}
\]

“Keepers” can be added to make circuit pseudo-static

Insensitive to Clock-Overlap

\[
\begin{align*}
D & \quad X & \quad Q \\
\end{align*}
\]

Pipelining

<table>
<thead>
<tr>
<th>Clock Period</th>
<th>Adder</th>
<th>Absolute Value</th>
<th>Logarithm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(a_1 + b_1)</td>
<td>(</td>
<td>a_1 + b_1</td>
</tr>
<tr>
<td>2</td>
<td>(a_2 + b_2)</td>
<td>(</td>
<td>a_2 + b_2</td>
</tr>
<tr>
<td>3</td>
<td>(a_3 + b_3)</td>
<td>(</td>
<td>a_3 + b_3</td>
</tr>
<tr>
<td>4</td>
<td>(a_4 + b_4)</td>
<td>(</td>
<td>a_4 + b_4</td>
</tr>
<tr>
<td>5</td>
<td>(a_5 + b_5)</td>
<td>(</td>
<td>a_5 + b_5</td>
</tr>
</tbody>
</table>

Other Latches/Registers: TSPC

Positive latch (transparent when CLK = 1)

Negative latch (transparent when CLK = 0)
Including Logic in TSPC

Example: logic inside the latch

AND latch

TSPC Register

\[ Q \]

\[ D \]

\[ M_1 \]

\[ M_2 \]

\[ M_3 \]

\[ M_4 \]

\[ M_5 \]

\[ M_6 \]

\[ M_7 \]

\[ M_8 \]

\[ M_9 \]

\[ \phi \]

\[ \pi-latch \]

Output stable when \( \phi \) is high

\( \mu-\pi \) latches: Poor man’s TSPC Latch

- What is wrong with this TSPC Latch?

- Second attempt:
Pulse-Triggered Latches
An Alternative Approach

Ways to design an edge-triggered sequential cell:

Master-Slave Latches

Pulse-Triggered Latch

Data
L1
L2
D
Q
Clk
Data
D
Q
Clk

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

Hybrid Latch-FF Timing

Pulsed Latches

(a) register
(b) glitch generation
(c) glitch clock

Pulsed Latches

Hybrid Latch-FF Timing

Ways to design an edge-triggered sequential cell:

Hybrid Latch – Flip-flop (HLFF), AMD K-6 and K-7:

Hybrid Latch-FF Timing
Latch-Based Pipeline

Non-Bistable Sequential Circuits—Schmitt Trigger

- VTC with hysteresis
- Restores signal slopes

Noise Suppression using Schmitt Trigger

CMOS Schmitt Trigger

Moves switching threshold of the first inverter
Schmitt Trigger Simulated VTC

Voltage-transfer characteristics with hysteresis.

The effect of varying the ratio of the PMOS device $M_4$. The width is $k = 0.5 \times W_m$.

CMOS Schmitt Trigger (2)

Multivibrator Circuits

Bistable Multivibrator
flip-flop, Schmitt Trigger

Monostable Multivibrator
one-shot

Astable Multivibrator
oscillator

Transition-Triggered Monostable
Monostable Trigger (RC-based)

(a) Trigger circuit.

(b) Waveforms.

Relaxation Oscillator

\[ T = 2 \left( \log_3 \right) RC \]

Astable Multivibrators (Oscillators)

Ring Oscillator

simulated response of 5-stage oscillator

Voltage Controller Oscillator (VCO)

Current starved inverter

propagation delay as a function of control voltage

Schmitt Trigger restores signal slopes
Differential Delay Element and VCO

delay cell

two stage VCO

simulated waveforms of 2-stage VCO