Lecture 9

Circuit Extraction & irsim

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Reading: Irsim manual

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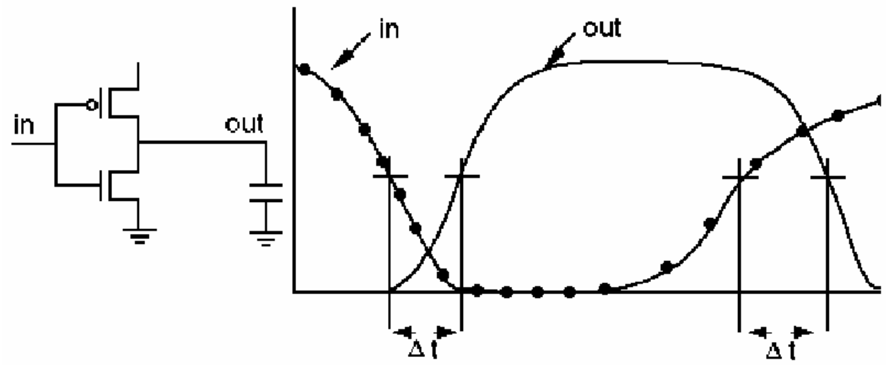
Delay measurement with RC model

- Delay measured from 50% crossing point on input and output swings.
- Define R_{sq} of a transistor so RC gives the right delay values



- Typically nMOS = 13KΩ * L/W, pMOS = 26K. * L/W

Extraction

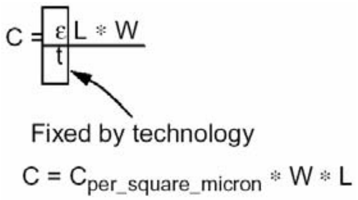
- Need to verify that the layout is correct.
- This is done by circuit extraction, I.e. extract a netlist from the layout information.
- Read the magic tutorial 7 on extraction.
- Produce netlist with interconnecting transistors
- Produce wire resistance and parasitic capacitances
- Extracted netlist can be in two formats:
  - SPICE netlist for SPICE/HSPICE simulation
  - sim netlist for Irsim simulation

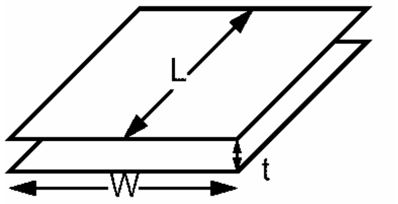
Extracted parameters

- C_{load} comes from three factors:
  1. Gate capacitance of driven transistors.
  2. Diffusion capacitance of source/drain regions connected to the wire.
  3. Wire capacitance
- Resistance/square for transistors and capacitance/micron don't change much with technology scaling.
- For a 0.25μ technology Rsq of a nMOS device is 15K, pMOS is 36K, which is similar to the 1μ numbers. The cap/micron numbers are nearly the same.
- The reason the gates get faster is that the cap/lambda goes down, so the cap of a 10:2 device scales down, while the resistance remains constant.

Parallel plate capacitance

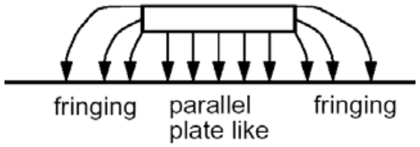
- Two simple models
  - Parallel Plate
  - Cylindrical
- The capacitance of most real objects can be approximated by a combination of these two factors.
- Parallel Plate

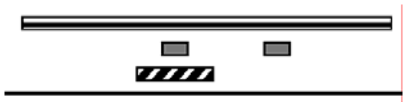




Wire capacitance

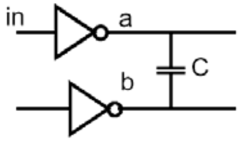
- So, wires have two components to capacitance, one that is proportional to the wire’s area, and the other proportional to the wire’s perimeter. **For minimum width metal wires, the edge component is much larger than the area component**, so forgetting the edge is a large error.
- The area capacitance depends on the thickness of the oxide between the capacitor plates, and that thickness depends on what is below it.

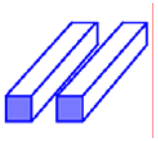




Coupling capacitance

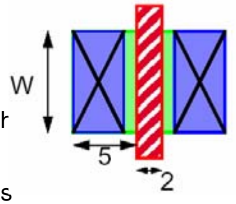
- Capacitance is mostly between two wires, not between a wire and ground
- Coupling capacitance makes analysis more complex:
  - It creates noise issues - ‘a’ changing will cause noise on ‘b’
  - It makes delay calculations harder
  - If ‘a’ and ‘b’ transition at the same time in same direction
    - ΔV across the cap will be zero, and it won’t affect the delay
- If ‘a’ and ‘b’ transition at the same time in opposite direction (Miller effect)
    - ΔV across the cap will be 2V, and it will look like a grounded cap of 2C



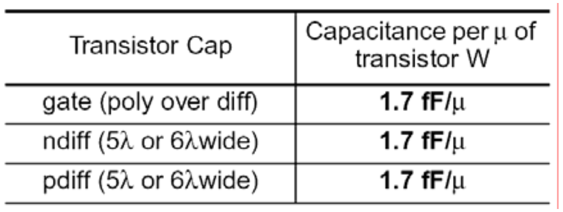


Estimate capacitances

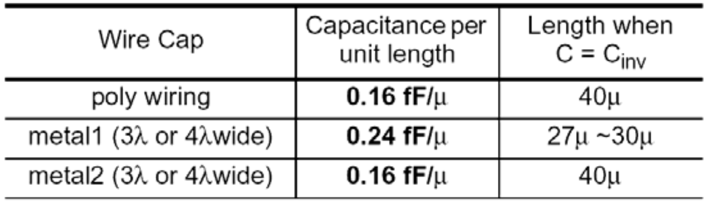
- Want to have numbers that make it easy to estimate the capacitance
  - Want the estimates to depend on the fewest number of parameters
  - Willing to make some approximations
- For wires
  - Most wires are minimum width
  - Large edge component of capacitance anyhow
  - So makes sense to measure capacitance per unit length
- For transistors
  - Gate length is usually minimum (2λ, 0.35μ), width varies
  - Diffusion region kept small, size depends on transistor width
  - Give cap of these region as capacitance per unit transistor width



Rule of thumb estimates

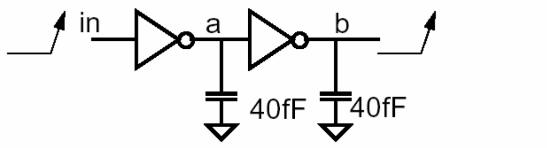


Transistor Cap	Capacitance per μ of transistor W
gate (poly over diff)	**1.7 fF/μ**
ndiff (5λ or 6λwide)	**1.7 fF/μ**
pdiff (5λ or 6λwide)	**1.7 fF/μ**



Wire Cap	Capacitance per unit length	Length when C = C_{inv}
poly wiring	**0.16 fF/μ**	40μ
metal1 (3λ or 4λwide)	**0.24 fF/μ**	27μ ~30μ
metal2 (3λ or 4λwide)	**0.16 fF/μ**	40μ

A simple example

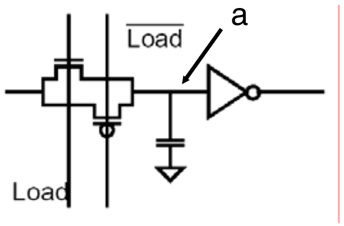


40fF includes the diffusion and gate cap

- Assume that all transistors are 4λ width and 2λ in length
- When the ‘in’ rises, ‘a’ will fall:
  - delay = RC = 13K/2 * 40fF = 0.26ns (nMOS transistor is on)
- When ‘a’ falls ‘b’ will rise:
  - delay = RC = 26K/2 * 40fF = 0.52ns (pMOS transistor is on)
- Total delay from ‘in’ to ‘b’ = 0.26ns + 0.52ns = 0.8ns

Dynamic nodes

- What happens to the value on node ‘a’ when the switch disconnects?



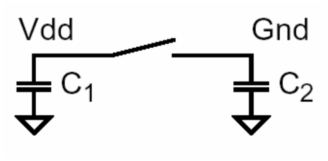
- When the switch is off, the current driving the capacitor is zero
  - i = CdV/dt dV/dt = 0, so the voltage remains unchanged
- The value remains unchanged
  - That is, when you stop driving a node its value remains unchanged, and remains almost the same until it is driven again. This is the good part of capacitance.

Leakage current

- There is no leakage current from the gate of a MOS transistor but the source/drain terminals do have a small leakage current.
- Leakage current is very small, usually picoAmps
  - Charge will leak away, but very slowly
- Storage times are usually about **1 second** at Room Temp
  - Leakage is temp sensitive
  - Doubles every 10°C
  - 10ms at 70 °C
- Leakage is much slower than the clock rate. Dynamic store is ok, if the node is reloaded every few clocks. If you can’t guarantee when you will reload the storage node, you had better use a different storage element.

Charge sharing

- What happens when you connect two capacitors together?



- Charge must be conserved

  C1 Vdd = (C1 + C2) Vfinal

  Vfinal = Vdd * C1/(C1 +C2)
- So either

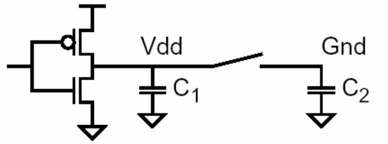
  C1 >> C2; both nodes become 1 >> requires approx 4x ratio

  C2 >> C1; both nodes become 0

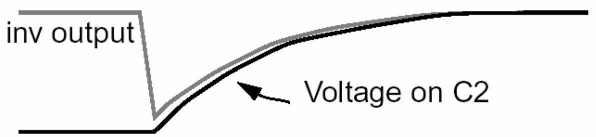
  otherwise you will get an undefined value.

+Charge sharing

- Charge sharing can occur even if you are driving the node
- If the resistance of the switch is small compared to the driving transistor, and C2 is larger than C1, then there is momentarily a resistive divider.



- C2 will first drive C1 to Gnd
- Then (more slowly) the pMOS will drive both capacitors high

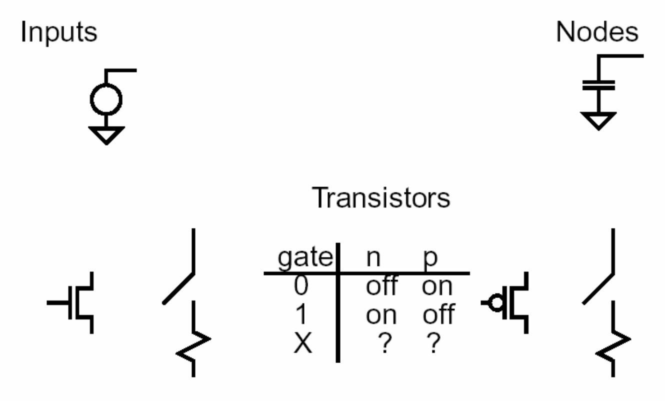


Switch level simulation

- Need some way to check the circuits to see if we built them correctly
  - Nice if the method could handle all legal switch circuits.
  - Want to find common bugs in circuits, yet not produce false errors.
  - Be fast and easy to use.
- Tool should answer the questions:
  - Does these transistors do the logic function that I want?
  - Are there any sneak paths (unexpected paths), floating outputs?
- Switch-level simulation is one good way to answer these questions.
  - Uses the same type of model shown earlier
  - Nodes are modelled as capacitors
  - Values on the nodes are 0,1,X
  - Transistor is modelled as a switch in series with a resistor, where the value of resistor depends on the type of transistor and the quantized signal values. (i.e. nMOS resistance lower for driving to gnd than for pulling up to vdd; pMOS resistance lower for pulling up)

Switch-level simulation models

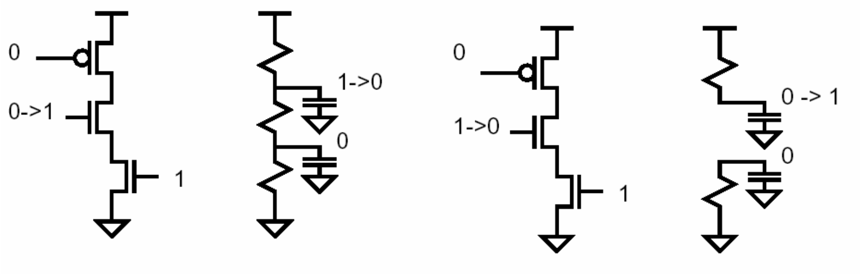
- Build RC network based on these simple models:



gate	n	p
0	off	on
1	on	off
X	?	?

+Switch-level simulation

- To find a value in a switch network
  1. Build a cluster of connected transistors Walk out from a node through all the **on** transistors
  2. Replace all transistors by their equivalent resistance
  3. Replace all nodes by a capacitor, charged to the old value
  4. Solve the RC circuit for final value, delay



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irsim

- **irsim** will calculate:

1. Final voltage for each node in the circuit, correctly handling all ratios. All R,C, and intermediate voltage ranges are floating point computations. Quantizes to 0,1,X state only at the end of each event.

2. Delay (Quantized to 0.1nS for efficiency in scheduling events)

   Uses a better model than the one we have discussed in class.

   But it is conceptually similar

3. Correct charge sharing (even when the node is partially driven)

Of course, because it is an approximation, the program is not perfect.

Sometimes too generous with X values propagation of X values can be too fast

Some legal circuits will not simulate (but most digital circuits will be ok)

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irsim netlist

- The two required input files are a transistor parameter file (called .prm format) and the network connection file (called .sim format). Can also put multiple command files (preceded by '-') on the command line using the same commands as are listed for interactive use.
- The .sim network description file is **flat** (no hierarchy), and has a simple format (documented in the .sim manual page). Each line is one of:

  n gate_node source_node drain_node length[μ] width[μ]

  p gate_node source_node drain_node length[μ] width[μ]

  C node cap_value[fF] (adds cap between node and gnd)

  C node1 node2 cap_value[fF]

- Capacitors need only be added to model the wiring interconnect. The irsim program will automatically add gate loading.

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irsim netlist example

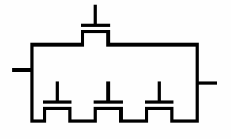
```
Example of irsim file
| units: 40 tech: scmos
p in_b out Vdd 2 8
n in_b out GND 2 4
p out out_b Vdd 2 8
n out out_b GND 2 4
p out_b out1 Vdd 2 8
n out_b out1 GND 2 4
p out1 out1_b Vdd 2 8
n out1 out1_b GND 2 4
c out gnd 50
c out_b gnd 60
c out1 gnd 70
c out1_b gnd 80
```

What irsim finds difficult?

- There are two kinds of problems that irsim has trouble handling:

  1. Transistor loops

     In this structure there are a set of transistors that form a loop, and neither end of the loop is a power supply. In this case the loop will be broken, (to convert it to a tree) and the simulation will continue. Note that multiple paths to supplies are ok, as are single transistor loops (CMOS transmission gates)



- 2. Self-connected transistors

  These structures have the gate of a transistor connected to the same cluster as one of the outputs of the circuit. Since irsim needs to set the inputs to figure out the outputs, the program can have problems with this type of circuit. This circuit rarely comes up, except for the 6T XOR gate.