Topic 2

Basic MOS theory & SPICE simulation

Peter Cheung
Department of Electrical & Electronic Engineering
Imperial College London

(Weste&Harris, Ch 2 & 5.1-5.3
Rabaey, Ch 3)

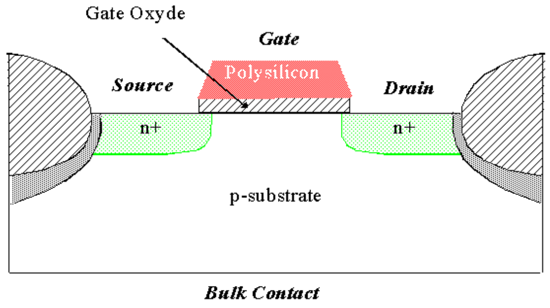
URL: www.ee.ic.ac.uk/pcheung/
E-mail: p.cheung@imperial.ac.uk

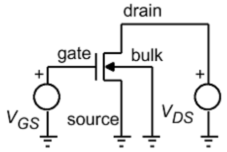
Conduction Characteristics of MOS Transistors (for fixed Vds)

- MOS transistors are majority-carrier devices.
- For n-channel transistors, the majority carriers are electrons conducted through a channel.
- A positive gate voltage (w.r.t. substrate) ***enhances*** the number of carriers in the channel, and increases conduction.
- **Threshold voltage** V_{tn} denotes the gate-to-source voltage above which conduction occurs.
- For **enhancement** mode devices, V_{tn} is positive; for **depletion** mode devices, V_{tn} is negative.
- p-channel devices are similar to n-channel devices, except that all voltages and currents are
- in opposite polarity.

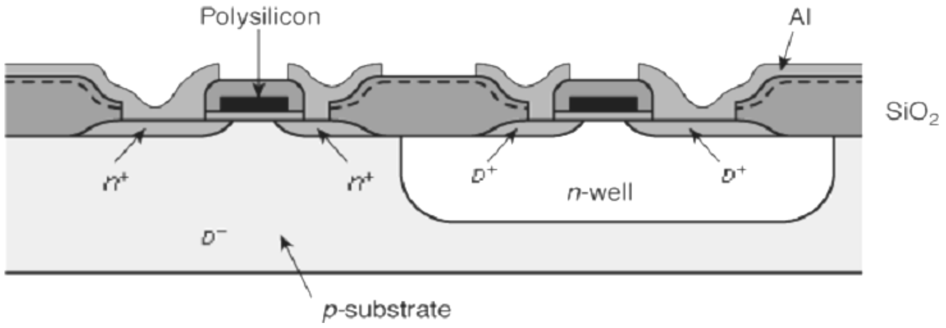
MOS Transistor

- Shown here is the cross-section of an n-channel enhancement transistor:
- Substrate is moderately doped with p-type material. Substrate in digital circuit is usually connected to V_{Gnd} (ground).
- The source and drain regions are heavily doped with n-type material through diffusion. These are often referred to as the **diffusion** regions.

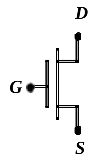




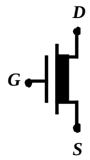
Cross-Section of CMOS Technology



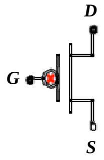
MOS transistors - Types and Symbols



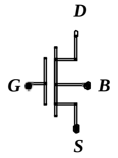
NMOS Enhancement



NMOS Depletion

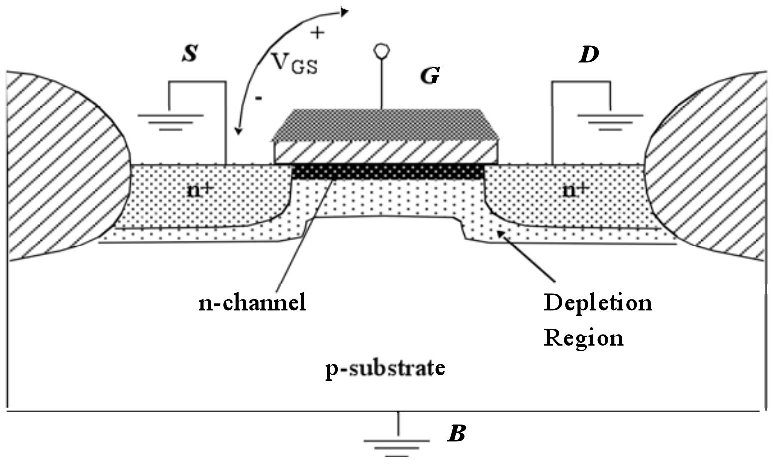


PMOS Enhancement



NMOS with Bulk Contact

Threshold Voltage: Concept



MOS transistor (1)

- Between the diffusion regions is the gate area form from a layer of polycrystaline silicon (known as **polysilicon**). This is separated from the substrate by a layer of **thin oxide** (made of silicon dioxide). Polysilicon is reasonable conductor and form the gate electrode.
- Underneath the thin oxide and between the n+ regions is the **channel**. The channel is conducting when a suitable electric field is applied to the gate.
- Due to geometric symmetry, there are **no distinctions** between the source and drain regions. However, we usually refer the terminal with more positive voltage the drain (for n-type) and less positive voltage the source.
- For a zero gate bias and a positive V_{DS}, no current flows between the drain and source because of the two **reverse biased diodes** shown in the diagram. The drain and source are therefore isolated from each other.
- Assuming that the substrate is always at the most negative supply voltage, these two diode should never become forward bias under normal operation.

MOS transistor (2)

- When a positive voltage is applied to the gate, an electric field is produced across the substrate which attracts electrons toward the gate. Eventually, the area under the gate changes from p-type to n-type, providing a conduction path between the source and drain.
- The gate-source voltage V_{GS} when a channel starts to form under that gate is called the **threshold voltage** V_T.
- The surface underneath the gate under this condition is said to be **inverted**. The surface is known as the **inversion layer.**
- As larger bias is applied to the gate the inversion layer becomes thicker
- An other p-n junction exists between the inversion layer and the substrate. This diode junction is **field induced**. Contrast this with the p-n junction between the source (or drain) and the substrate, which is created by a metallurgical process.

The Threshold Voltage

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

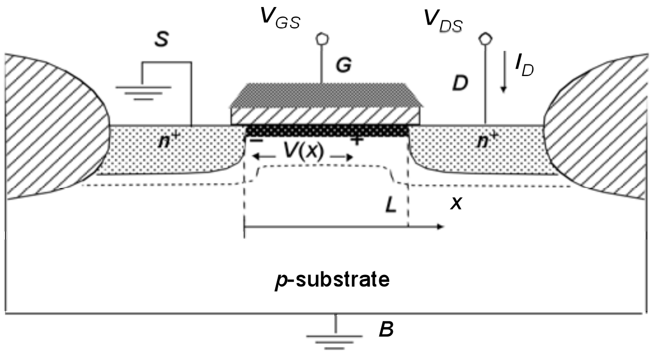
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Current-Voltage Relations



MOS transistor and its bias conditions

Current-Voltage Relations

Linear Region: $V_{DS} \le V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

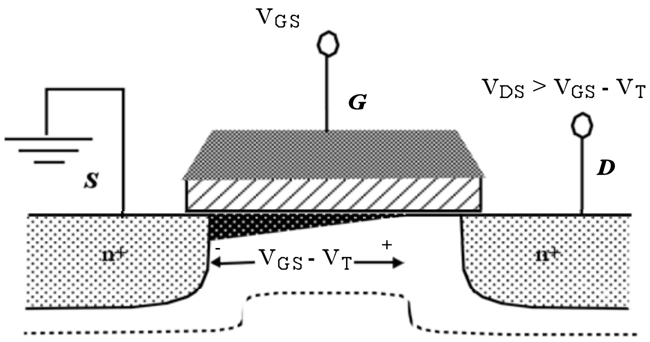
Process Transconductance Parameter

Saturation Mode: $V_{DS} \ge V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

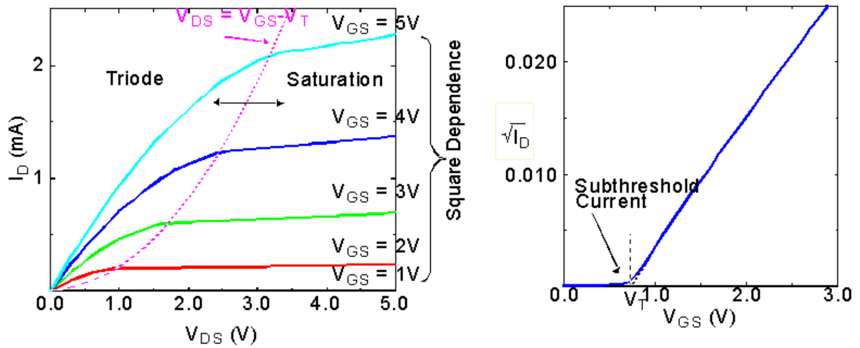
Transistor in Saturation



MOS transistor (3)

- As a voltage is applied between the source and drain, the inversion layer becomes thinner at the drain terminal due to interaction between V_G and V_D.
- If $V_{DS} < V_{GS} - V_T$, then the drain current Id is a function of both V_{GS} and V_{DS}. Furthermore, for a given V_{DS}, I_D increases linearly with ($V_{GS} - V_T$). The transistor is said to be operating in its **linear** or **resistive** region.
- If $V_{DS} > V_{GS} - V_T$, then $V_{GS} < V_T$ and no inversion layer can exist at the drain terminal. The channel is said to be '***pinched-off***'. The transistor is operating in the **saturation** region, where the drain current is dependent on V_{GS} and is almost independent of V_{DS}.

I-V Relation

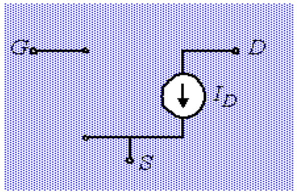


(a) I_D as a function of V_{DS}

(b) $\sqrt{I_D}$ as a function of V_{GS} (for V_{DS} = 5V)

NMOS Enhancement Transistor: W = 100 μm, L = 20 μm

A model for manual analysis



$V_{DS} > V_{GS} - V_T$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

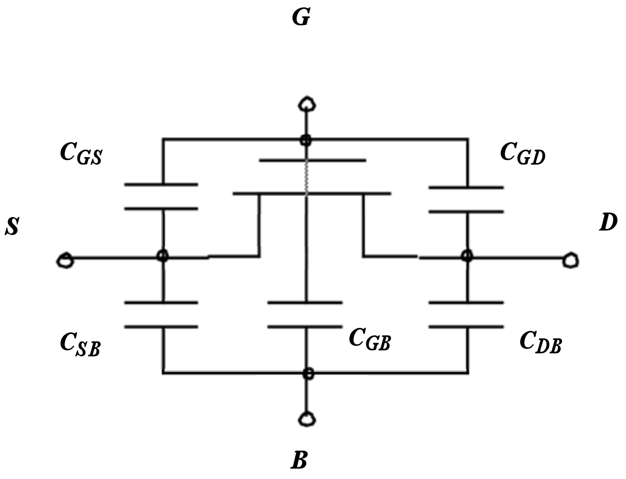
$V_{DS} < V_{GS} - V_T$

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

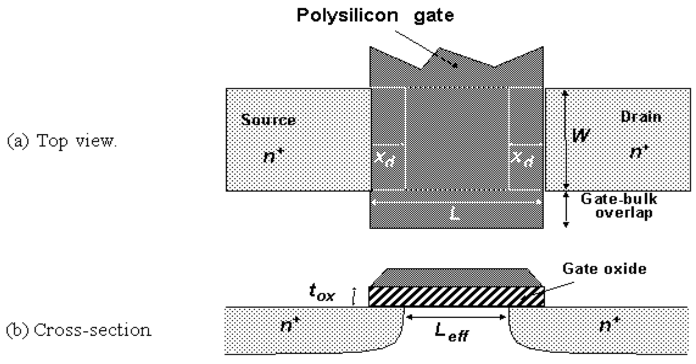
with

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

Dynamic Behavior of MOS Transistor



The Gate Capacitance



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

Average Gate Capacitance

Different distributions of gate capacitance for varying operating conditions

Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

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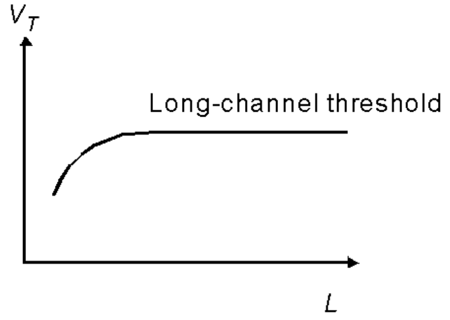
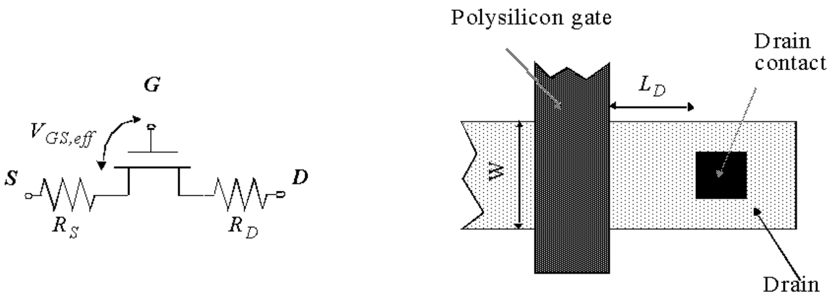
Issues concerning Sub-Micron MOS Transistors

- **Threshold Variations**
- **Parasitic Resistances**
- **Velocity Saturation**
- **Mobility Degradation**

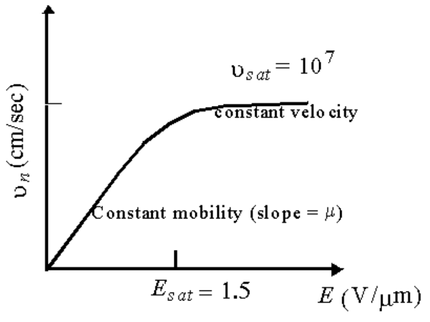


Threshold as a function of the length (for low V_{DS})

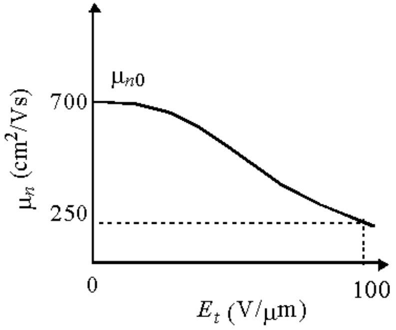
Parasitic Resistances



Velocity Saturation (1)

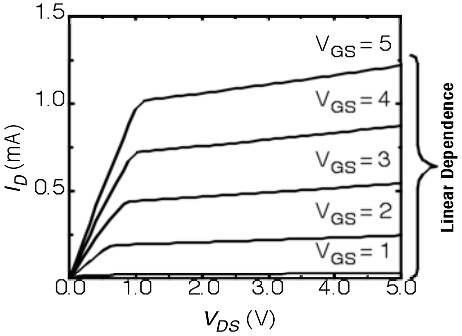


(a) Velocity saturation

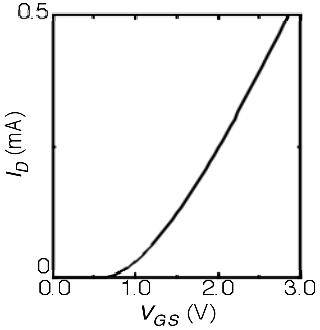


(b) Mobility degradation

Velocity Saturation (2)



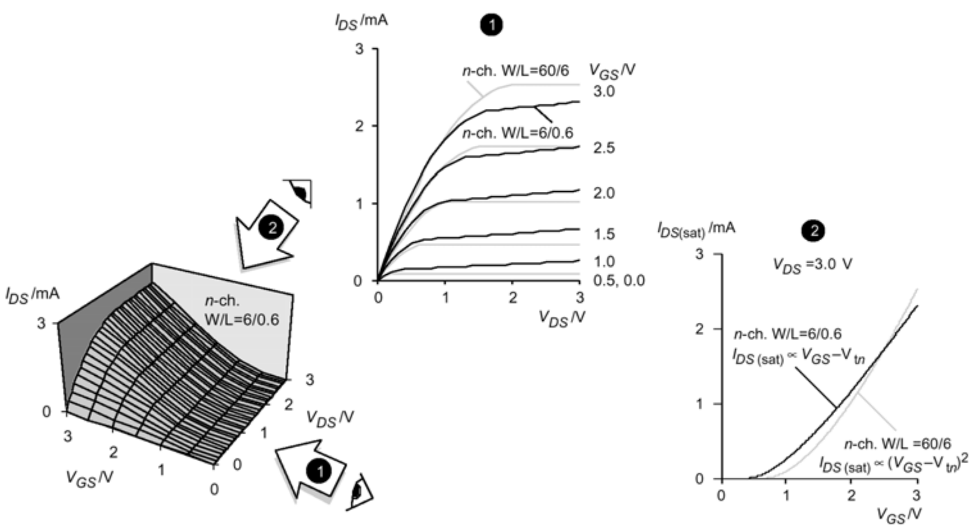
(a) I_D as a function of V_{DS}



(b) I_D as a function of V_{GS} (for V_{DS} = 5 V).

Linear Dependence on V_{GS}

Characteristics of an n-channel transistor



What is SPICE Circuit Simulator?

- **SPICE** is a widely-used circuit-level simulator, originally from Berkeley.
- We use an industrial version - **HSPICE** in the Department
  - You can download WinSPICE which is free (see course web page)
- SPICE uses numerical techniques to solve nodal analysis of circuit. It supports the following:
  - Textual input to specify circuit & simulation commands
  - Text or graphical output format for simulation results
- You can use SPICE to specify these circuit components:
  - Resistors, Capacitors, Inductors
  - Independent sources (V, I), Dependent sources (V, I)
  - Transmission lines
  - Active devices (diodes, BJTs, JFETS, MOSFETS)
- You can use SPICE to perform the following types circuit analysis:
  - **non-linear d.c.**
  - **non-linear transient**
  - linear a.c.
  - Noise & temperature

SPICE MODELS

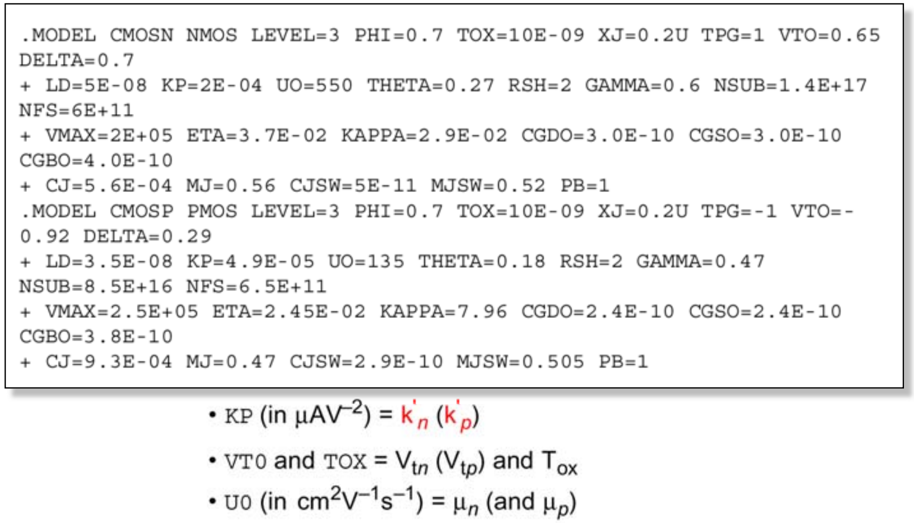
Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

Level 4 (BSIM): Emperical - Simple and Popular

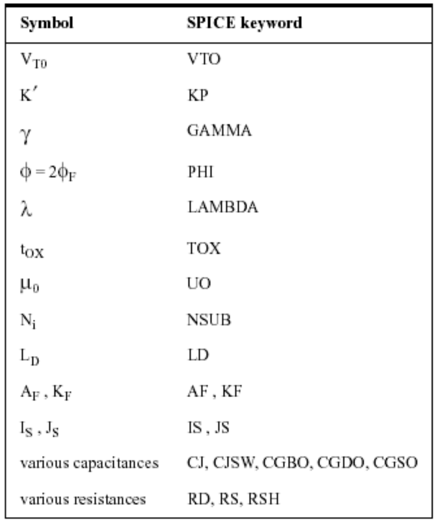
SPICE Parameters



```
.MODEL CMOSN NMOS LEVEL=3 PHI=0.7 TOX=10E-09 XJ=0.2U TPG=1 VTO=0.65
DELTA=0.7
+ LD=5E-08 KP=2E-04 UO=550 THETA=0.27 RSH=2 GAMMA=0.6 NSUB=1.4E+17
NFS=6E+11
+ VMAX=2E+05 ETA=3.7E-02 KAPPA=2.9E-02 CGDO=3.0E-10 CGSO=3.0E-10
CGBO=4.0E-10
+ CJ=5.6E-04 MJ=0.56 CJSW=5E-11 MJSW=0.52 PB=1
.MODEL CMOSP PMOS LEVEL=3 PHI=0.7 TOX=10E-09 XJ=0.2U TPG=-1 VTO=-
0.92 DELTA=0.29
+ LD=3.5E-08 KP=4.9E-05 UO=135 THETA=0.18 RSH=2 GAMMA=0.47
NSUB=8.5E+16 NFS=6.5E+11
+ VMAX=2.5E+05 ETA=2.45E-02 KAPPA=7.96 CGDO=2.4E-10 CGSO=2.4E-10
CGBO=3.8E-10
+ CJ=9.3E-04 MJ=0.47 CJSW=2.9E-10 MJSW=0.505 PB=1
```

- `KP` (in μAV^{-2}) = k'_n (k'_p)
- `VTO` and `TOX` = V_{tn} (V_{tp}) and T_{ox}
- `UO` (in $cm^2V^{-1}s^{-1}$) = μ_n (and μ_p)

MAIN MOS SPICE PARAMETERS

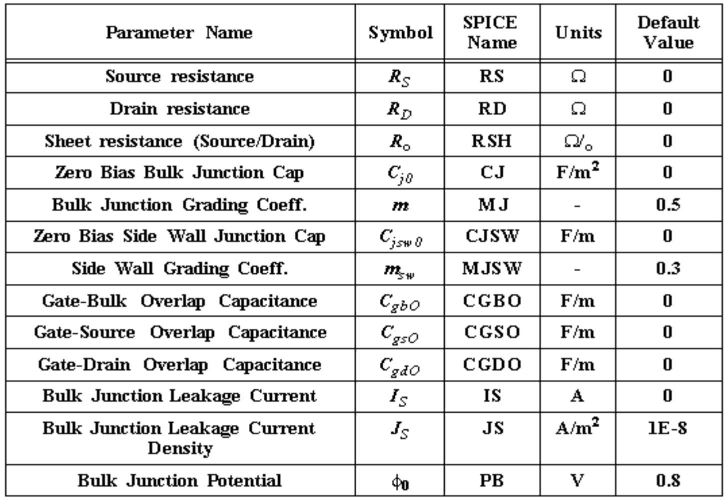


Symbol	SPICE keyword
V_{T0}	VTO
K'	KP
γ	GAMMA
$\phi = 2\phi_F$	PHI
λ	LAMBDA
t_{OX}	TOX
μ_0	UO
N_i	NSUB
L_D	LD
A_F , K_F	AF , KF
I_S , J_S	IS , JS
various capacitances	CJ, CJSW, CGBO, CGDO, CGSO
various resistances	RD, RS, RSH

SPICE Transistors Parameters

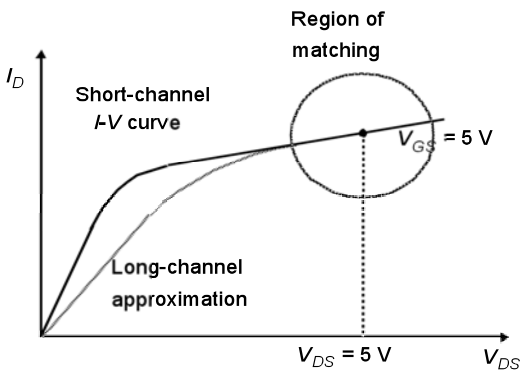
Parameter Name	Symbol	SPICE Name	Units	Default Value
Drawn Length	L	L	m	-
Effective Width	W	W	m	-
Source Area	AREA	AS	m2	0
Drain Area	AREA	AD	m2	0
Source Perimeter	PERIM	PS	m	0
Drain Perimeter	PERIM	PD	m	0
Squares of Source Diffusion		NRS	-	1
Squares of Drain Diffusion		NRD	-	1

SPICE Parameters for Parasitics



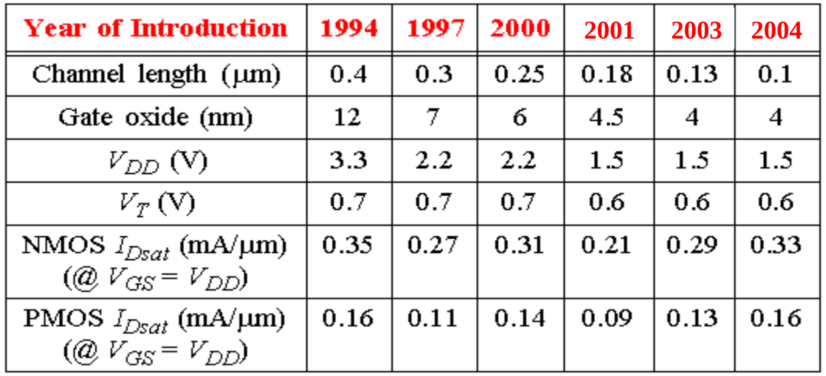
Parameter Name	Symbol	SPICE Name	Units	Default Value
Source resistance	R_S	RS	Ω	0
Drain resistance	R_D	RD	Ω	0
Sheet resistance (Source/Drain)	$R_\circ$	RSH	$\Omega/_\circ$	0
Zero Bias Bulk Junction Cap	C_{j0}	CJ	F/m^2	0
Bulk Junction Grading Coeff.	m	MJ	-	0.5
Zero Bias Side Wall Junction Cap	C_{jsw0}	CJSW	F/m	0
Side Wall Grading Coeff.	m_{sw}	MJSW	-	0.3
Gate-Bulk Overlap Capacitance	C_{gbO}	CGBO	F/m	0
Gate-Source Overlap Capacitance	C_{gsO}	CGSO	F/m	0
Gate-Drain Overlap Capacitance	C_{gdO}	CGDO	F/m	0
Bulk Junction Leakage Current	I_S	IS	A	0
Bulk Junction Leakage Current Density	J_S	JS	A/m^2	1E-8
Bulk Junction Potential	ϕ_0	PB	V	0.8

Fitting level-1 model for manual analysis



Select k' and λ such that best matching is obtained @ $V_{gs} = V_{ds} = V_{DD}$

Technology Evolution



Year of Introduction	1994	1997	2000	2001	2003	2004
Channel length (µm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/µm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/µm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16