Introduction to Digital Integrated Circuit Design

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URL: http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/index.html
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Aims and Objectives

- The aim of this course is to introduce the basics of digital integrated circuits design.
- After following this course you will be able to:
  - Comprehend the different issues related to the development of digital integrated circuits including fabrication, circuit design, implementation methodologies, testing, design methodologies and tools and future trends.
  - Use tools covering the back-end design stages of digital integrated circuits.

Course Outline

Week	Lectures	Laboratory/Project
1	Introduction and Trends	
2	Basic MOS Theory, SPICE Simulation, CMOS Fabrication	Learning Electric & SPICE simulation
3	Inverters and Combinational Logic	Learning Layout with Electric
4	Sequential Circuits	Switch-level simulation with IRSIM
5	Timing and Interconnect Issues	Finishing the previous labs
6	Data Path Circuits	Design Project
7	Memory and Array Circuits	Design Project
8	Low Power Design Package, Power and I/O	Design Project
9	Design for Test	Design Project
10	Design Methodologies and Tools	Design Project

Recommended Books

- N. H. E. Weste and D. Harris, **"CMOS VLSI Design: A Circuits and Systems Perspective",** 3rd Edition**,** Addison-Wesley, ISBN 0-321-14901-7, May 2004.
- J. Rabaey, A. Chandrakasan, B. Nikolic, **"Digital Integrated Circuits: A Design Perspective"** 2nd Edition, Prentice Hall, ISBN 0131207644, January 2003.
- W. Wolf, **"Modern VLSI Design: System-on-Chip Design",** 3rd Edition, Prentice Hall, ISBN 0-13-061970-1, 2002.
- M.J.S. Smith, **"Application-Specific Integrated Circuits"**, Addison-Wesley, ISBN 0-201-50022-1, 1997.
- L. A. Glasser and D. W. Dobberpuhl, **"The Design and Analysis of VLSI Circuits"**. Addison-Wesley, ISBN 0-201-12580-3, 1985. Detailed analysis of circuits, but largely nMOS.
- C. A. Mead and L. A. Conway, **"Introduction to VLSI Systems"**. Addison-Wesley, ISBN 0-201-04358-0, 1980. The first textbook in this subject, a bit old!

Supporting Material

- Lectures notes - reference to textbooks if relevant
- Material for further reading
- Notes for laboratory/project

- Consult the course web-page:

  http://www.ee.ic.ac.uk/pcheung/teaching/ee4_asic/index.html

Design Project

- Lab sessions: TBA, Mahanakorn Lab (Level 9)

- Spend first 4 weeks learning CAD tools (Electric, IRSIM, SPICE)
  - Public domain tools – links from course web-page
  - All tools are installed in the Departmental computers - you are encouraged to install them on your PCs
- Spend the remaining weeks working in small groups to design a chip
- Deadline for completion: Last day of Autumn term
- Deadline for report: First day of Spring term

- Report (one per group) should include:
  - description of circuit designed (full schematic and layout)
  - block diagram showing different module in chip
  - plot of the entire chip
  - evidence that it works (from simulation plots)
  - test strategy and testbench
  - a description of contribution from each member, signed by all!

Assessment

- May/June examination (open-book) - 75%

- Course work designing a chip in a group (3-4 people) - 25%

Topic 1
Introduction & Trends

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Based on slides/material by…

- J. Rabaey http://bwrc.eecs.berkeley.edu/Classes/IcBook/instructors.html
  "Digital Integrated Circuits: A Design Perspective", Prentice Hall
- D. Harris http://www.cmosvlsi.com/coursematerials.html
  Weste and Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley
- M. Smith
  http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/ASICs.htm
  "Application Specific Integrated Circuits", Addison Wesley

Recommended Reading

- J. Rabaey et. al. "Digital Integrated Circuits: A Design Perspective": Chapter 1 (1.1 – 1.2), Chapter 8
- Weste and Harris, "CMOS VLSI Design: A Circuits and Systems Perspective": Chapter 1 (1.1 – 1.2), Chapter 4 (4.9), Chapter 8 (8.5)
- M. Smith, "Application Specific Integrated Circuits" : Chapter 1

Outline

- **History**
- Implementation methodologies
- Design flow
- Technology scaling
- VLSI/IC economics
- Future trends

Integrated Circuits

- Integrated circuits are made on a thin (a few hundred microns thick), circular silicon wafer
- Each wafer holds hundreds of die
- Transistors and wiring are made from many layers built on top of one another
- Each successive mask layer has a pattern that is defined using a mask similar to a glass photographic slide
- First group of layers define transistors
- The remaining layers define metal wires between transistors (interconnect)

A Brief History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2003
  - Intel Pentium 4 μProcessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

History of Integration

- A **gate equivalent** is a NAND gate $F = \overline{A \bullet B}$, or four transistors

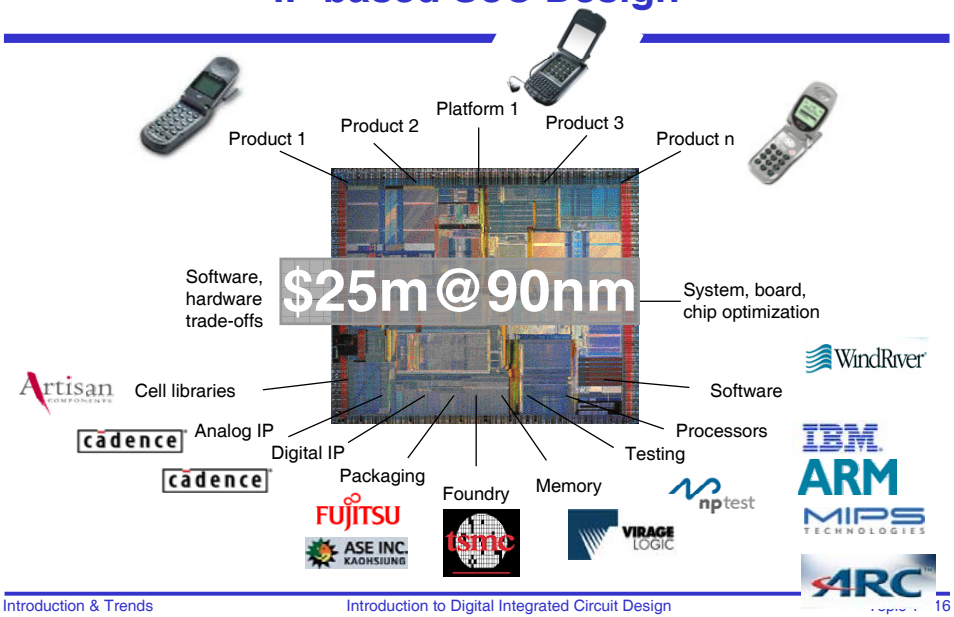
- **small-scale integration** (**SSI**, ~10 gates per chip, 60's)
- **medium-scale integration** (**MSI**, ~100–1000 gates per chip, 70's)
- **large-scale integration** (**LSI**, ~1000–10,000 gates per chip, 80's)
- **very large-scale integration** (**VLSI**, ~10,000–100,000 gates per chip, 90's)
- **ultra-large scale integration** (**ULSI**, ~1M–10M gates per chip)

History of Technology

- **bipolar technology** and **transistor–transistor logic** (**TTL**) preceded ...
- **metal-oxide-silicon** (**MOS**) technology because it was difficult to make metal-gate n-channel MOS (**nMOS** or **NMOS**)
- the introduction of **complementary MOS** (**CMOS**) greatly reduced power

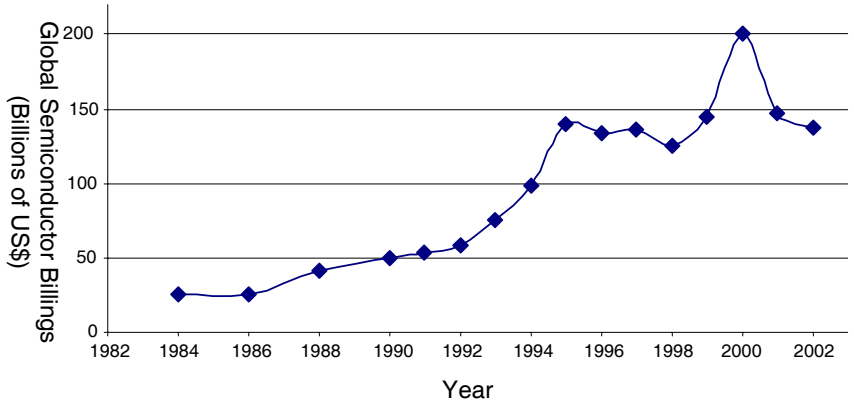
- The **feature size** is the smallest shape you can make on a chip and is measured in **λ** or **lambda**

IP based SoC Design

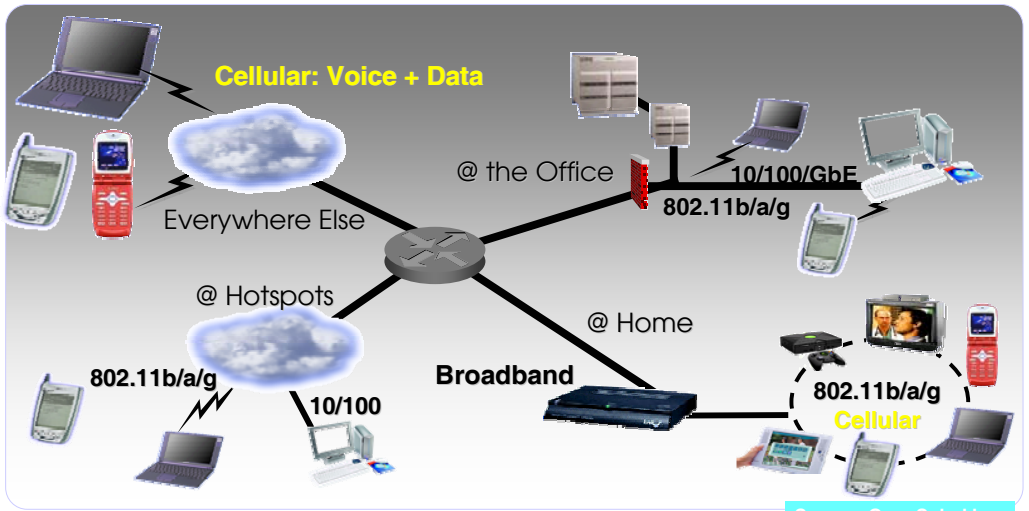


Annual Sales

- 10^{18} transistors manufactured in 2003
  - 100 million for every human on the planet



Any Device, Any Time, Anywhere

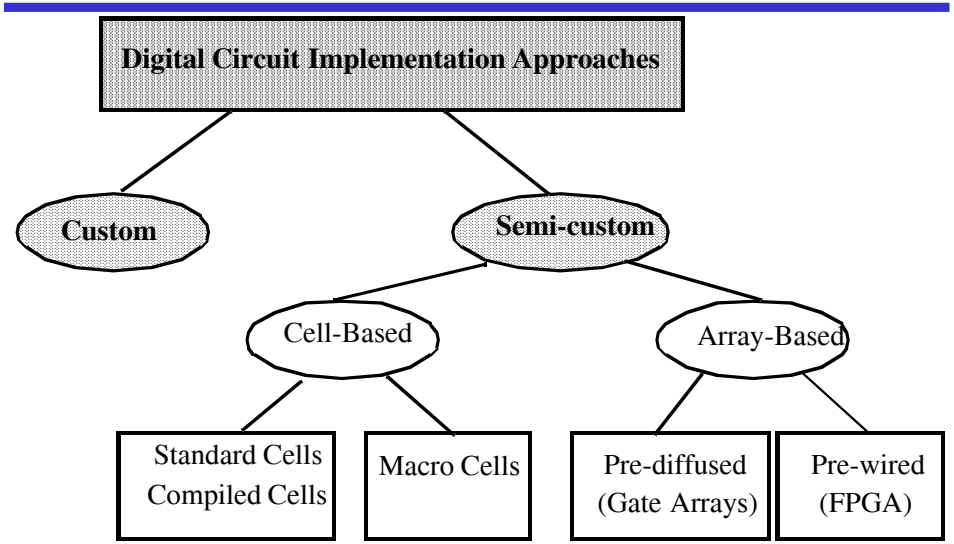


2010: 1.5 billion interconnected PCs,
2.5 billion interconnected PDAs

Outline

- History
- **Implementation methodologies**
- Design flow
- Technology scaling
- VLSI/IC economics
- Future trends

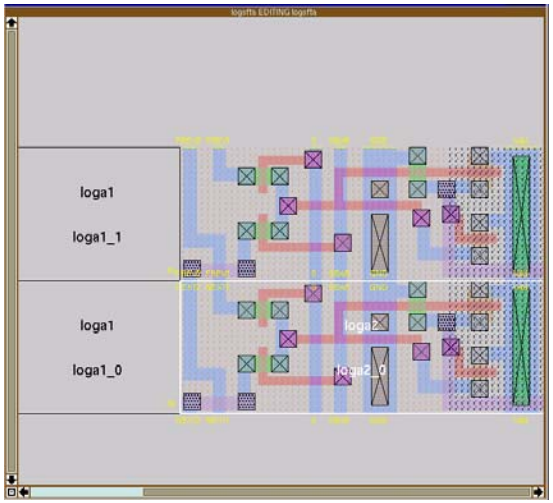
Implementation Methodologies



Full-custom

- All mask layers are customized in a full-custom IC.
- Full-custom offers the highest performance and lowest part cost (smallest die size) with the disadvantages of increased design time, complexity, design expense, and highest risk.
- Microprocessors were exclusively full-custom, but designers are increasingly turning to semi-custom techniques in this area too.
- Other examples of full-custom ICs are: high-voltage (automobile), analog/digital (communications), or sensors and actuators.
- Makes sense for performance critical parts or if there are no libraries available.

Custom Design - Layout

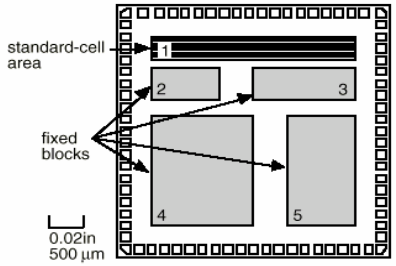


Magic Layout Editor
(UC Berkeley)

Standard-Cell–Based ICs

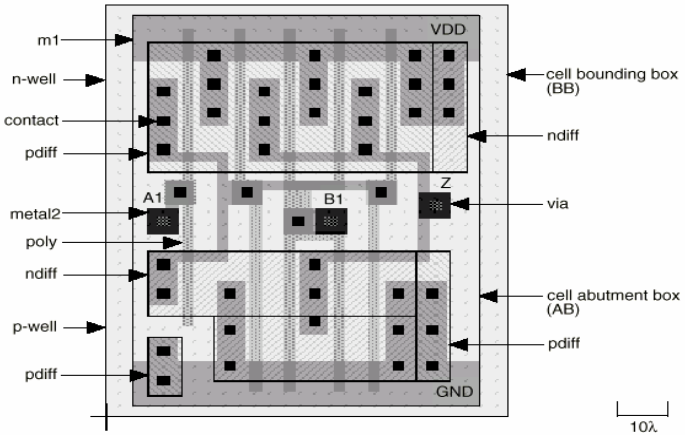
A **cell-based ASIC** (**CBIC**—"sea-bick")

- Standard cells
- Possibly **megacells**, **megafunctions**, **full-custom blocks**, **system-level macros** (**SLMs**), **fixed blocks**, **cores**, or **Functional Standard Blocks** (**FSBs**)
- All mask layers are customized—transistors and interconnect
- Custom blocks can be embedded
- Manufacturing lead time is about eight weeks.



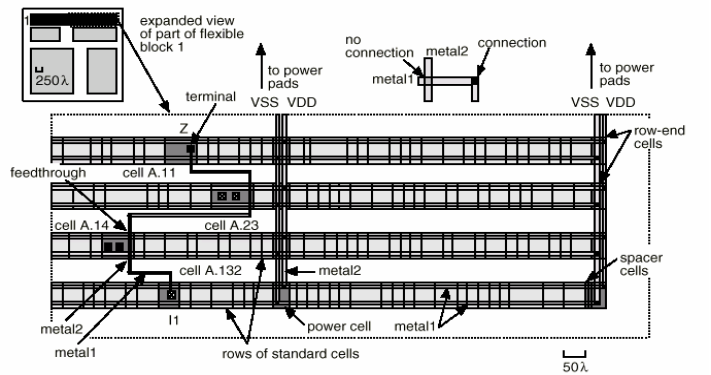
- In **datapath** (**DP**) logic we may use a **datapath compiler** and a **datapath library**. Cells such as **arithmetic and logical units** (**ALUs**) are **pitch-matched** to each other to improve timing and density.

Full-custom Standard Cell



Looking down on the layout of a **standard cell** from a **standard-cell library**

Routing a Standard Cell-based IC

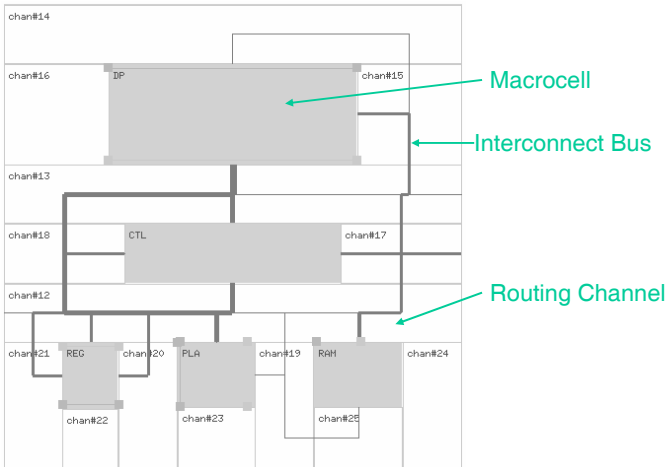


- Routing a CBIC (cell-based IC)
  - A "wall" of standard cells forms a **flexible block**
  - **metal2** may be used in a **feedthrough cell** to cross over cell rows that use **metal1** for wiring
  - Other wiring cells: **spacer cells**, **row-end cells**, and **power cells**

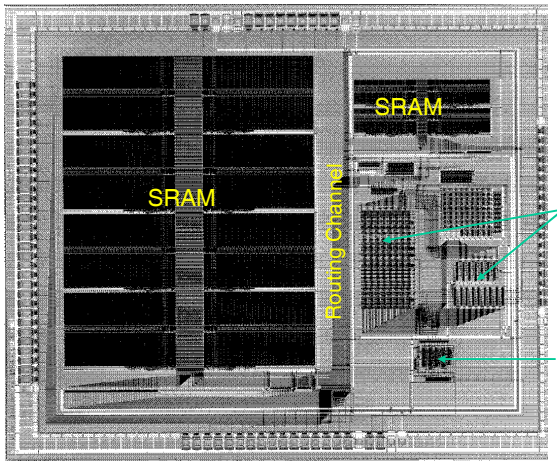
Standard Cell Libraries

- Use a **design kit** from the **IC vendor**
- Buy an **IC-vendor library** from a **library vendor**
- Build your own cell library

Macrocell-Based Design



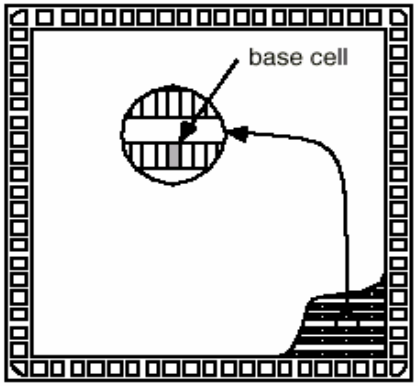
Macrocell-Based Design Example



Video-encoder chip
[Brodersen92]

Gate-Array–Based ICs

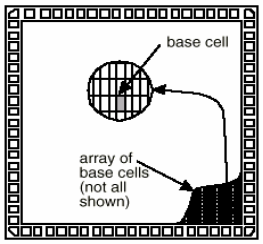
- A **gate array**, **masked gate array**, **MGA**, or **prediffused array** uses **macros** (**books**) to reduce **turnaround time** and comprises a **base array** made from a **base cell** or **primitive cell**. There are three types:
  - Channeled gate arrays
  - Channelless gate arrays
  - Structured gate arrays

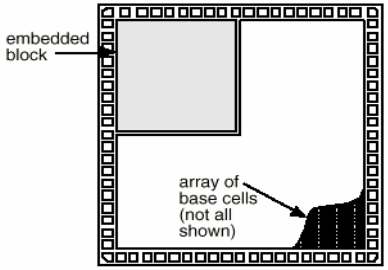


- A **channeled gate array**
  - The interconnect uses predefined spaces between rows of base cells

Gate-Array–Based ICs (con't)

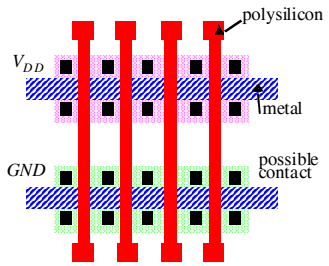
- A **channelless gate array** (**channel-free gate array**, **sea-of-gates array**, or **SOG** array)
  - Routing uses rows of unused transistors



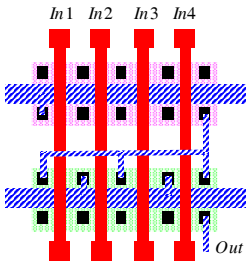


- An **embedded gate array** or **structured gate array** (**masterslice** or **masterimage**)
  - Either channeled or channelless
  - Custom blocks (the same for each design) can be embedded

Gate Array Approach - Example



Uncommited Cell

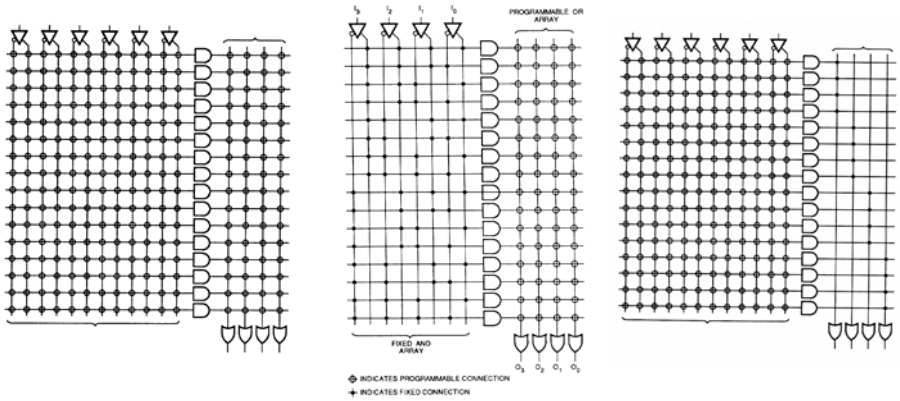


Committed Cell (4-input NOR)

Prewired Arrays

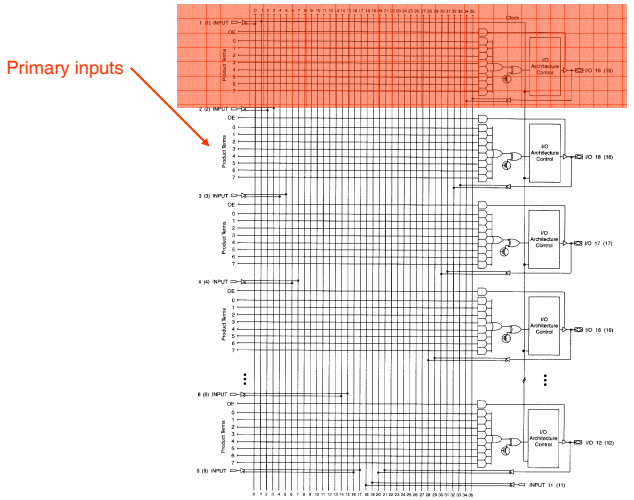
- Categories of prewired arrays (or field-programmable devices):
  - Fuse-based (program-once)
  - Non-volatile EPROM based
  - RAM based

Programmable Logic Devices



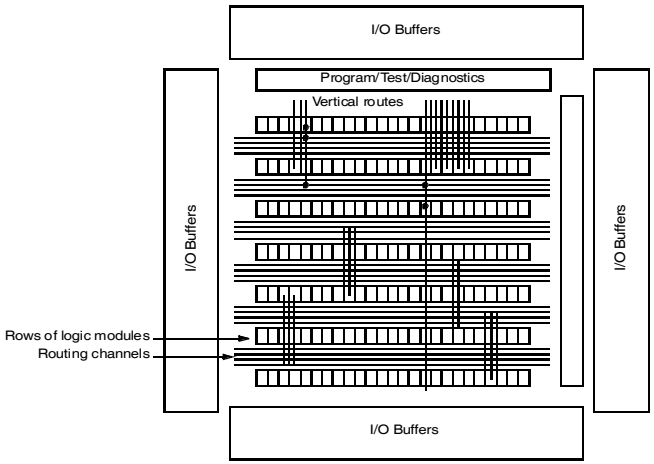
PLA PROM PAL

EPLD Block Diagram



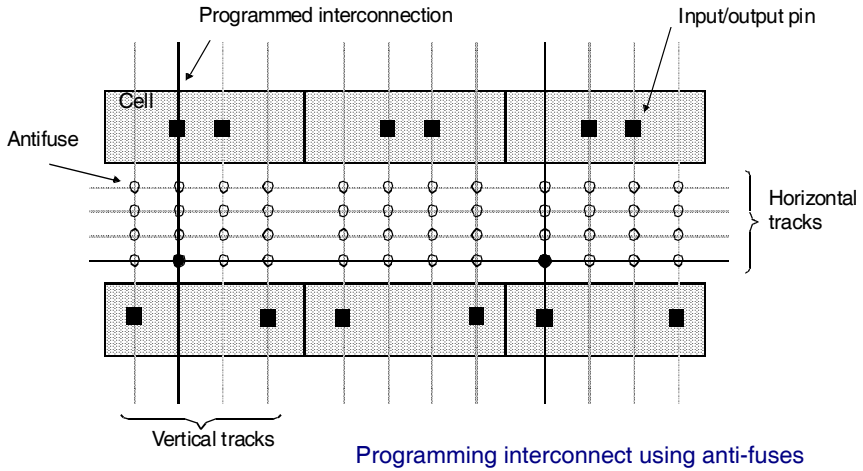
Courtesy Altera Corp.

Field-Programmable Gate Arrays Fuse-based



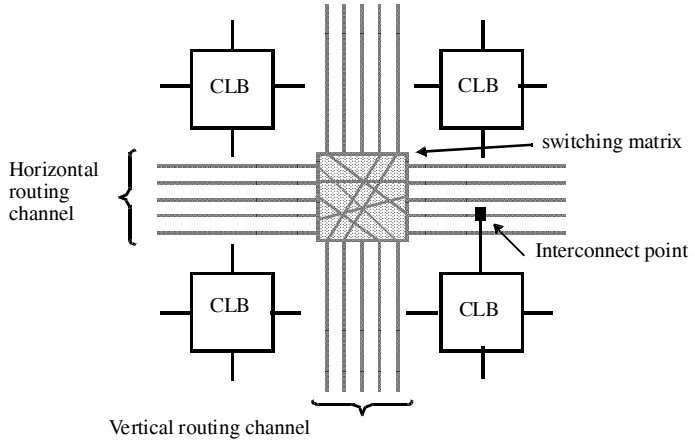
Standard-cell like floorplan

Interconnect

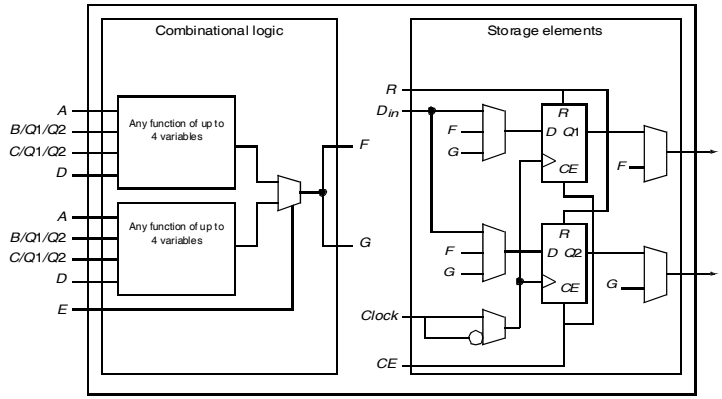


Programming interconnect using anti-fuses

Field-Programmable Gate Arrays RAM-based



RAM-based FPGA Basic Cell (CLB)

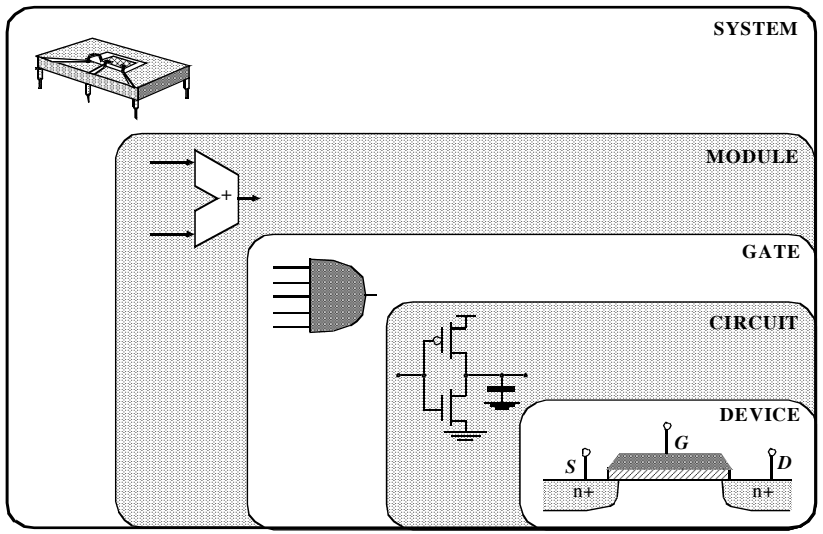


Courtesy of Xilinx

Outline

- History
- Implementation methodologies
- **Design flow**
- Technology scaling
- VLSI/IC economics
- Future trends

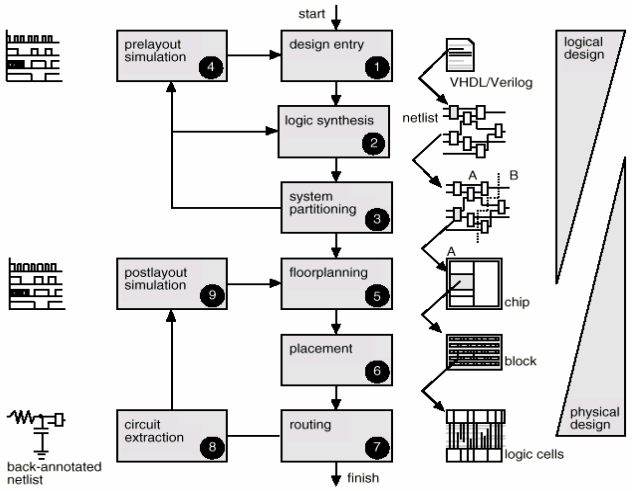
Design Abstraction Levels



ASIC Design Flow

- A **design flow** is a sequence of steps to design an ASIC
  - **Design entry**.
  - **Logic synthesis**.
  - **Pre-layout simulation**.
  - **Floorplanning**.
  - **Placement**.
  - **Routing**.
  - **Extraction**.
  - **Postlayout simulation**.

ASIC Design Flow (con't)



ASIC design flow. Steps 1–4 are **logical design**, and steps 5–9 are **physical design**

Outline

- History
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- **Technology scaling**
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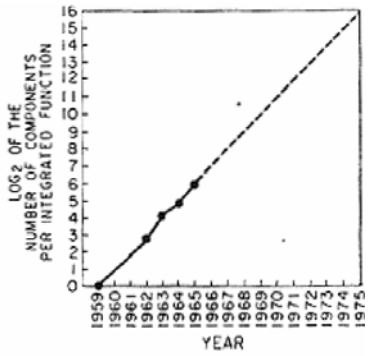
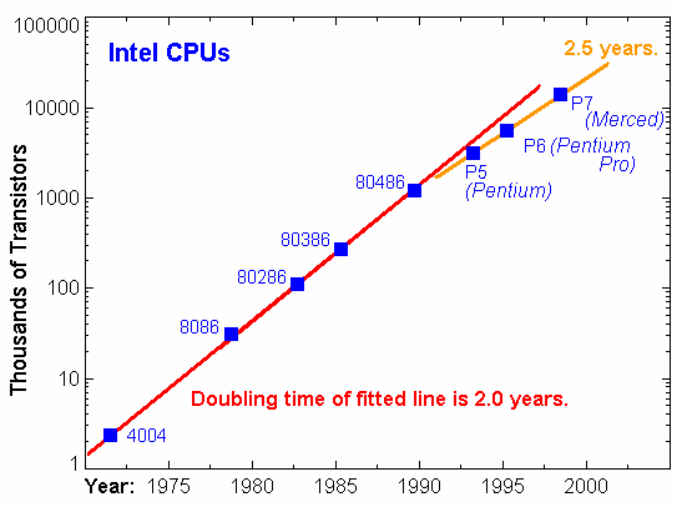
- Future trends

Moore's Law

- In 1965, Gordon Moore, co-founder of Intel, predicted the exponential growth of the number of transistors on an IC (number of transistors per square inch in ICs to double every year)
- Predicted > 65,000 transistors by 1975!
- In subsequent years, the pace slowed down a bit, but density has doubled approximately every 18 months, and this is the current definition of Moore's Law.
- Growth limited by power
- Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades

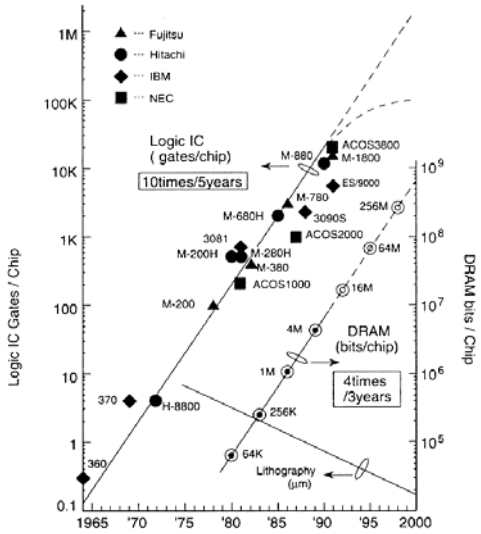


Moore's Law – Intel Microprocessors



Source: Intel

Evolution in Complexity

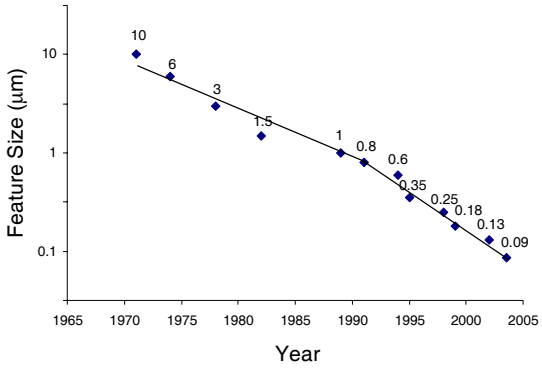


Why ?

- Why more transistors per IC?
  - Smaller transistors
  - Larger dice
- Why faster computers?
  - Smaller, faster transistors
  - Better microarchitecture
  - Fewer gate delays per cycle

Scaling

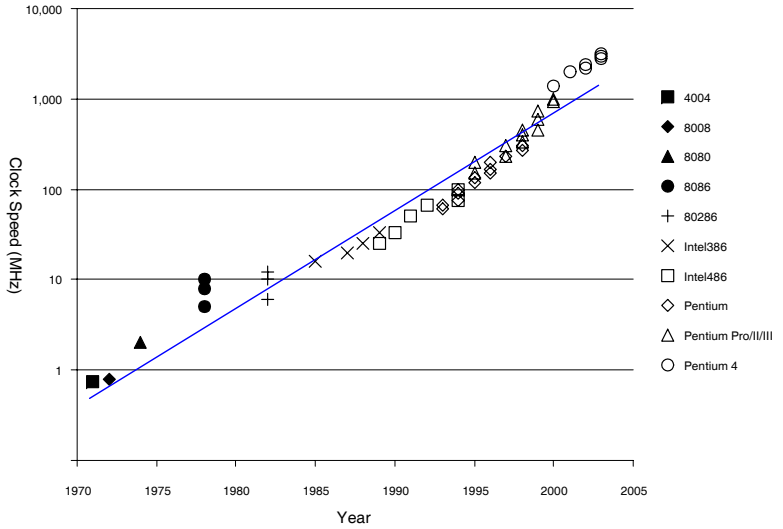
- The only constant in VLSI/IC design is constant change
- Feature size shrinks by 30% every 2-3 years
  - Transistors become smaller, faster, less power hungry, cheaper to manufacture
  - Noise, reliability issues
  - Current density goes up
  - Wires do not improve (and may get worse)
- Scale factor $S \approx \sqrt{2}$
  - Typically
  - Technology nodes



Scaling Implications

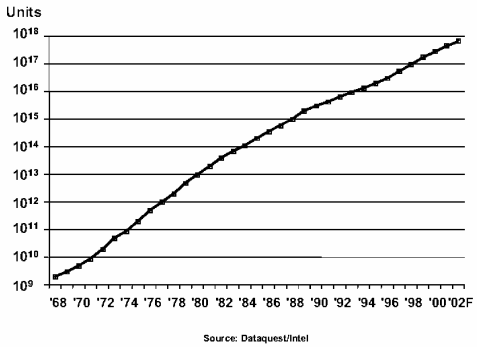
- Improved Performance
- Improved Cost
- Interconnect Woes
- Power Woes
- Productivity Challenges
- Physical Limits

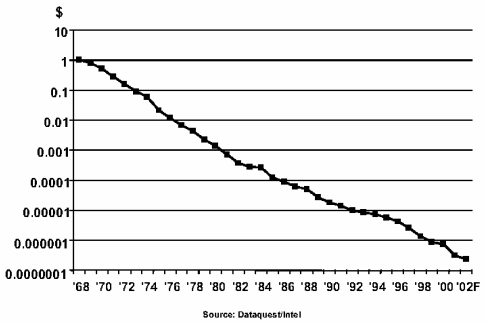
Performance Improvement



Cost Improvement

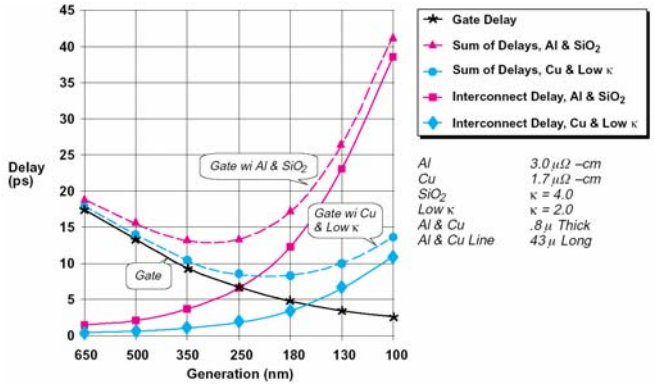
- In 2003, $0.01 bought you 100,000 transistors





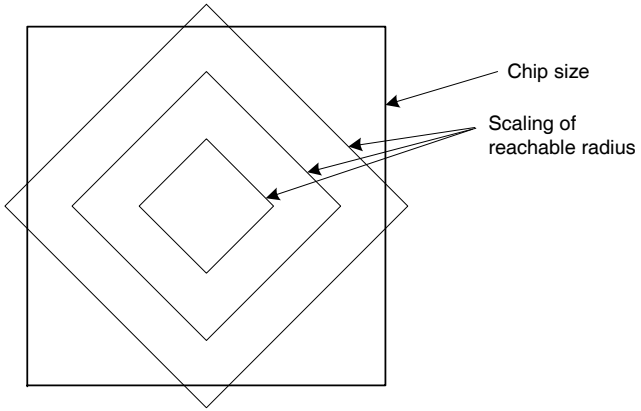
Interconnect Woes

- SIA made a gloomy forecast in 1997
  - Delay would reach minimum at 250 – 180 nm, then get worse because of wires
- But…
  - Misleading scale
  - Global wires
- 100 kgate blocks ok



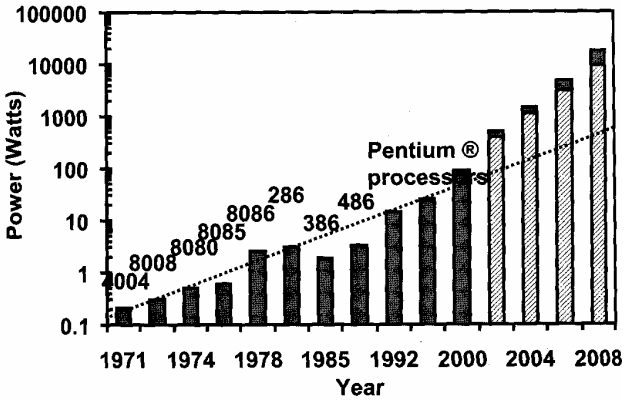
Reachable Radius

- We can't send a signal across a large fast chip in one cycle anymore
- But the microarchitect can plan around this
  - Just as off-chip memory latencies were tolerated



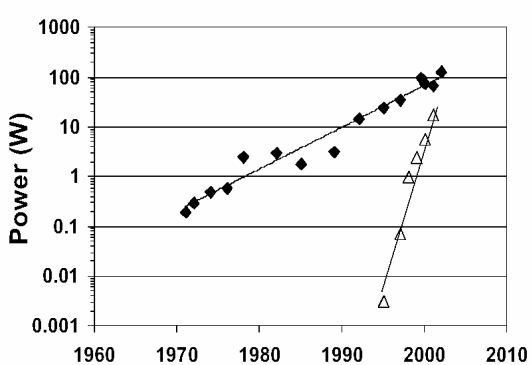
Dynamic Power

- Intel VP Patrick Gelsinger (ISSCC 2001)
  - If scaling continues at present pace, by 2005, high speed processors would have power density of nuclear reactor, by 2010, a rocket nozzle, and by 2015, surface of sun.
  - "Business as usual will not work in the future."
- Intel stock dropped 8% on the next day
- But attention to power is increasing



Static Power

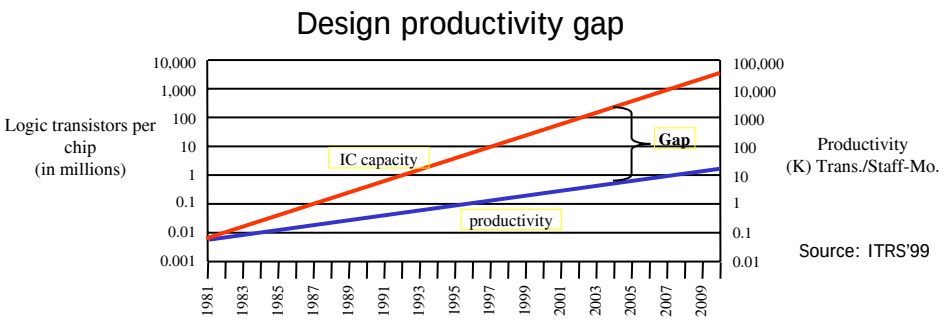
- V_{DD} decreases
  - Save dynamic power
  - Protect thin gate oxides and short channels
  - No point in high value because of velocity sat.
- V_t must decrease to maintain device performance
- But this causes exponential increase in OFF leakage
- Major future challenge



Productivity

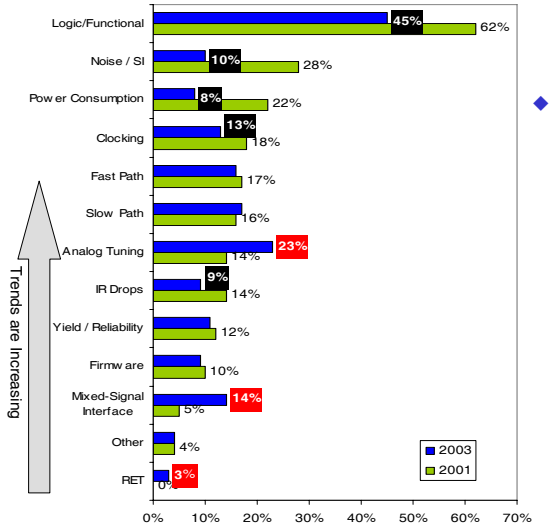
- Transistor count is increasing faster than designer productivity (gates / week)
  - Bigger design teams
    - ↗ Up to 500 for a high-end microprocessor
  - More expensive design cost
  - Pressure to raise productivity
    - ↗ Rely on synthesis, IP blocks
  - Need for good engineering managers

Very Few Companies Can Design High-End ICs



- Designer productivity growing at slower rate
  - 1981: 100 designer months → ~$1M
  - 2002: 30,000 designer months → **~$300M**

Less First Silicon Success and the Changing Rate of Failures



- **First silicon success rates declining**
  - **First Silicon OK**
    48% in 2000
    39% in 2002
    34% in 2003
  - **Third Silicon OK**
    >90% in 2000
    >70% in 2002
    >60% in 2003

Trends are Decreasing

Collett International Research:
2000, 2002 Functional Verification Studies;
2003 Design Closure Study, 01/04

Physical Limits

- Will Moore's Law run out of steam?
  - Can't build transistors smaller than an atom…
- Many reasons have been predicted for end of scaling
  - Dynamic power
  - Subthreshold leakage, tunneling
  - Short channel effects
  - Fabrication costs
  - Electromigration
  - Interconnect delay
- Rumors of demise have been exaggerated

Outline

- History
- Implementation methodologies
- Design flow
- Technology scaling
- **VLSI/IC economics**
- Future trends

Integrated Circuits Economics

- Selling price S_{total}
  - $S_{total} = C_{total} / (1-m)$
- m = profit margin
- C_{total} = total cost
  - Nonrecurring engineering cost (NRE)
  - Recurring cost
  - Fixed cost

Non-Recurring Engineering Costs (NRE)

- Engineering cost
  - Depends on size of design team
  - Include benefits, training, computers
  - CAD tools:
    - Digital front end: $10K
    - Analog front end: $100K
    - Digital back end: $1M
- Prototype manufacturing
  - Mask costs: $500k – 1M in 130 nm process
  - Test fixture and package tooling

Recurring Costs

- Fabrication
  - Wafer cost / (Dice per wafer * Yield)
  - Wafer cost: $500 - $3000
  - Dice per wafer:

$$N = \pi\left[\frac{r^2}{A} - \frac{2r}{\sqrt{2A}}\right]$$

  - Yield: $Y = e^{-AD}$
    - For small A, $Y \approx 1$, cost proportional to area
    - For large A, $Y \rightarrow 0$, cost increases exponentially
- Packaging
- Test

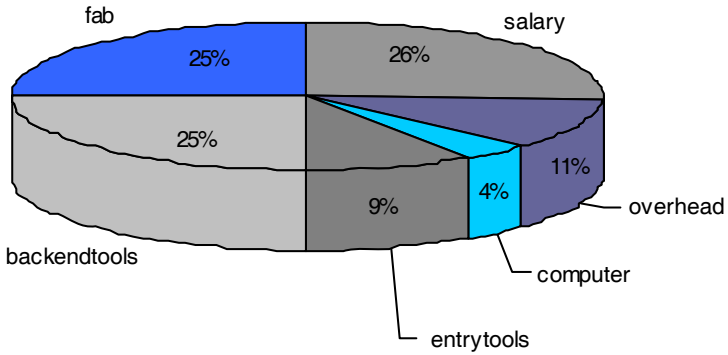
Fixed Cost

- Data sheets and application notes
- Marketing and advertising
- Yield analysis

New IC Design is Fairly Capital Intensive

- Estimated capital to start a company to design a wireless communication IC
- Digital designers (7):
  - $70k salary
  - $30k overhead
  - $10k computer
  - $10k CAD tools
  - Total: $120k * 7 = $840k
- Analog designers (3)
  - $100k salary
  - $30k overhead
  - $10k computer
  - $100k CAD tools
  - Total: $240k * 3 = $720k
- Support staff (5)
  - $45k salary
  - $20k overhead
  - $5k computer
  - Total: $70k * 5 = $350k
- Fabrication
  - Back-end tools: $1M
  - Masks: $1M
  - Total: $2M / year
- Summary
  - 2 years @ $3.91M / year
  - $8M design & prototype

Cost Breakdown



Outline

- History
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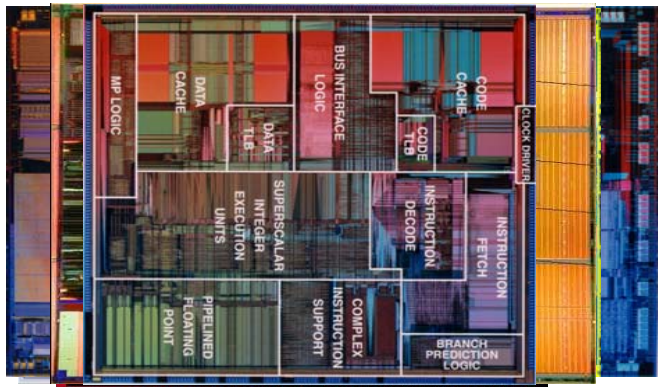
Evolution of Intel Microprocessors



1974 1982 1989 1993 1997 1999 2002

Intel Microprocessors Summary

- 10^4 increase in transistor count, clock frequency over 30 years!

Table 4.19 History of Intel microprocessors over three decades

Processor	Year	Feature Size (μm)	Transistors	Frequency (MHz)	Word size	Package
4004	1971	10	2.3k	0.75	4	16-pin DIP
8008	1972	10	3.5k	0.5–0.8	8	18-pin DIP
8080	1974	6	6k	2	8	40-pin DIP
8086	1978	3	29k	5–10	16	40-pin DIP
80286	1982	1.5	134k	6–12	16	68-pin PGA
Intel386	1985	1.5–1.0	275k	16–25	32	100-pin PGA
Intel486	1989	1–0.6	1.2M	25–100	32	168-pin PGA
Pentium	1993	0.8–0.35	3.2–4.5M	60–300	32	296-pin PGA
Pentium Pro	1995	0.6–0.35	5.5M	166–200	32	387-pin MCM PGA
Pentium II	1997	0.35–0.25	7.5M	233–450	32	242-pin SECC
Pentium III	1999	0.25–0.18	9.5–28M	450–1000	32	330-pin SECC2
Pentium 4	2001	0.18–0.13	42–55M	1400–3200	32	478-pin PGA

Silicon in 2010

Die Area: 2.5x2.5 cm
Voltage: 0.6 V
Technology: 0.07 μm

	Density (Gbits/cm2)	Access Time (ns)
DRAM	8.5	10
DRAM (Logic)	2.5	10
SRAM (Cache)	0.3	1.5

	Density (Mgates/cm2)	Max. Ave. Power (W/cm2)	Clock Rate (GHz)
Custom	25	54	3
Std. Cell	10	27	1.5
Gate Array	5	18	1
Single-Mask GA	2.5	12.5	0.7
FPGA	0.4	4.5	0.25

ITRS

- Semiconductor Industry Association forecast
  - Intl. Technology Roadmap for Semiconductors

Table 4.17 Predictions from the 2002 ITRS

Year	2001	2004	2007	2010	2013	2016
Feature size (nm)	130	90	65	45	32	22
V_{DD} (V)	1.1–1.2	1–1.2	0.7–1.1	0.6–1.0	0.5–0.9	0.4–0.9
Millions of transistors/die	193	385	773	1564	3092	6184
Wiring levels	8–10	9–13	10–14	10–14	11–15	11–15
Intermediate wire pitch (nm)	450	275	195	135	95	65
Interconnect dielectric constant	3–3.6	2.6–3.1	2.3–2.7	2.1	1.9	1.8
I/O signals	1024	1024	1024	1280	1408	1472
Clock rate (MHz)	1684	3990	6739	11511	19348	28751
FO4 delays/cycle	13.7	8.4	6.8	5.8	4.8	4.7
Maximum power (W)	130	160	190	218	251	288
DRAM capacity (Gbits)	0.5	1	4	8	32	64

Summary

- Integrated circuits are the faster growing technology the last 45 years
- Different implementation methodologies
  - Trade-off: design and turn around time vs design density and performance
- Abstraction is the basis of design flows and tools
- The only constant in VLSI design is scaling
  - Moore's Law and implications
- The development of integrated circuits requires large investment
- 32nm in 2013, what next ?

Journals and Conferences

- IEEE Journal of Solid State Circuits
- IEICE Transactions on Electronics (Japan)
- IEEE Transactions on VLSI Systems

- International Solid-State and Circuits Conference (ISSCC)
- VLSI Circuits Symposium
- Custom Integrated Circuits Conference (CICC)
- European Solid-State Circuits Conference (ESSCIRC)
- International ASIC Conference

Further Reading

- Original article by Moore
- Article on Moore's Law
- International Technology Roadmap for Semiconductors (2003 Edition, 2004 Update)
- **Assignment:** Analysis of ITRS 2003 Edition (or 2004 update)