Topic 2

Basic MOS Theory, SPICE Simulation, CMOS Fabrication

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Based on slides/material by…

- J. Rabaey http://bwrc.eecs.berkeley.edu/Classes/IcBook/instructors.html
  “Digital Integrated Circuits: A Design Perspective”, Prentice Hall
- D. Harris http://www.cmosvlsi.com/coursematerials.html
  Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Addison Wesley

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Recommended Reading

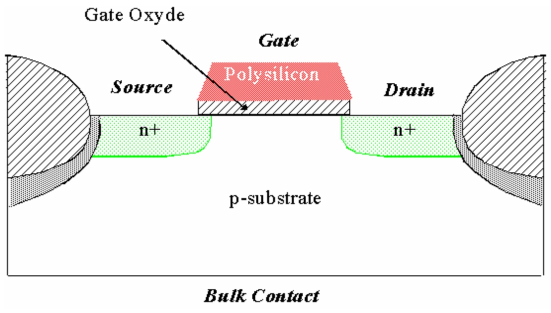
- J. Rabaey et. al. “Digital Integrated Circuits: A Design Perspective”: Chapter 2 (2.1 – 2.3), Chapter 3 (3.3)
- Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”: Chapter 2, Chapter 3 (3.2), Chapter 5.

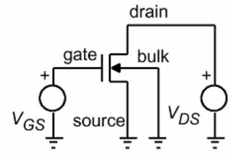
Outline

- **MOS transistors**
- SPICE simulation
- CMOS fabrication process
- Layout rules

MOS Transistor

- Shown here is the cross-section of an n-channel enhancement transistor:
- Substrate is moderately doped with p-type material. Substrate in digital circuit is usually connected to V_{Gnd} (ground).
- The source and drain regions are heavily doped with n-type material through diffusion. These are often referred to as the **diffusion** regions.

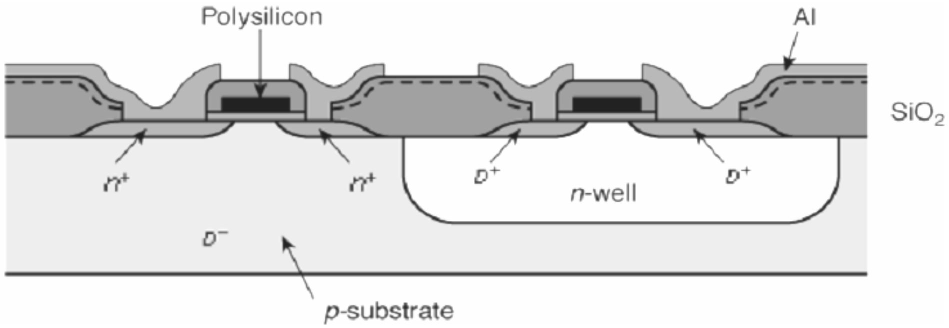




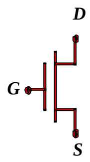
Conduction Characteristics of MOS Transistors (for fixed Vds)

- MOS transistors are majority-carrier devices.
- For n-channel transistors, the majority carriers are electrons conducted through a channel.
- A positive gate voltage (w.r.t. substrate) ***enhances*** the number of carriers in the channel, and increases conduction.
- **Threshold voltage** V_{tn} denotes the gate-to-source voltage above which conduction occurs.
- For **enhancement** mode devices, V_{tn} is positive; for **depletion** mode devices, V_{tn} is negative.
- p-channel devices are similar to n-channel devices, except that all voltages and currents are in opposite polarity.

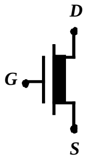
Cross-Section of CMOS Technology



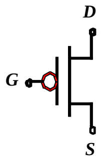
MOS transistors - Types and Symbols



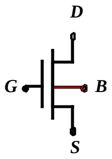
NMOS Enhancement



NMOS Depletion

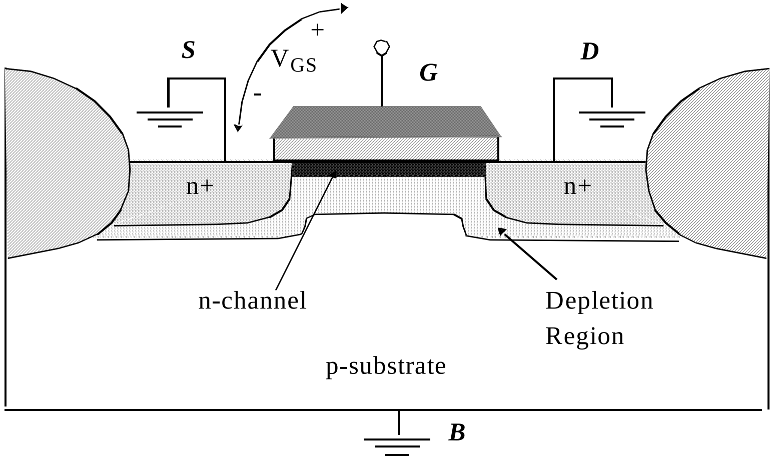


PMOS Enhancement



NMOS with Bulk Contact

Threshold Voltage: Concept



MOS transistor (1)

- Between the diffusion regions is the gate area form from a layer of polycrystaline silicon (known as **polysilicon**). This is separated from the substrate by a layer of **thin oxide** (made of silicon dioxide). Polysilicon is reasonable conductor and form the gate electrode.
- Underneath the thin oxide and between the n+ regions is the **channel**. The channel is conducting when a suitable electric field is applied to the gate.
- Due to geometric symmetry, there are **no distinctions** between the source and drain regions. However, we usually refer the terminal with more positive voltage the drain (for n-type) and less positive voltage the source.
- For a zero gate bias and a positive V_{DS}, no current flows between the drain and source because of the two **reverse biased diodes** shown in the diagram. The drain and source are therefore isolated from each other.
- Assuming that the substrate is always at the most negative supply voltage, these two diode should never become forward bias under normal operation.

MOS transistor (2)

- When a positive voltage is applied to the gate, an electric field is produced across the substrate which attracts electrons toward the gate. Eventually, the area under the gate changes from p-type to n-type, providing a conduction path between the source and drain.
- The gate-source voltage V_{GS} when a channel starts to form under that gate is called the **threshold voltage** V_T.
- The surface underneath the gate under this condition is said to be **inverted**. The surface is known as the **inversion layer.**
- As larger bias is applied to the gate the inversion layer becomes thicker
- An other p-n junction exists between the inversion layer and the substrate. This diode junction is **field induced**. Contrast this with the p-n junction between the source (or drain) and the substrate, which is created by a metallurgical process.

The Threshold Voltage

$$V_{T0} = \phi_{ms} - 2\phi_F - \underbrace{\frac{Q_B}{C_{ox}}}_{\text{Depletion Layer Charge}} - \underbrace{\frac{Q_{SS}}{C_{ox}}}_{\text{Surface Charge}} - \underbrace{\frac{Q_I}{C_{ox}}}_{\text{Implants}}$$

Workfunction Difference

$$V_T = V_{T0} + \overset{\text{Body Effect Coefficient}}{\gamma}\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

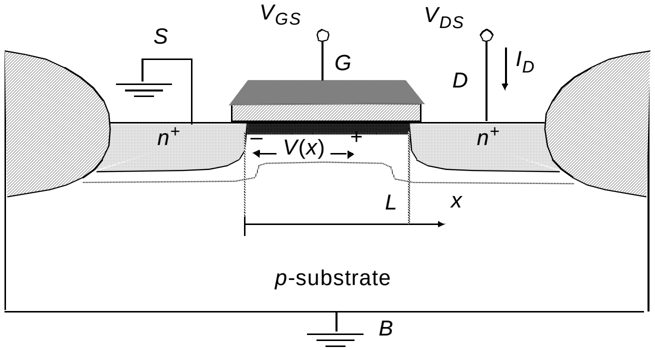
with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_A}}{C_{ox}}$$

Current-Voltage Relations



MOS transistor and its bias conditions

Current-Voltage Relations

Linear Region: $V_{DS} \le V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

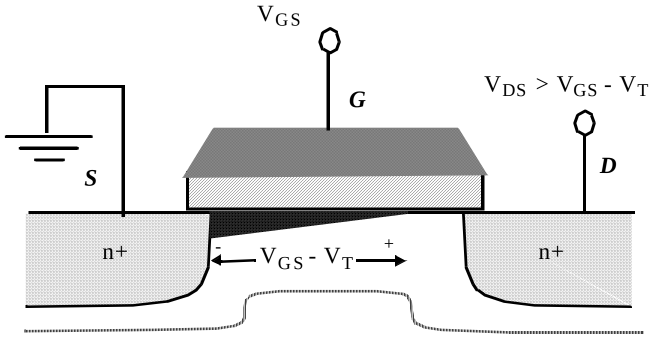
Process Transconductance Parameter

Saturation Mode: $V_{DS} \ge V_{GS} - V_T$

Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

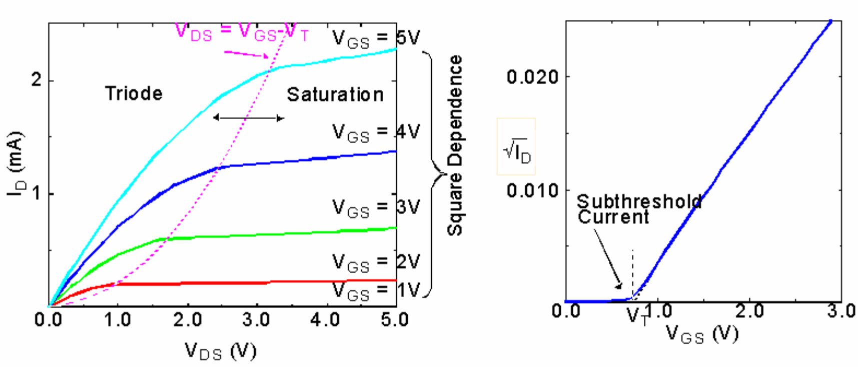
Transistor in Saturation



MOS transistor (3)

- As a voltage is applied between the source and drain, the inversion layer becomes thinner at the drain terminal due to interaction between V_G and V_D.
- If $V_{DS} < V_{GS} - V_T$, then the drain current Id is a function of both V_{GS} and V_{DS}. Furthermore, for a given V_{DS}, I_D increases linearly with ($V_{GS} - V_T$). The transistor is said to be operating in its **linear** or **resistive** region.
- If $V_{DS} > V_{GS} - V_T$, then $V_{GS} < V_T$ and no inversion layer can exist at the drain terminal. The channel is said to be ***'pinched-off'***. The transistor is operating in the **saturation** region, where the drain current is dependent on V_{GS} and is almost independent of V_{DS}.

I-V Relation

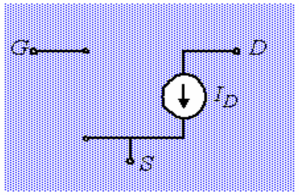


(a) I_D as a function of V_{DS}

(b) $\sqrt{I_D}$ as a function of V_{GS} (for V_{DS} = 5V)

NMOS Enhancement Transistor: W = 100 μm, L = 20 μm

A model for manual analysis



$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

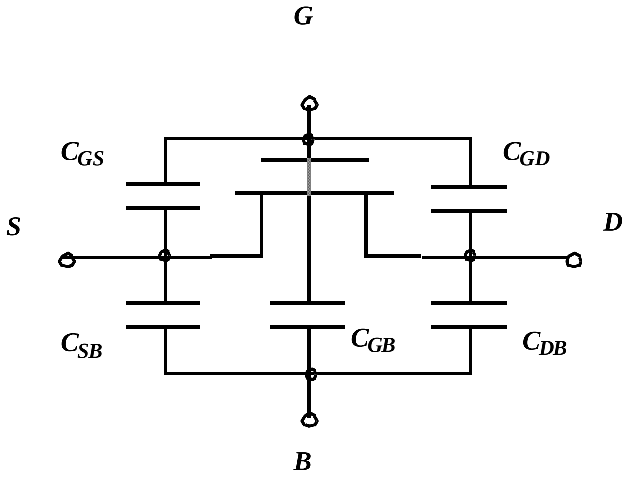
$$V_{DS} < V_{GS} - V_T$$

$$I_D = k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

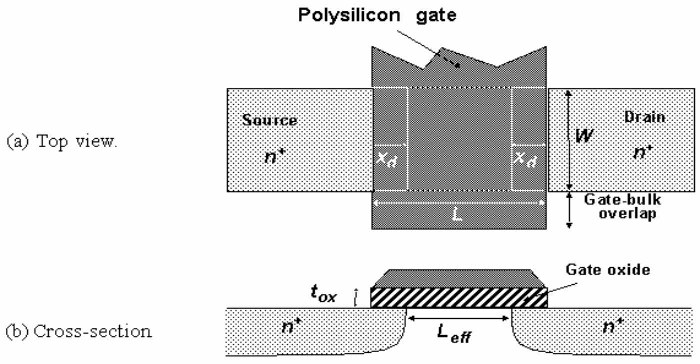
with

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

Dynamic Behavior of MOS Transistor



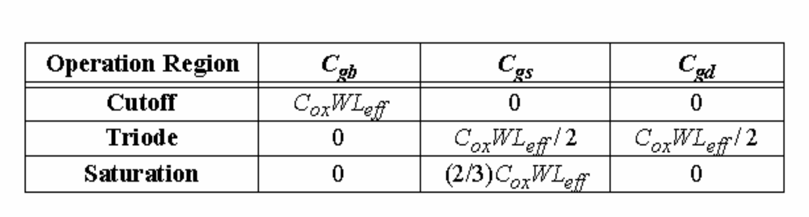
The Gate Capacitance



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}}WL$$

Average Gate Capacitance

Different distributions of gate capacitance for varying operating conditions



Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

- Most important regions in digital design: saturation and cut-off

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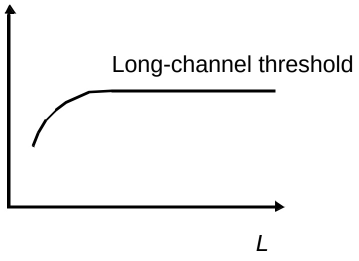
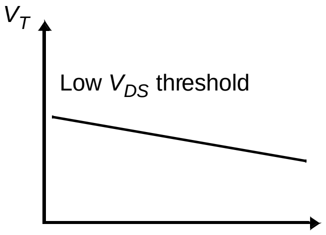
Issues concerning Sub-Micron MOS Transistors

- Threshold Variations
- Parasitic Resistances
- Velocity Saturation
- Mobility Degradation

Threshold Variations

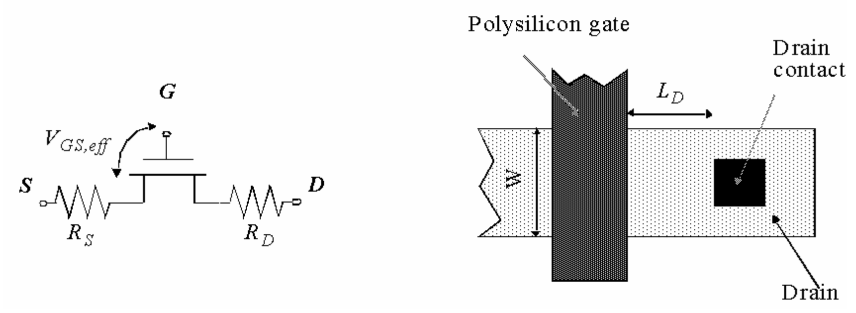


Threshold as a function of the length (for low V_{DS})

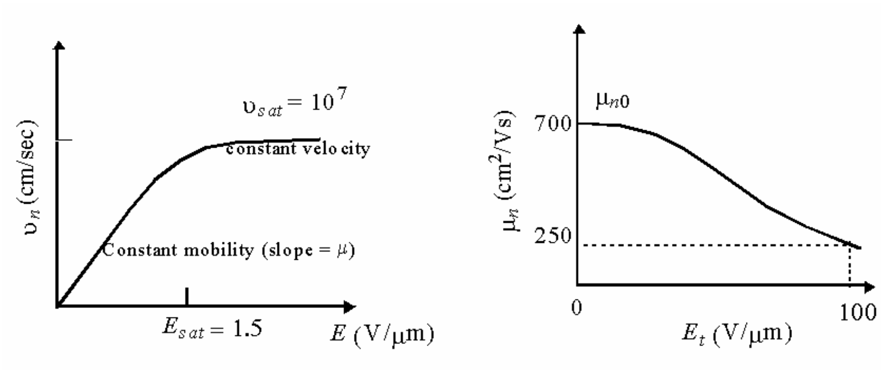


Drain-induced barrier lowering (for low L)

Parasitic Resistances



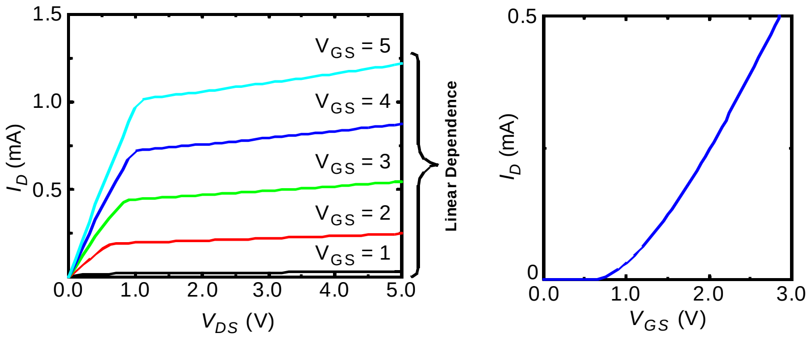
Velocity Saturation (1)



(a) Velocity saturation

(b) Mobility degradation

Velocity Saturation (2)

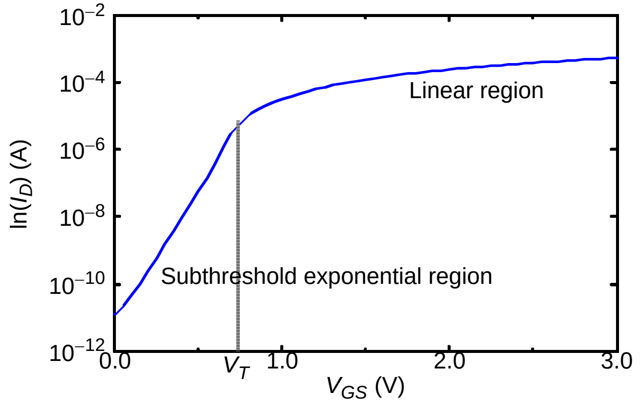


(a) I_D as a function of V_{DS}

(b) I_D as a function of V_{GS} (for V_{DS} = 5 V).

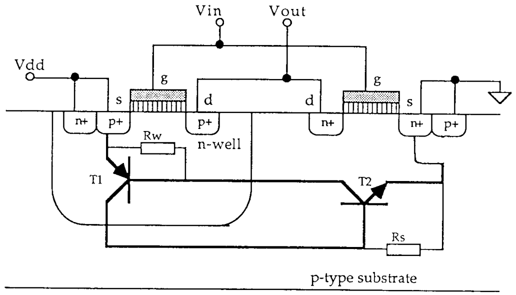
Linear Dependence on V_{GS}

Sub-Threshold Conduction



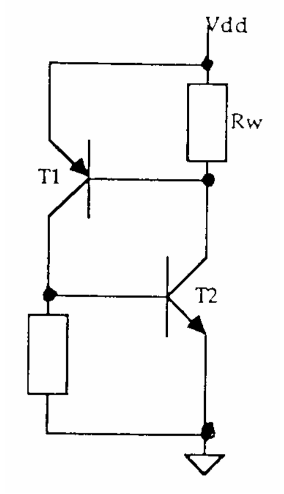
Latch-up problem (1)

- The p+ region of the p-transistor, the n-well and the p- substrate form a parasitic pnp transistor T1.
- The n- well, the p- substrate and the p+ source of the n-transistor forms another parasitic npn transistor T2.
- There exists two resistors Rw and Rs due to the resistive drop in the well area and the substrate area.



Latch-up problem (2)

- T1 and T2 form a thyristor circuit.
- If Rw and/or Rs are not 0, and for some reason (power-up, current spike etc), T1 or T2 are forced to conduct, Vdd will be shorted to Gnd through the small resistances and the transistors.
- Once the circuit is 'fired', both transistors will remain conducting due to the voltage drop across Rw and Rs. The only way to get out of this mode is to turn the power off.
- This condition is known as **latch-up**.
- To avoid latch-up, substrate-taps (tied to Gnd) and well-taps (tied to Vdd) are inserted as frequently as possible. This has the effect of shorting out Rw and Rs.



Outline

- MOS transistors
- **SPICE simulation**
- CMOS fabrication process
- Layout rules

What is SPICE Circuit Simulator?

- **SPICE** is a widely-used circuit-level simulator, originally from Berkeley.
- SPICE uses numerical techniques to solve nodal analysis of circuit. It supports the following:
  - Textual input to specify circuit & simulation commands
  - Text or graphical output format for simulation results
- You can use SPICE to specify these circuit components:
  - Resistors, Capacitors, Inductors
  - Independent sources (V, I), Dependent sources (V, I)
  - Transmission lines
  - Active devices (diodes, BJTs, JFETS, MOSFETS)
- You can use SPICE to perform the following types circuit analysis:
  - non-linear d.c.
  - non-linear transient
  - linear a.c.
  - Noise & temperature

SPICE MODELS

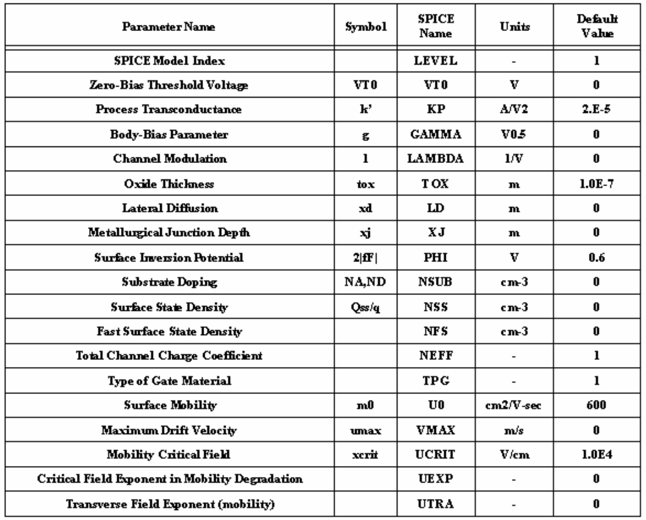
Level 1: Long Channel Equations - Very Simple

Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations

Level 3: Semi-Emperical - Based on curve fitting to measured devices

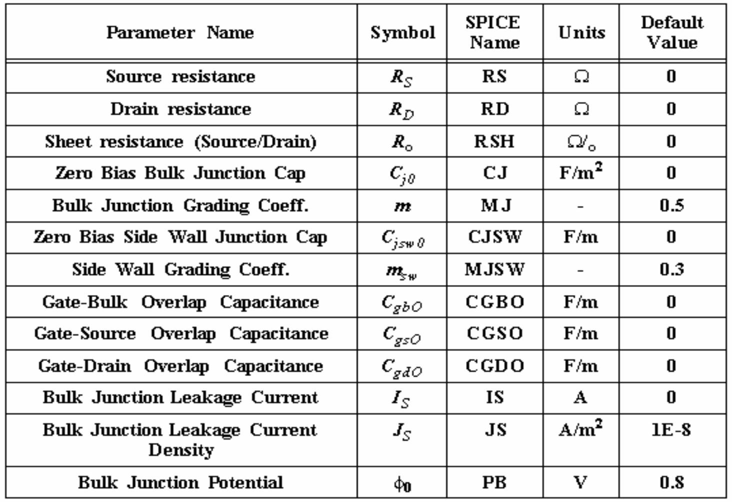
Level 4 (BSIM): Emperical - Simple and Popular

MAIN MOS SPICE PARAMETERS



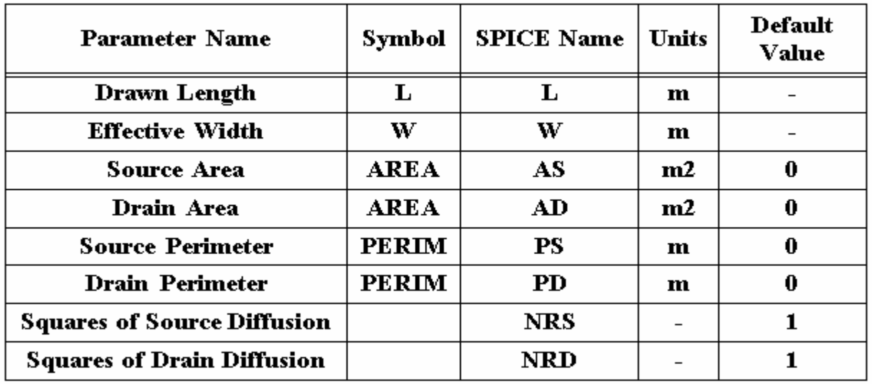
Parameter Name	Symbol	SPICE Name	Units	Default Value
SPICE Model Index		LEVEL	-	1
Zero-Bias Threshold Voltage	VT0	VT0	V	0
Process Transconductance	k'	KP	A/V2	2.E-5
Body-Bias Parameter	g	GAMMA	V0.5	0
Channel Modulation	l	LAMBDA	1/V	0
Oxide Thickness	tox	TOX	m	1.0E-7
Lateral Diffusion	xd	LD	m	0
Metallurgical Junction Depth	xj	XJ	m	0
Surface Inversion Potential	2|fF|	PHI	V	0.6
Substrate Doping	NA,ND	NSUB	cm-3	0
Surface State Density	Qss/q	NSS	cm-3	0
Fast Surface State Density		NFS	cm-3	0
Total Channel Charge Coefficient		NEFF	-	1
Type of Gate Material		TPG	-	1
Surface Mobility	m0	U0	cm2/V-sec	600
Maximum Drift Velocity	umax	VMAX	m/s	0
Mobility Critical Field	xcrit	UCRIT	V/cm	1.0E4
Critical Field Exponent in Mobility Degradation		UEXP	-	0
Transverse Field Exponent (mobility)		UTRA	-	0

SPICE Parameters for Parasitics



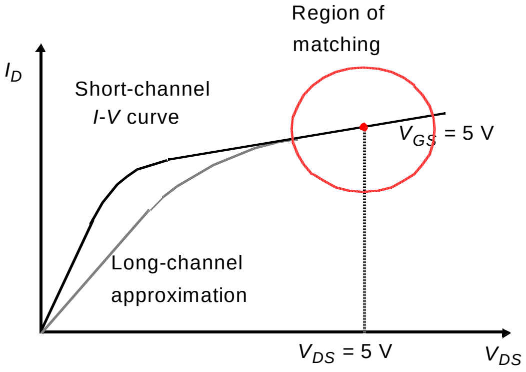
Parameter Name	Symbol	SPICE Name	Units	Default Value
Source resistance	R_S	RS	Ω	0
Drain resistance	R_D	RD	Ω	0
Sheet resistance (Source/Drain)	$R_\circ$	RSH	$\Omega/_\circ$	0
Zero Bias Bulk Junction Cap	C_{j0}	CJ	F/m^2	0
Bulk Junction Grading Coeff.	m	MJ	-	0.5
Zero Bias Side Wall Junction Cap	C_{jsw0}	CJSW	F/m	0
Side Wall Grading Coeff.	m_{sw}	MJSW	-	0.3
Gate-Bulk Overlap Capacitance	C_{gb0}	CGBO	F/m	0
Gate-Source Overlap Capacitance	C_{gs0}	CGSO	F/m	0
Gate-Drain Overlap Capacitance	C_{gd0}	CGDO	F/m	0
Bulk Junction Leakage Current	I_S	IS	A	0
Bulk Junction Leakage Current Density	J_S	JS	A/m^2	1E-8
Bulk Junction Potential	ϕ_0	PB	V	0.8

SPICE Transistors Parameters



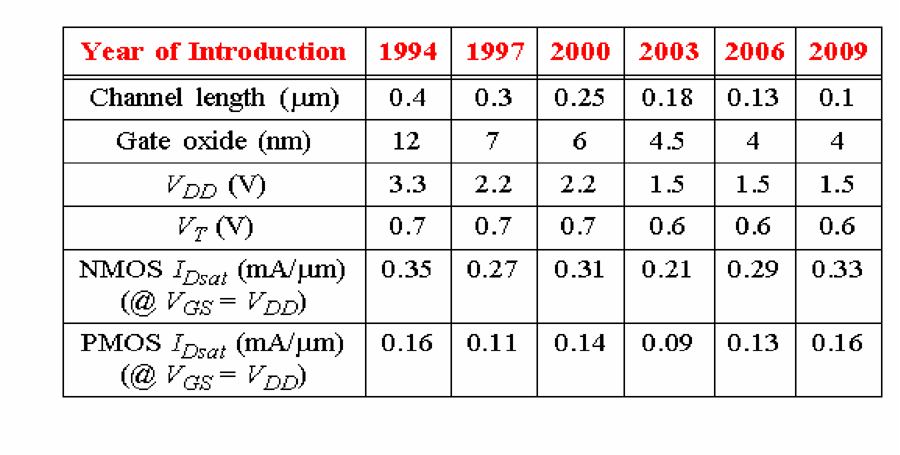
Parameter Name	Symbol	SPICE Name	Units	Default Value
Drawn Length	L	L	m	-
Effective Width	W	W	m	-
Source Area	AREA	AS	m2	0
Drain Area	AREA	AD	m2	0
Source Perimeter	PERIM	PS	m	0
Drain Perimeter	PERIM	PD	m	0
Squares of Source Diffusion		NRS	-	1
Squares of Drain Diffusion		NRD	-	1

Fitting level-1 model for manual analysis



Select k' and λ such that best matching is obtained @ $V_{gs} = V_{ds} = V_{DD}$

Technology Evolution



Year of Introduction	1994	1997	2000	2003	2006	2009
Channel length (µm)	0.4	0.3	0.25	0.18	0.13	0.1
Gate oxide (nm)	12	7	6	4.5	4	4
V_{DD} (V)	3.3	2.2	2.2	1.5	1.5	1.5
V_T (V)	0.7	0.7	0.7	0.6	0.6	0.6
NMOS I_{Dsat} (mA/µm) (@ $V_{GS} = V_{DD}$)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{Dsat} (mA/µm) (@ $V_{GS} = V_{DD}$)	0.16	0.11	0.14	0.09	0.13	0.16

Outline

- MOS transistors
- SPICE simulation
- **CMOS fabrication process**
- Layout rules

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

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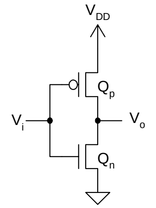
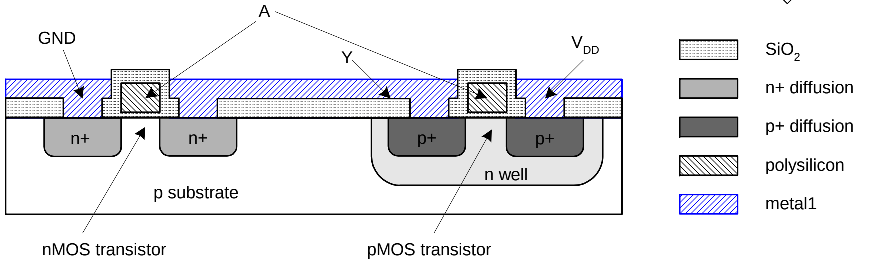
Inverter Cross-section

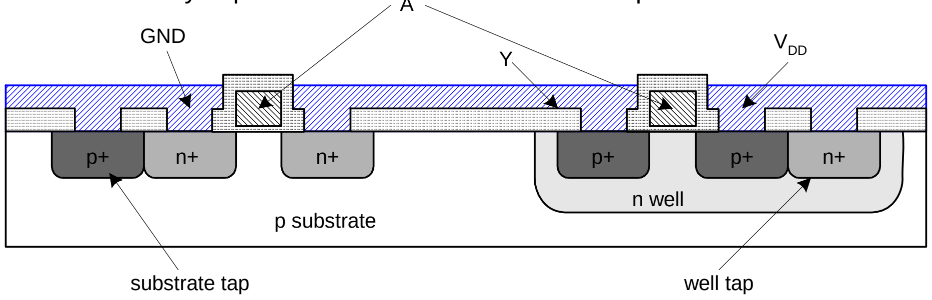
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors





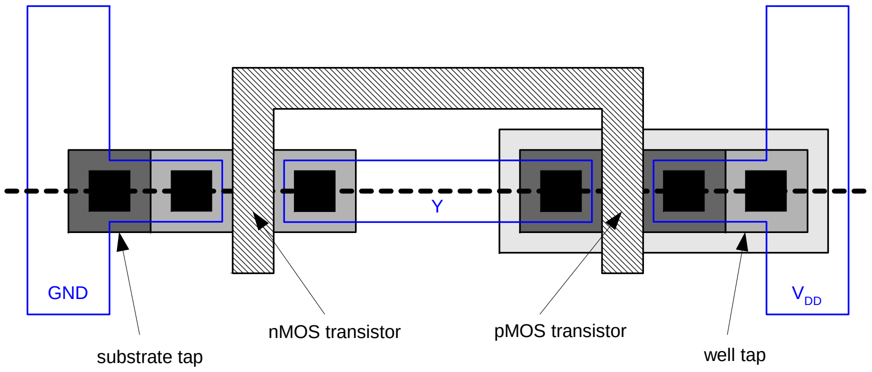
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps



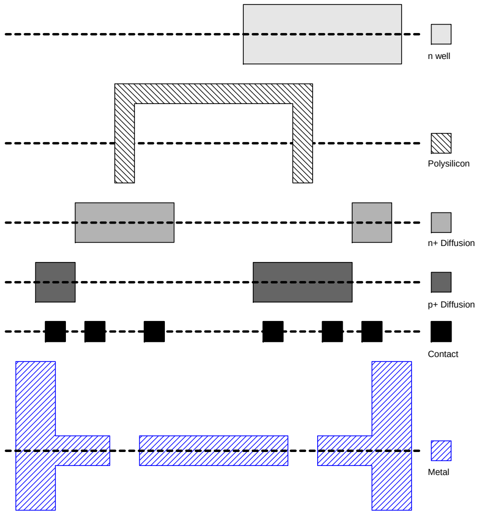
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

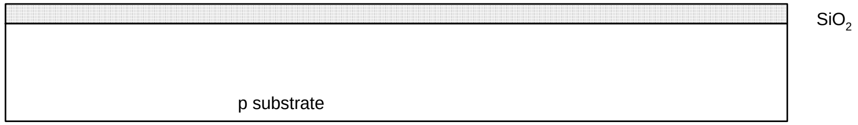


Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2

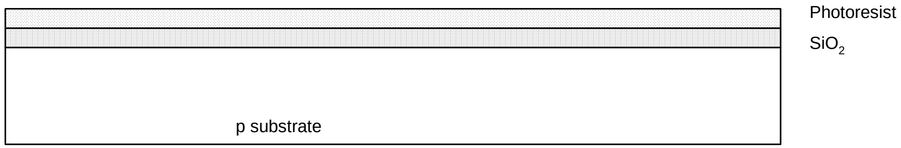
Oxidation

- Grow SiO_2 on top of Si wafer
  - 900 – 1200 C with H_2O or O_2 in oxidation furnace



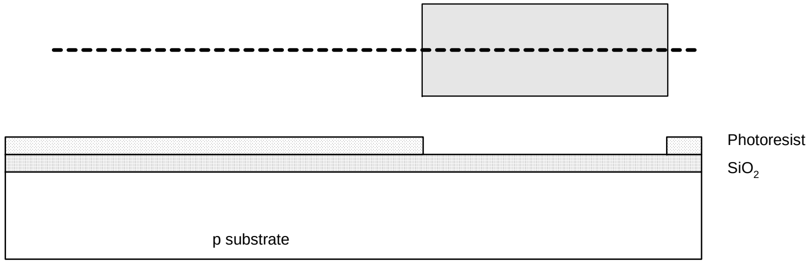
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light



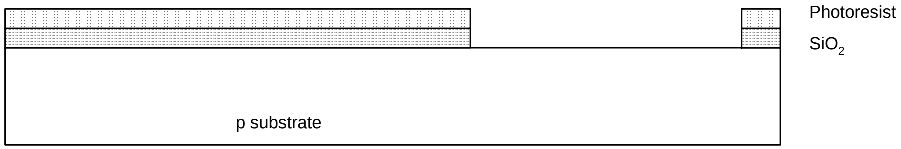
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



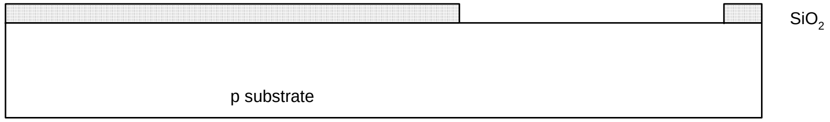
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed



Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



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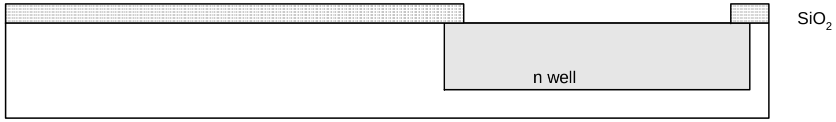
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO_2, only enter exposed Si

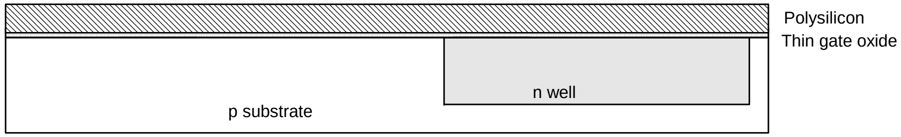


Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

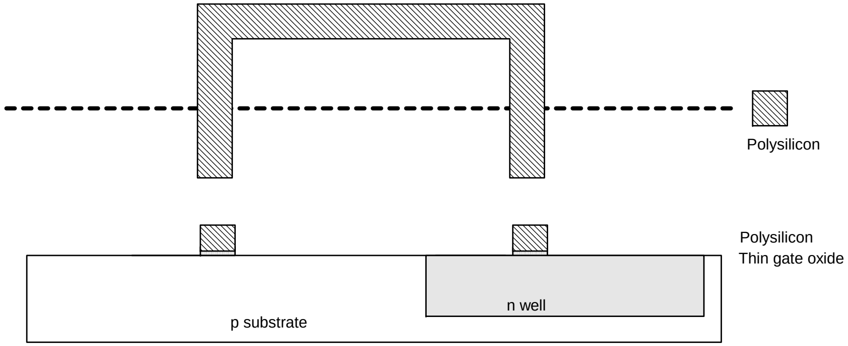
Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



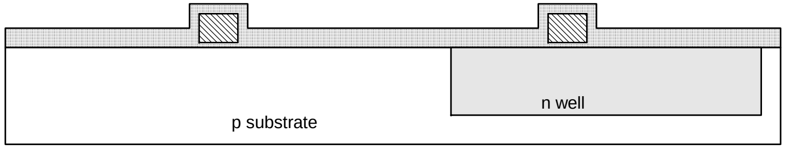
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



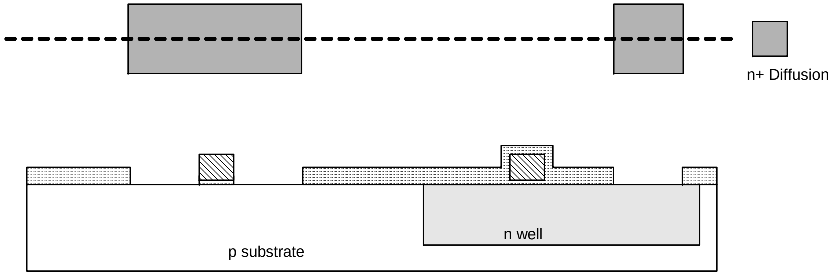
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



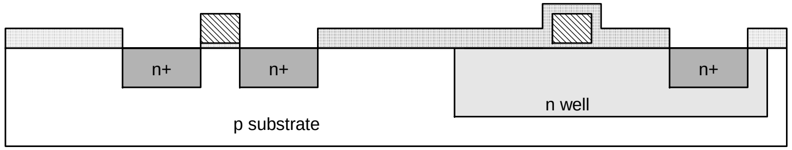
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing



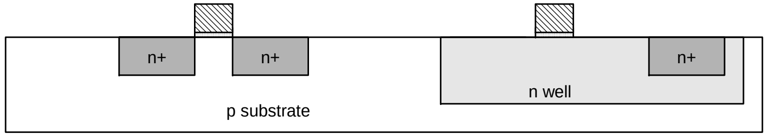
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



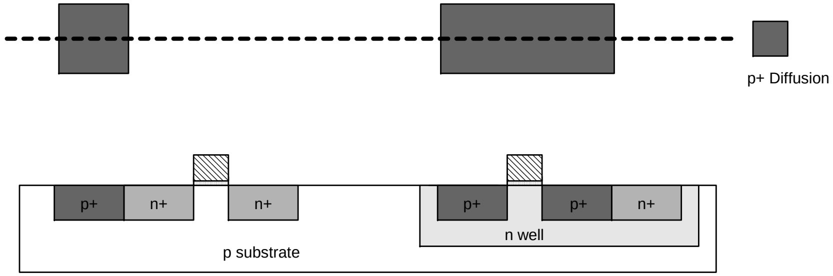
N-diffusion cont.

- Strip off oxide to complete patterning step



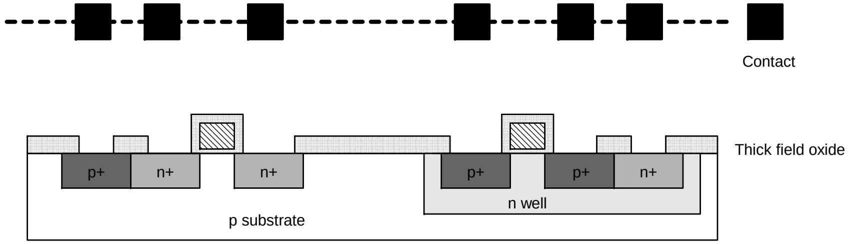
P-diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



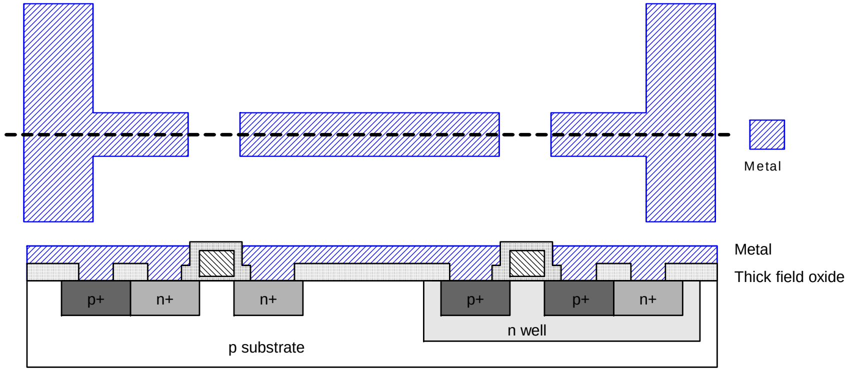
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metalization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- **Layout rules**

Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size *f* = distance between source and drain
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3$ µm in 0.6 µm process

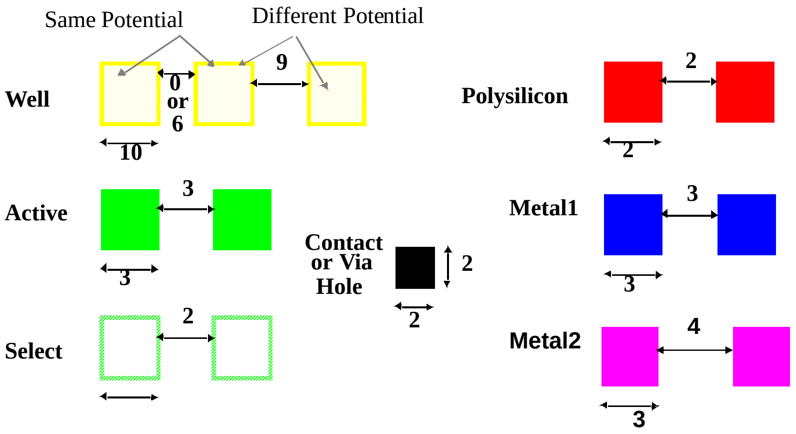
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

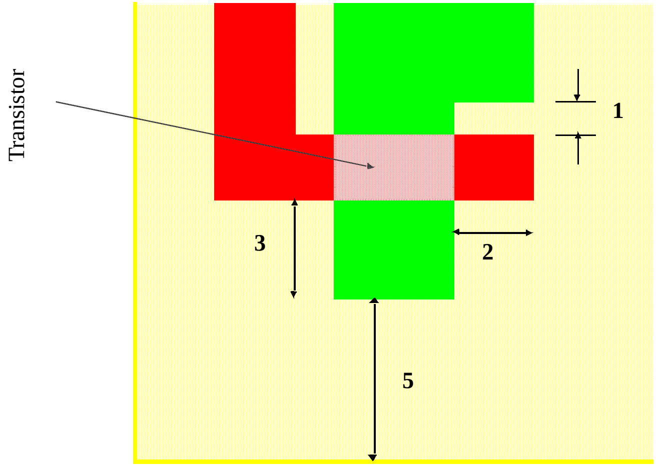
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	□
Active Area (n+,p+)	Green	🟩
Select (p+,n+)	Green	⬚
Polysilicon	Red	🟥
Metal1	Blue	🟦
Metal2	Magenta	🟪
Contact To Poly	Black	⬛
Contact To Diffusion	Black	⬛
Via	Black	⬛

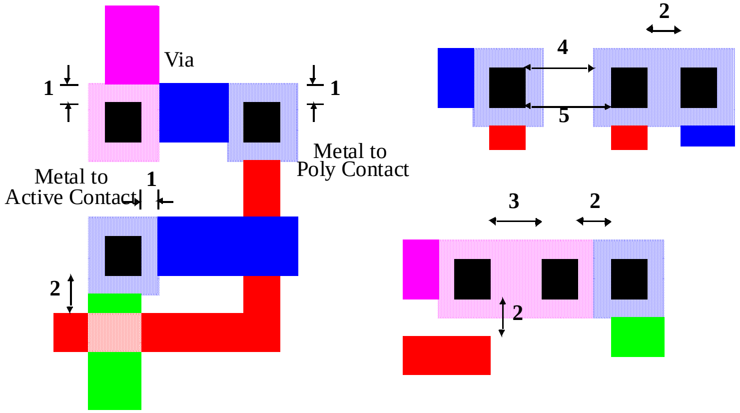
Intra Layer Design Rules



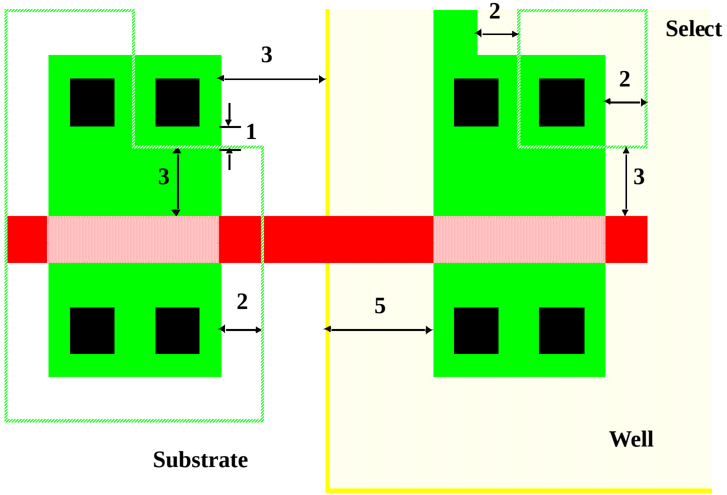
Transistor Layout



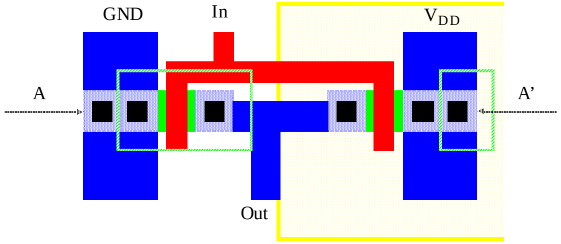
Via’s and Contacts



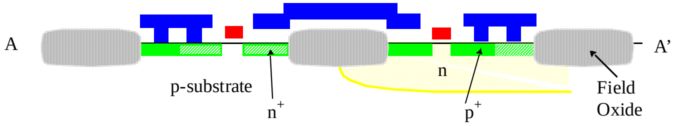
Select Layer



CMOS Inverter Layout



(a) Layout



(b) Cross-Section along A-A'

Summary

- MOS transistor: majority carrier device – building block of integrated circuits
- SPICE: popular circuit level simulator that applies nodal analysis of circuit
- CMOS transistors are fabricated on silicon wafer
  - Lithography process
  - Different materials are deposited or etched in each step
- Layout rules: contract between IC designer and process engineer
  - Guidelines for constructing process masks