Topic 2

Basic MOS Theory, SPICE Simulation, CMOS Fabrication

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Recommended Reading

- J. Rabaey et. al. “Digital Integrated Circuits: A Design Perspective”: Chapter 2 (2.1 – 2.3), Chapter 3 (3.3)
- Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”: Chapter 2, Chapter 3 (3.2), Chapter 5.

Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules

Based on slides/material by...

- D. Harris http://www_cmosvlsi.com/coursematerials.html Weste and Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, Addison Wesley
**MOS Transistor**

- Shown here is the cross-section of an n-channel enhancement transistor:
- Substrate is moderately doped with p-type material. Substrate in digital circuit is usually connected to $V_{\text{Gnd}}$ (ground).
- The source and drain regions are heavily doped with n-type material through diffusion. These are often referred to as the diffusion regions.

**Conduction Characteristics of MOS Transistors (for fixed $V_{ds}$)**

- MOS transistors are majority-carrier devices.
- For n-channel transistors, the majority carriers are electrons conducted through a channel.
- A positive gate voltage (w.r.t. substrate) enhances the number of carriers in the channel, and increases conduction.
- **Threshold voltage** $V_{tn}$ denotes the gate-to-source voltage above which conduction occurs.
- For enhancement mode devices, $V_{tn}$ is positive; for depletion mode devices, $V_{tn}$ is negative.
- p-channel devices are similar to n-channel devices, except that all voltages and currents are in opposite polarity.

**Cross-Section of CMOS Technology**

**MOS transistors - Types and Symbols**
Threshold Voltage: Concept

- When a positive voltage is applied to the gate, an electric field is produced across the substrate which attracts electrons toward the gate. Eventually, the area under the gate changes from p-type to n-type, providing a conduction path between the source and drain.
- The gate-source voltage $V_{GS}$ when a channel starts to form under that gate is called the threshold voltage $V_T$.
- The surface underneath the gate under this condition is said to be inverted. The surface is known as the inversion layer.
- As larger bias is applied to the gate the inversion layer becomes thicker.
- An other p-n junction exists between the inversion layer and the substrate. This diode junction is field induced. Contrast this with the p-n junction between the source (or drain) and the substrate, which is created by a metallurgical process.

MOS transistor (1)

- Between the diffusion regions is the gate area form from a layer of polycrystalline silicon (known as polysilicon). This is separated from the substrate by a layer of thin oxide (made of silicon dioxide). Polysilicon is reasonable conductor and form the gate electrode.
- Underneath the thin oxide and between the n+ regions is the channel. The channel is conducting when a suitable electric field is applied to the gate.
- Due to geometric symmetry, there are no distinctions between the source and drain regions. However, we usually refer the terminal with more positive voltage the drain (for n-type) and less positive voltage the source.
- For a zero gate bias and a positive $V_{DS}$, no current flows between the drain and source because of the two reverse biased diodes shown in the diagram. The drain and source are therefore isolated from each other.
- Assuming that the substrate is always at the most negative supply voltage, these two diode should never become forward bias under normal operation.

MOS transistor (2)

- When a positive voltage is applied to the gate, an electric field is produced across the substrate which attracts electrons toward the gate. Eventually, the area under the gate changes from p-type to n-type, providing a conduction path between the source and drain.
- The gate-source voltage $V_{GS}$ when a channel starts to form under that gate is called the threshold voltage $V_T$.
- The surface underneath the gate under this condition is said to be inverted. The surface is known as the inversion layer.
- As larger bias is applied to the gate the inversion layer becomes thicker.
- An other p-n junction exists between the inversion layer and the substrate. This diode junction is field induced. Contrast this with the p-n junction between the source (or drain) and the substrate, which is created by a metallurgical process.

The Threshold Voltage

\[
V_T = V_{TB} + \gamma \sqrt{\frac{2 \Phi_p - V_{SB} - V_T}{2 \Phi_p}}
\]

with

\[
V_{TB} = \Phi_{mS} - 2 \Phi_p - \frac{\phi_B}{C_{ox}} - \frac{\phi_{SS}}{C_{ox}} - \frac{\phi_I}{C_{ox}}
\]

and

\[
\gamma = \frac{q g_{mS} N_D}{C_{ox}}
\]
Current-Voltage Relations

\[ I_D = \frac{\kappa}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \]

\[ \kappa' = \mu_n \frac{C_{ox}}{L} = \frac{W}{L} \frac{C_{ox}}{t_{ox}} \]

**Linear Region:** \( V_{DS} \leq V_{GS} - V_T \)

**Saturation Mode:** \( V_{DS} \geq V_{GS} - V_T \)

\[ I_D = \frac{\nu_{n}}{2} \left( V_{GS} - V_T \right)^2 \left( 1 + \kappa' V_{DS} \right) \]

Transistor in Saturation

- As a voltage is applied between the source and drain, the inversion layer becomes thinner at the drain terminal due to interaction between \( V_G \) and \( V_D \).
- If \( V_{DS} < V_{GS} - V_T \), then the drain current \( I_D \) is a function of both \( V_{GS} \) and \( V_{DS} \). Furthermore, for a given \( V_{DS} \), \( I_D \) increases linearly with \( (V_{GS} - V_T) \). The transistor is said to be operating in its linear or resistive region.
- If \( V_{DS} > V_{GS} - V_T \), then \( V_{GS} < V_T \) and no inversion layer can exist at the drain terminal. The channel is said to be 'pinched-off'. The transistor is operating in the saturation region, where the drain current is dependent on \( V_{GS} \) and is almost independent of \( V_{DS} \).
I-V Relation

(a) $I_D$ as a function of $V_{DS}$

(b) $V_D$ as a function of $V_{GS}$

NMOS Enhancement Transistor: $W = 100 \mu m, L = 20 \mu m$

A model for manual analysis

$$V_{DS} > V_{GS} - V_T$$

$$I_D = \frac{W}{L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right)$$

$$V_{DS} < V_{GS} - V_T$$

$$I_D = \frac{W}{L} \left(V_{GS} - V_T\right)^2 \frac{V_{DS}^2}{2}$$

with

$$V_T = V_{TO} + \gamma \left(\sqrt{-2\phi_F} + \sqrt{V_{SB}} - \sqrt{-2\phi_F}\right)$$

Dynamic Behavior of MOS Transistor

The Gate Capacitance

$$C_{Gate} = \frac{d_{ox}}{W/L}$$
**Average Gate Capacitance**

Different distributions of gate capacitance for varying operating conditions.

<table>
<thead>
<tr>
<th>Operation Region</th>
<th>$C_{gd}$</th>
<th>$C_{gs}$</th>
<th>$C_{gd}$</th>
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<tbody>
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<td>$C_{gd}W_{L_{eff}}$</td>
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<td>$C_{gd}W_{L_{eff}}/2$</td>
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<td>Saturation</td>
<td>0</td>
<td>$(2/3)C_{gd}W_{L_{eff}}$</td>
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</table>

- Most important regions in digital design: saturation and cut-off

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**Issues concerning Sub-Micron MOS Transistors**

- Threshold Variations
- Parasitic Resistances
- Velocity Saturation
- Mobility Degradation

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**Threshold Variations**

- Long-channel threshold
- Low $V_{DS}$ threshold
- Drain-induced barrier lowering (for low $L$)

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**Parasitic Resistances**

- Polysilicon gate
- Drain contact
- Drain

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**MOS Theory, SPICE, Fabrication**

Introduction to Digital Integrated Circuit Design

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**MOS Theory, SPICE, Fabrication**

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**MOS Theory, SPICE, Fabrication**

Introduction to Digital Integrated Circuit Design

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### Velocity Saturation (1)

- **Graph (a):**
  - $V_{sat} = 10^7$
  - Constant velocity
  - $E_{sat} = 1.5$

- **Graph (b):**
  - Mobility degradation
  - $\mu_c$
  - $E_t (V/\mu m)$

#### Linear Dependence on $V_{GS}$

- **Graph (a):**
  - $I_D$ as a function of $V_{DS}$
  - $V_{GS} = 5$ V

- **Graph (b):**
  - $I_D$ as a function of $V_{GS}$
  - $V_{DS} = 5$ V

### Sub-Threshold Conduction

- **Graph:**
  - $\ln(I_D) (A)$ vs. $V_{GS}$ (V)
  - Linear region
  - Subthreshold exponential region

### Latch-up problem (1)

- The p+ region of the p-transistor, the n-well and the p- substrate form a parasitic pnp transistor T1.
- The n- well, the p- substrate and the p+ source of the n-transistor forms another parasitic npn transistor T2.
- There exists two resistors $R_w$ and $R_s$ due to the resistive drop in the well area and the substrate area.
Latch-up problem (2)

- T1 and T2 form a thyristor circuit.
- If Rw and/or Rs are not 0, and for some reason (power-up, current spike etc), T1 or T2 are forced to conduct, Vdd will be shorted to Gnd through the small resistances and the transistors.
- Once the circuit is 'fired', both transistors will remain conducting due to the voltage drop across Rw and Rs. The only way to get out of this mode is to turn the power off.
- This condition is known as **latch-up**.
- To avoid latch-up, substrate-taps (tied to Gnd) and well-taps (tied to Vdd) are inserted as frequently as possible. This has the effect of shorting out Rw and Rs.

Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules

What is SPICE Circuit Simulator?

- **SPICE** is a widely-used circuit-level simulator, originally from Berkeley.
- SPICE uses numerical techniques to solve nodal analysis of circuit. It supports the following:
  - Textual input to specify circuit & simulation commands
  - Text or graphical output format for simulation results
- You can use SPICE to specify these circuit components:
  - Resistors, Capacitors, Inductors
  - Independent sources (V, I), Dependent sources (V, I)
  - Transmission lines
  - Active devices (diodes, BJTs, JFETS, MOSFETS)
- You can use SPICE to perform the following types circuit analysis:
  - non-linear d.c.
  - non-linear transient
  - linear a.c.
  - Noise & temperature

SPICE MODELS

**Level 1: Long Channel Equations - Very Simple**

**Level 2: Physical Model - Includes Velocity Saturation and Threshold Variations**

**Level 3: Semi-Emperical - Based on curve fitting to measured devices**

**Level 4 (BSIM): Emperical - Simple and Popular**
### MAIN MOS SPICE PARAMETERS

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Symbol</th>
<th>SPICE Name</th>
<th>Units</th>
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<td>VT0</td>
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### SPICE Parameters for Parasitics

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<tr>
<td>Drain resistance</td>
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<td>Rdoire</td>
<td>Ω</td>
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<tr>
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<td>Rsoire</td>
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<td>CJ</td>
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<td>MJ</td>
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### SPICE Transistors Parameters

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<td>Source Area</td>
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<tr>
<td>Drain Area</td>
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<tr>
<td>Squares of Drain Diffusion</td>
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</tbody>
</table>

### Fitting level-1 model for manual analysis

Select $k'$ and $\lambda$, such that best matching is obtained @ $V_{gs} = V_{ds} = V_{DD}$

- Short-channel $i-V$ curve
- Long-channel approximation
- Region of matching
- $V_{DS} = 5\, V$
- $V_{DS} = 5\, V$
Technology Evolution

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<td>Channel length (μm)</td>
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<td>NMOS $I_{Dsat}$ (mA/μm) (@ $V_{GS} = V_{DD}$)</td>
<td>0.35</td>
<td>0.27</td>
<td>0.31</td>
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<tr>
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<td>0.11</td>
<td>0.14</td>
<td>0.09</td>
<td>0.13</td>
<td>0.16</td>
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</tbody>
</table>

Outline

- MOS transistors
- SPICE simulation
- CMOS fabrication process
- Layout rules

CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
Well and Substrate Taps

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps

Inverter Mask Set

- Transistors and wires are defined by masks
- Cross-section taken along dashed line

Detailed Mask Views

- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO₂ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO₂
**Oxidation**

- Grow SiO$_2$ on top of Si wafer
  - 900 – 1200 °C with H$_2$O or O$_2$ in oxidation furnace

**Photoresist**

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light

**Lithography**

- Expose photoresist through n-well mask
- Strip off exposed photoresist

**Etch**

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
  - Only attacks oxide where resist has been exposed
**Strip Photoresist**

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step

**n-well**

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO₂, only enter exposed Si

**Strip Oxide**

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

**Polysilicon**

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
### Polysilicon Patterning

- Use same lithography process to pattern polysilicon

![Polysilicon Patterning Diagram](image1)

### Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

![Self-Aligned Process Diagram](image2)

### N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing

![N-diffusion Diagram](image3)

### N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

![N-diffusion cont. Diagram](image4)
**N-diffusion cont.**

- Strip off oxide to complete patterning step

**P-diffusion**

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

**Contacts**

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

**Metalization**

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires
Outline

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Layout

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size $f = \text{distance between source and drain}
  - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - E.g. $\lambda = 0.3 \mu m$ in 0.6 $\mu m$ process

Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)

CMOS Process Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>Color</th>
<th>Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well (p,n)</td>
<td>Yellow</td>
<td></td>
</tr>
<tr>
<td>Active Area (n+,p+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Select (p+,n+)</td>
<td>Green</td>
<td></td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
<td></td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
<td></td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta</td>
<td></td>
</tr>
<tr>
<td>Contact To Poly</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Contact To Diffusion</td>
<td>Black</td>
<td></td>
</tr>
<tr>
<td>Via</td>
<td>Black</td>
<td></td>
</tr>
</tbody>
</table>
CMOS Inverter Layout

(a) Layout

(b) Cross-Section along A-A'

Summary

- MOS transistor: majority carrier device – building block of integrated circuits
- SPICE: popular circuit level simulator that applies nodal analysis of circuit
- CMOS transistors are fabricated on silicon wafer
  - Lithography process
  - Different materials are deposited or etched in each step
- Layout rules: contract between IC designer and process engineer
  - Guidelines for constructing process masks